10 MHz (typ.) $V_{CC} = 10 V, C_1 = 50 pF$

0.45 V_{CC} (typ.)

100 nW/ (typ.)

3 V to 15 V

Drive 2 LTTL loads

National Semiconductor

MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift reaister.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

Features

- Medium speed operation
- High noise immunity
- Low power
- Tenth power TTL compatible
- Wide supply voltage range
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout.

Applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Block and Connection Diagrams



Function Table

INPUTS						OUTPUTS					
MODE	CLOCKS			PARALLEL							
CONTROL	2 (L)	1 (R)	SERIAL	Α	8	С	D	0 _A	O8	QC	QD
H	н	x	×	x	x	×	х	0 ₄₀	O _{B0}	0 _{c0}	Q _{D0}
н	4	x	×	а	Þ	c	d	a	b	c	đ
н	4	×	×	001	a _c †	o₀†	d	084	Q _{Cn}	Q _D	đ
L	L	н	×	×	x	×	x	O _{A0}	O _{GO}	O _{co}	000
L	×	4	н	x	x	×	x	н	OAn	Q _{8n}	0c.,
L	x	1	ι	x	x	×	x	L	0 _{An}	Q _{Bn}	Q _C
t	L	L	x	x	×	x	х	OA0	O _{B0}	0 _{co}	000
1	L	L	×	х	x	×	×	Q _{A0}	OBO	O _C o	000
4	L	н	x	x	x	×	х	Q _{A0}	O _{B0}	O _{CO}	000
t	н	L	×	×	×	x	x	O _{A0}	O _{B0}	Oco	000
t	н	н	×	×	×	×	x	040	O _{B0}	O _{co}	Q _{D0}
t	L	н	x	×	x	x	x	Undefi	ned		
4	н	L	×	x	x	x	x	Operating Conditions			

*Shifting left requires external connection of Og to A, Oc to B, and Op to C. Serial data is entered at input D H × high level (tready state), L × fow level (tready state), X × inrelevant layr input, including transitiont) • × transition from light to low level, 1 × transition from low to high feed

b.c. d.= the level of steady state input at inputs A. B. C or D, respectively

 Q_{AD} , Q_{BD} , Q_{CD} , Q_{DD} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady state input co Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent \perp transition of the



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Absolute Maximum Ratings (Note 1)

Voltage at Any Pin **Operating Temperature** MM54Č95 MM74C95 Storage Tomporature

-0.3 V to V_{CC}+0.3 V -55°C to +125°C -40°C to +85°C 65%C to 1 150%C

Maximum V_{CC} Voltage Package Dissipation Operating V_{CC} Range Lead Temperature (Soldering, 10 sec.)

18V 500 mW +3V to +15V 300°C

Parameter			Conditions	Min.	Тур.	Max.	Units
	CMOS to CMOS	· · · · ·					
V _{IN(1)}	Logical "1" Input Voltage		= 5.0 V = 10 V	3.5 8.0			v v
VIN(0)	Logical "0" Input Voltage		= 5.0 V = 10 V			1.5 2.0	v
V _{OUT(1)}	Logical "1" Output Voltage		= 5.0 V = 10 V	4.5 9			V V
V _{OUT(0)}	Logical "0" Output Voltage		= 5.0 V = 10 V			0.5 1	v v
I _{IN(1)}	Logical "1" Input Current	V _{cc}	= 15 V			1	μA
IIN(0)	Logical "0" Input Current	V _{cc}	= 15 V	-1			μΑ
Icc	Supply Current		= 15 V		0.050	300	μA
	Low Power TTL/CMOS Interface					L	•
V _{IN(1)}	Logical "1" Input Voltage		, $V_{CC} = 4.5 V$, $V_{CC} = 4.75 V$	V _{CC} – 1.5 V _{CC} – 1.5			v v
V _{IN(0)}	Logical "0" Input Voltage		, V _{CC} = 4.5 V , V _{CC} = 4.75 V			0.8 0.8	V V
V _{OUT(1)}	Logical "1" Output Voltage		, $V_{CC} = 4.5 \text{ V}$, $I_0 = 360 \mu \text{A}$, $V_{CC} = 4.75 \text{ V}$, $I_0 = 360 \mu \text{A}$	2.4 2.4			V V
V _{OUT(0)}	Logical "0" Output Voltage	54C, $V_{CC} = 4.5 \text{ V}$, $I_0 = 360 \mu\text{A}$ 74C, $V_{CC} = 4.75 \text{ V}$, $I_0 = 360 \mu\text{A}$				0.4 0.4	v v
	Output Drive (See 54C/74C Family Cha	aracte	ristics Data Sheet)				
ISOURCE			= 5.0 V, V _{IN(0)} = 0 V = 25°C, V _{OUT} = 0 V	-1.75			mA
ISOURCE	Output Source Current		= 10 V, V _{IN(0)} = 0 V = 25°C, V _{OUT} = 0 V	-8.0			mA
I _{SINK}	Output Sink Current		= 5.0 V, V _{IN(1)} = 5.0 V = 25°C, V _{OUT} = V _{CC}	1.75			mA
I _{SINK}	Output Sink Current		= 10 V, V _{IN(1)} = 10 V = 25°C, V _{OUT} = V _{CC}	8.0			mA
AC EI	ectrical Characteristics TA	= 25°C	C, $C_L = 50 \text{pF}$, unless other	wise noted.			
	Parameter		Conditions	Min.	Тур.	Max.	Units
t _{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q		$V_{CC} = 5.0 V$ $V_{CC} = 10 V$		200 80	400 160	ns ns
t _{s0} , t _{s1}			$V_{CC} = 5.0 V$ $V_{CC} = 10 V$	60 25	30 10		ns ns
						1	1

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Time After Clock Pulse that Data must

Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)

Time Prior to Clock Pulse that Mode

Maximum Input Clock Frequency

Control must be Preset

Note 2: Capacitance is guaranteed by periodic testing.

tH0, tH1

tpw

t_{SM}

f_{MAX}

be Held

Note 3: CPD determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

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 $V_{CC} = 5.0 V$

 $V_{CC} = 10 V$

 $V_{CC} = 5.0 V$

 $V_{CC} = 10 V$

 $V_{CC} = 5.0 V$

 $V_{CC} = 10 V$

 $V_{CC} = 5.0 V$

25

10

200

100

3

6.5

10

50

100

50

100

50

5

10

ns

ns

ns

ns

пs

ns

MHz

MHz

рF

рF