National Semiconductor

MM54C989/MM74C989 64-Bit (16 × 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines, a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note. The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

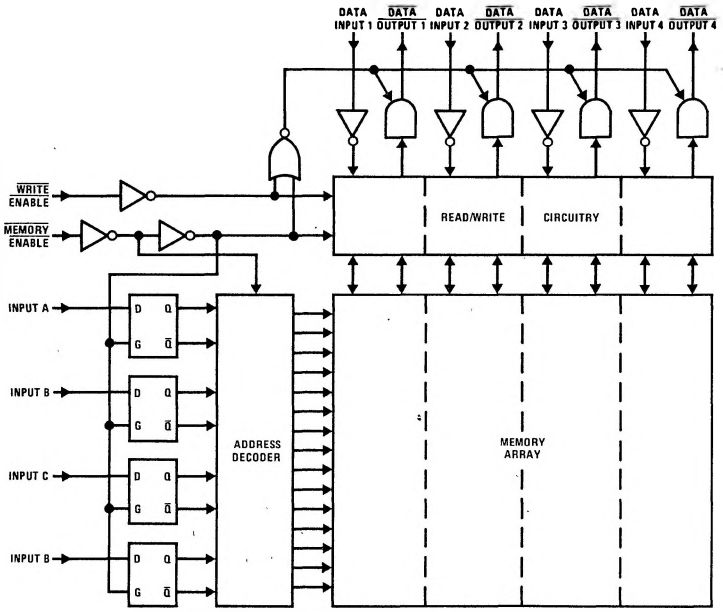
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE® (Hi-Z) condition.

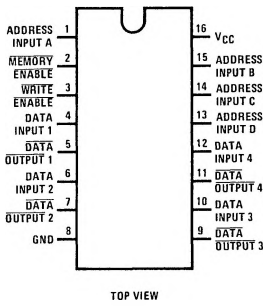
Features

- Wide supply voltage range — 3.0V to 5.5V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 250 nW/package (typ.) @ V_{CC} = 5V
- Fast access time — 140 ns (typ.) at V_{CC} = 5V
- TRI-STATE output

Logic and Connection Diagrams



Dual-in-Line Package



TOP VIEW

Order Number MM54C989J or MM74C989J
See NS Package J16A

Order Number MM74C989N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Package Dissipation	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range		3.0V to 5.5V	
Standby V_{CC} Range		1.5V to 5.5V	

DC Electrical Characteristics MM54C989/MM74C989

(Min/max limits apply across the temperature and power supply range indicated).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	2.4			V
		I_O = −150 μA	V_{CC}−0.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 360 μA			0.4	V
	Output Current in High Impedance State	V_O = 5V		0.005	1	μA
		V_O = 0	−1	−0.005		μA
I_{CC}	Supply Current (Active)	$\overline{ME}$ = 0, V_{CC} = 5V		0.05	150	μA
	Supply Current (Stand-By)	$\overline{ME}$ = 5V			3	μA

AC Electrical Characteristics MM54C989/MM74C989

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

PARAMETER		MIN	TYP	MAX	UNITS
t_{ACC}	Access Time From Address		140	500	ns
t_{PD}	Propagation Delay From $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE®, C_L = 5 pF, R_L = 10k, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

AC Electrical Characteristics (Continued)

MM54C989: $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$. $C_L = 50$ pF
MM74C989: $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.75V$ to $5.25V$. $C_L = 50$ pF

PARAMETER		MM54C989		MM74C989		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time From Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay From $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE®, (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

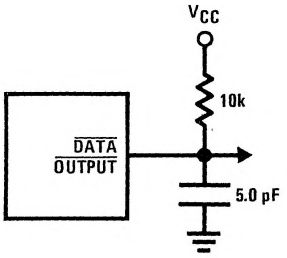
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

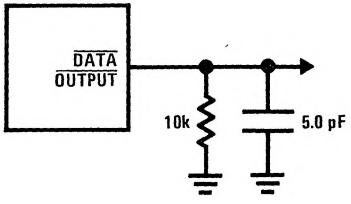
$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

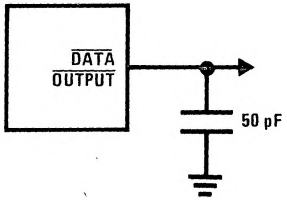
t_{0H}



t_{1H}

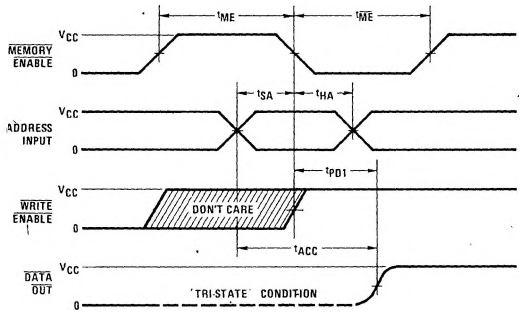


All Other AC Tests

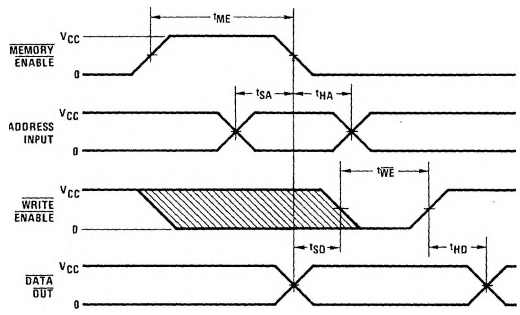


Switching Time Waveforms

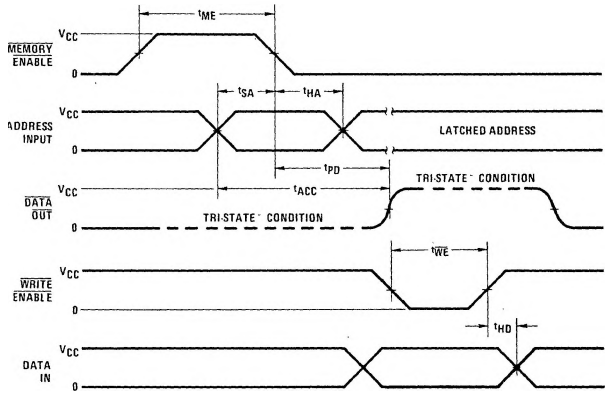
Read Cycle (Note 1)



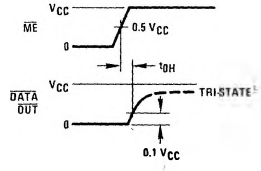
Write Cycle (Note 1)



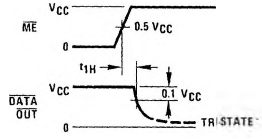
Read-Modify-Write Cycle (Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.