National Semiconductor

# MM54C73/MM74C73/MM54C76/MM74C76/MM54C107 MM74C107 Dual J-K Flip-Flops with Clear and Preset

## General Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and Q outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

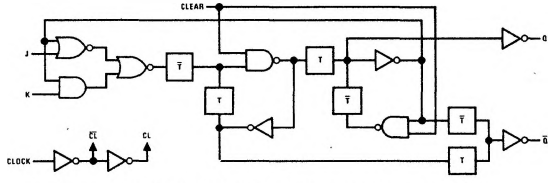
## Features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 $V_{CC}$ (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V supply

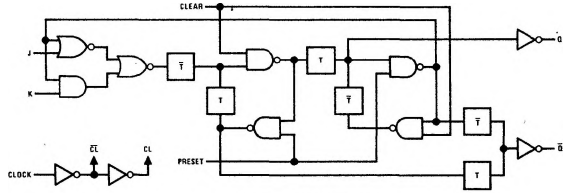
## Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

## Logic and Connection Diagrams

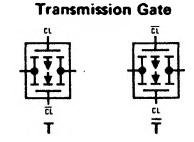


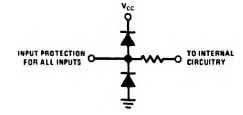

MM54C73/MM74C73 and MM54C107/MM74C107

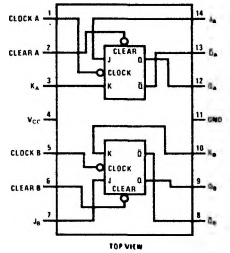



MM54C76/MM74C76

Transmission Gate

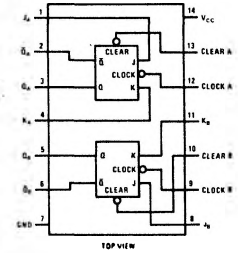


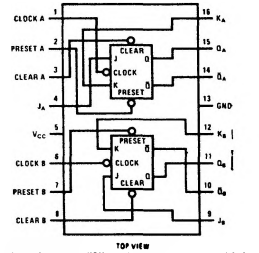

Note: A logic "0" on clear sets Q to logic "0."

MM54C73/MM74C73




Note: A logic "0" on clear sets Q to logic "0."

MM54C107/MM74C107




Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

MM54C76/MM74C76

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage at Any Pin (Note 1) | $-0.3V$ to $V_{CC} + 0.3V$ |
| Operating Temperature Range | |
| MM54CXX | $-55°C$ to $125°C$ |
| MM74CXX | $-40°C$ to $+85°C$ |
| Storage Temperature | $-65°C$ to $150°C$ |
| Package Dissipation | 500 mW |
| Lead Temperature (Soldering, 10 seconds) | 300°C |
| Operating $V_{CC}$ Range | $+3V$ to $15V$ |

## DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

| | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **CMOS to CMOS** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 3.5<br>8.0 | | | V<br>V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | | 1.5<br>2.0 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 4.5<br>9.0 | | | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | | 0.5<br>1.0 | V<br>V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15.0V$ | | | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15.0V$ | $-1.0$ | | | μA |
| $I_{CC}$ | Supply Current | $V_{CC} = 15.0V$ | | 0.050 | 60 | μA |
| | **Low Power TTL to CMOS Interface** | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C, $V_{CC} = 4.5V$<br>74C, $V_{CC} = 4.75V$ | $V_{CC} - 1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C, $V_{CC} = 4.5V$<br>74C, $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$<br>74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$<br>74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$ | | | 0.4 | V |
| | **Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)** | | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 5.0V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-1.75$ | | | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 10V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-8.0$ | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 5.0V$, $V_{IN(1)} = 5.0V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 1.75 | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 10V$, $V_{IN(1)} = 10V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 8.0 | | | mA |

## AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

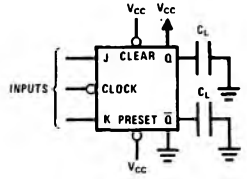
| Parameter | | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Any Input | | 5 | | pF |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 180<br>70 | 300<br>110 | ns<br>ns |
| $t_{pd0}$ | Propagation Delay Time to a Logical "0" from Preset or Clear | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 200<br>80 | 300<br>130 | ns<br>ns |
| $t_{pd}$ | Propagation Delay Time to a Logical "1" from Preset or Clear | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 200<br>80 | 300<br>130 | ns<br>ns |
| $t_S$ | Time Prior to Clock Pulse that Data must be Present | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 110<br>45 | 175<br>70 | ns<br>ns |
| $t_H$ | Time after Clock Pulse that J and K must be Held | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | −40<br>−20 | 0<br>0 | ns<br>ns |
| $t_{PW}$ | Minimum Clock Pulse Width $t_{WL} = t_{WH}$ | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 120<br>50 | 190<br>80 | ns<br>ns |
| $t_{PW}$ | Minimum Preset and Clear Pulse Width | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 90<br>40 | 130<br>60 | ns<br>ns |
| $f_{MAX}$ | Maximum Toggle Frequency | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | 2.5<br>7.0 | 4.0<br>11.0 | | MHz<br>MHz |
| $t_r$, $t_f$ | Clock Pulse Rise and Fall Time | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | | 15<br>5 | μs<br>μs |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

## AC Test Circuit




## Truth Table

| $t_n$ | | $t_{n+1}$ |
|---|---|---|
| J | K | Q |
| 0 | 0 | $Q_n$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q}_n$ |

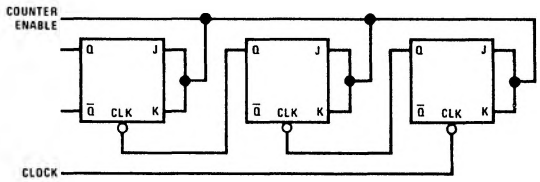
$t_n$ = bit time before clock pulse.
$t_{n+1}$ = bit time after clock pulse.

| Preset | Clear | $Q_n$ | $\overline{Q}_n$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | *$Q_n$ | *$\overline{Q}_n$ |

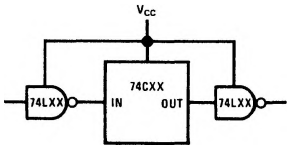
*No change in output from previous state.

# Typical Applications

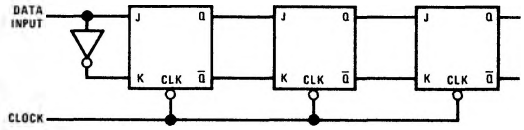
**Ripple Binary Counters**



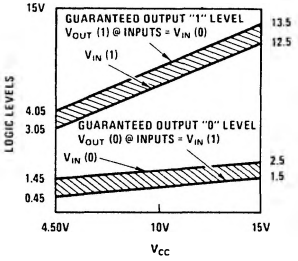

**74C Compatibility**




**Shift Registers**

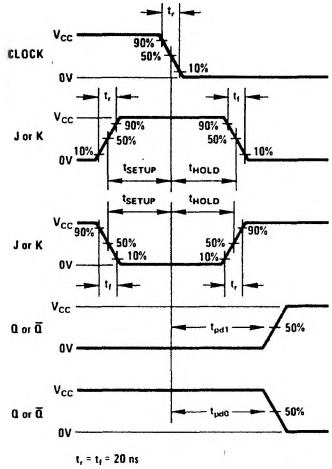



**Guaranteed Noise Margin as a Function of $V_{CC}$**




# Switching Time Waveforms

**CMOS to CMOS**




$t_r = t_f = 20$ ns