National Semiconductor

MM54C48/MM74C48 BCD-to-7 Segment Decoder

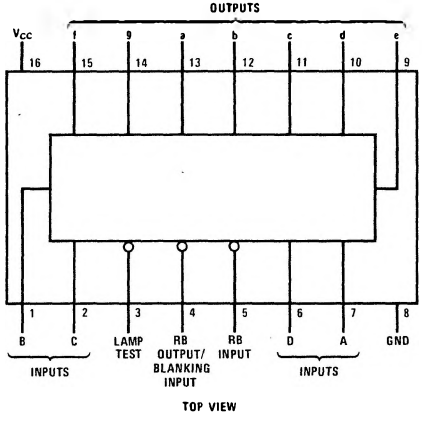
General Description

The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

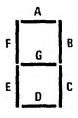
Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

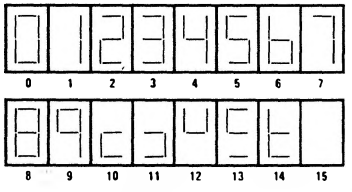
Connection Diagram



TOP VIEW



Segment Identification



Numerical Designations and Resultant Displays

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C48	$-55°C$ to $+125°C$
MM74C48	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" input Current	$V_{CC}=15.0V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	54C, $V_{CC}=4.5V$, $I_O=-50\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-50\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE}	Output Source Current (P-Channel) (RB Output Only)	$V_{CC}=4.75V$, $V_{OUT}=0.4V$ $V_{CC}=10V$, $V_{OUT}=0.5V$			-0.80 -4.0	mA mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA
	Output Source Current (NPN Bipolar)	$V_{CC}=5.0V$, $V_{OUT}=3.4$ $V_{CC}=5.0V$, $V_{OUT}=3.0$ $V_{CC}=10V$, $V_{OUT}=8.4$ $V_{CC}=10V$, $V_{OUT}=8.0$	-20 -20 	-50 -65 -50 -65		mA mA mA mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

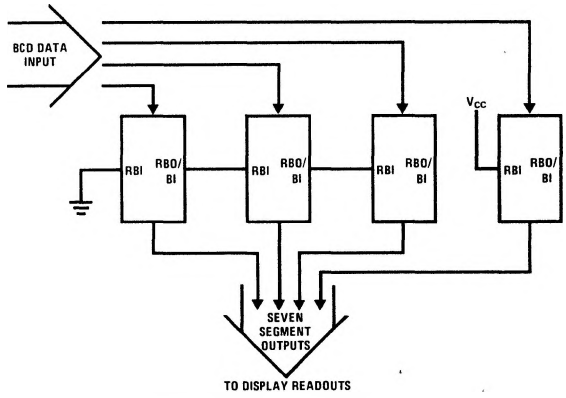
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		500 180	1600 550	ns ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		350 140	1200 450	ns ns
t_{pd1}	Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	1500 500	ns ns
t_{pd1}	Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		600 250	2000 800	ns ns
t_{pd0}	Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$ $V_{CC} = 10V$		140 50	450 150	ns ns

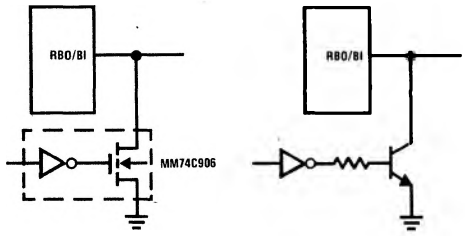
Typical Applications

Typical Connection Utilizing the Ripple-Blanking Feature



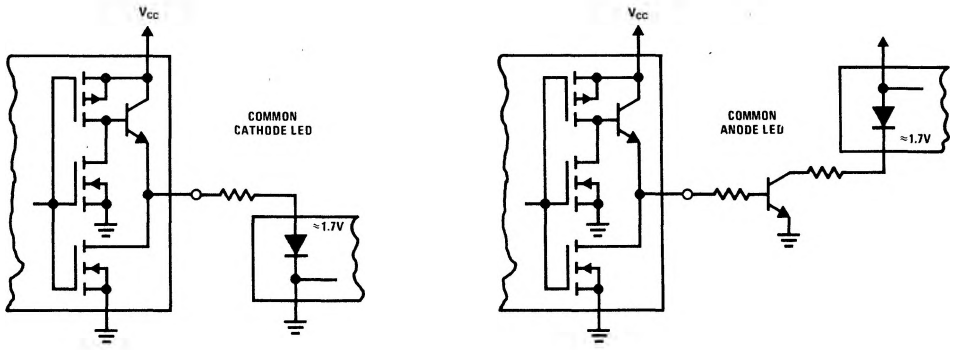
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

Blanking Input Connection Diagram



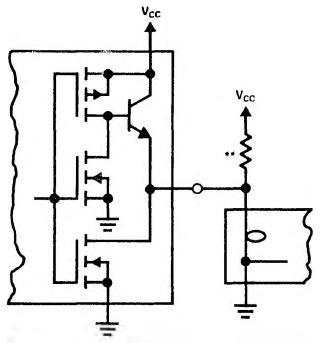
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout



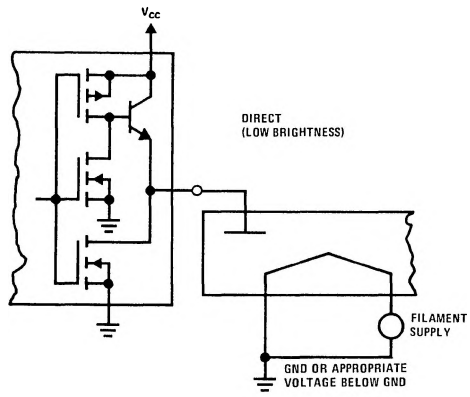
Typical Applications (Cont'd)

Incandescent Readout

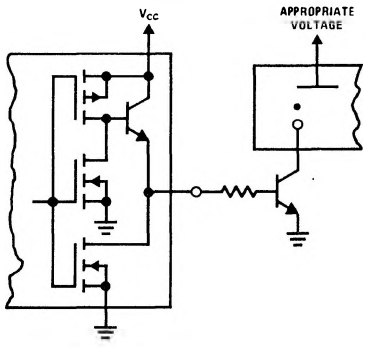


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

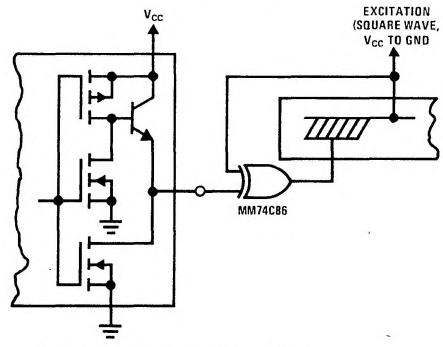
Fluorescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

Truth Table

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

† One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).