National Semiconductor

MM54C906/MM74C906 Hex Open Drain N-Channel Buffers
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers

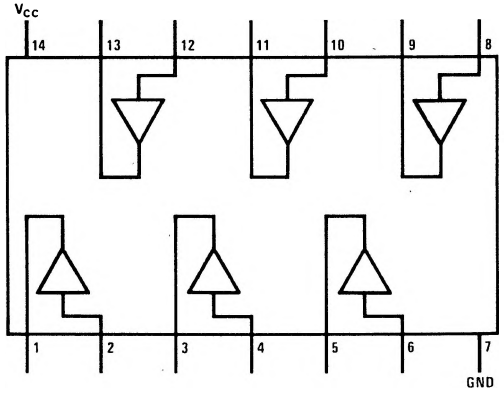
General Description

These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

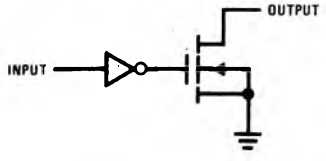
Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} (typ.)
- High current sourcing and sinking open drain outputs

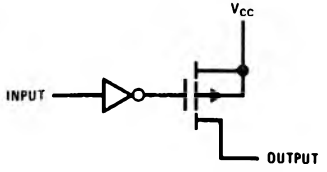
Connection Diagram



Logic Diagrams



MM54C906/MM74C906



MM54C907/MM74C907

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	$-0.3V$ to $V_{CC}+0.3V$
Voltage at any Output Pin	
MM54C906/MM74C906	$-0.3V$ to $+18V$
MM54C907/MM74C907	$V_{CC}-18$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C906/MM54C907	$-55°C$ to $+125°C$
MM74C906/MM74C907	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, Output Open		0.05	15	μA
	Output Leakage					
	MM54C906	$V_{CC}=4.5V$, $V_{IN}=V_{CC}-1.5$ $V_{CC}=4.5V$, $V_{OUT}=18V$		0.005	5	μA
	MM74C906	$V_{CC}=4.75V$, $V_{IN}=V_{CC}-1.5$ $V_{CC}=4.75V$, $V_{OUT}=18V$		0.005	5	μA
	MM54C907	$V_{CC}=4.5V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-18V$		0.005	5	μA
	MM74C907	$V_{CC}=4.75V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-18V$		0.005	5	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
	Output Drive Current					
	MM54C906	$V_{CC}=4.5V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.5V$, $V_{OUT}=0.5V$ $V_{CC}=4.5V$, $V_{OUT}=1.0V$	 2.1 4.2	 8.0 12		 mA mA
	MM74C906	$V_{CC}=4.75V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.75V$, $V_{OUT}=0.5V$ $V_{CC}=4.75V$, $V_{OUT}=1.0V$	 2.1 4.2	 8.0 12		 mA mA
	MM74C907	$V_{CC}=4.5V$, $V_{IN}=V_{CC}-1.5V$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-0.5V$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-1.0V$	 −1.05 −2.1	 −1.5 −3.0		 mA mA
	MM74C907	$V_{CC}=4.75V$, $V_{IN}=V_{CC}-1.5V$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-0.5V$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-1.0V$	 −1.05 −2.1	 −1.5 −3.0		 mA mA
	MM54C906/MM74C906	$V_{CC}=10V$, $V_{IN}=2.0V$ $V_{CC}=10V$, $V_{OUT}=0.5V$ $V_{CC}=10V$, $V_{OUT}=1.0V$	 4.2 8.4	 −20 −30		 mA mA
	MM54C907/MM74C907	$V_{CC}=10V$, $V_{IN}=8.0V$ $V_{CC}=10V$, $V_{OUT}=9.5V$ $V_{CC}=10V$, $V_{OUT}=9.0V$	 −2.1 −4.2	 −4.0 −8.0		 mA mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
C_{IN}	Input Capacity	(Note 2)		5.0		pF
C_{OUT}	Output Capacity	(Note 2)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

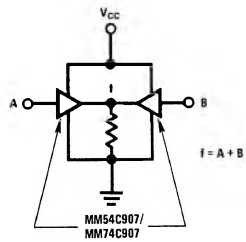
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capactiy (C_{OUT}).

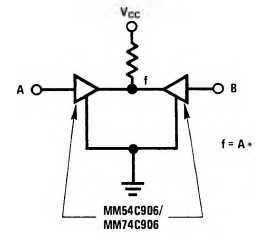
Typical Applications

Wire OR Gate



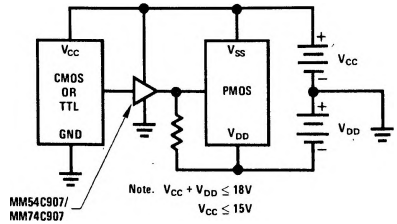
Note: Can be extended to more than 2 inputs.

Wire AND Gate



Note: Can be extended to more than 2 inputs.

CMOS or TTL to PMOS Interface



CMOS or TTL to CMOS at a Higher V_{CC}