National Semiconductor

MM74C912 6-Digit BCD Display Controller/Driver
MM74C917 6-Digit Hex Display Controller/Driver

General Description

The MM74C912, MM74C917 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, $\overline{CE}$, and WRITE ENABLE, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, $\overline{OSE}$, which is tied low in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives a LED display through high drive (100 mA typ) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format. The MM74C917 converts binary data into hex format.

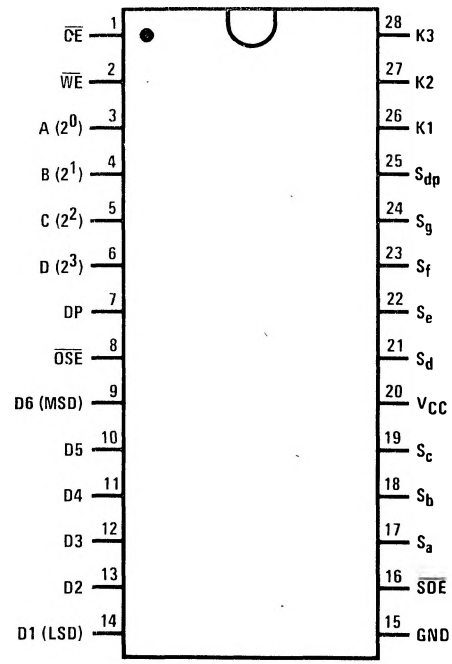
All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ) TRI-STATEABLE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ)
- Internal segment decoder
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS			$\overline{WE}$	OPERATION
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = don't care

Output Control

$\overline{SOE}$	$\overline{OSE}$	OPERATION
0	0	Refresh Display
0	1	Stop Oscillator*
1	0	Disable Segment Outputs
1	1	Standby Mode

*Segment drive may exceed maximum display dissipation.

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	Refer to $P_{D\ MAX}$ vs T_A Graph
Voltage at Any Input	$-0.3V$ to $+15V$	Operating V_{CC} Range	3V to 6V
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	$300°C$

DC Electrical Characteristics Min/max limits apply at $40°C \leq T_J \leq 85°C$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$, Outputs Open		0.5	2	mA
I_{OUT}	TRI-STATE Output Current	$V_{CC} = 5V$, $V_O = 5V$		0.03	10	μA
		$V_{CC} = 5V$, $V_O = 0V$	-10	-0.03		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC}-2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$,				mA
		$T_J = 25°C$	-60	-100		
		$T_J = 100°C$	-40	-60		mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 1V$,				
		$T_J = 25°C$	-10	-20		mA
		$T_J = 100°C$	-7	-15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	$V_{CC} = 5V$, $I_O = -360\ \mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Output	$V_{CC} = 5V$, $I_O = 360\ \mu A$			0.4	V
Θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages reference to ground.

Note 3: Θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

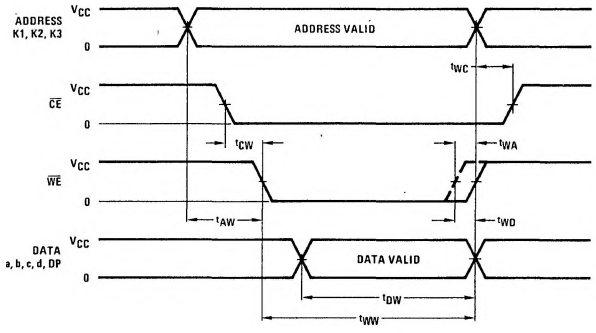
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable	$T_J = 25°C$	35	15		ns
	Setup Time	$T_J = 125°C$	50	20		ns
t_{AW}	Address to Write Enable	$T_J = 25°C$	35	15		ns
	Setup Time	$T_J = 125°C$	50	20		ns
t_{WW}	Write Enable Width	$T_J = 25°C$	400	225		ns
		$T_J = 125°C$	450	250		ns

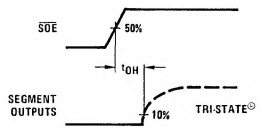
AC Electrical Characteristics (Continued) V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

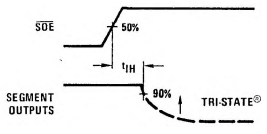
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DW}	Data to Write Enable Setup Time	T_J = 25°C	390	225		ns
		T_J = 125°C	430	250		ns
t_{WD}	Write Enable to Data Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WC}	Write Enable to Chip Enable	T_J = 25°C	50	30		ns
	Hold Time	T_J = 125°C	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels	R_L = 10k, T_J = 25°C		275	500	ns
	Into TRI-STATE	C_L = 10 pF, T_J = 125°C		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" to	R_L = 10k, T_J = 25°C		325	600	ns
	Logical "0" Level	C_L = 50 pF, T_J = 125°C		375	700	ns
t_{IB}	Interdigit Blanking Time	T_J = 25°C	5	10		μs
		T_J = 125°C	10	20		μs
f_{MUX}	Multiplex Scan Frequency	T_J = 25°C		350		Hz
		T_J = 125°C		250		Hz
C_{IN}	Input Capacitance	Note 4		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Note 4		30	50	pF

Note 4: Capacitance is guranteed by periodic testing.

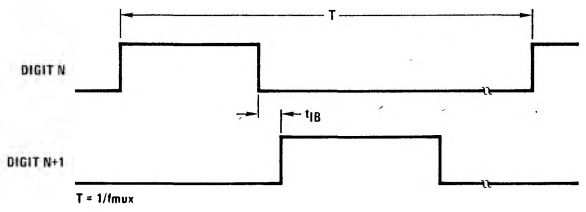
Switching Time Waveforms







Multiplexing Output Waveforms



Functional Description

Character Font

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	a	o	r	-	_		.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

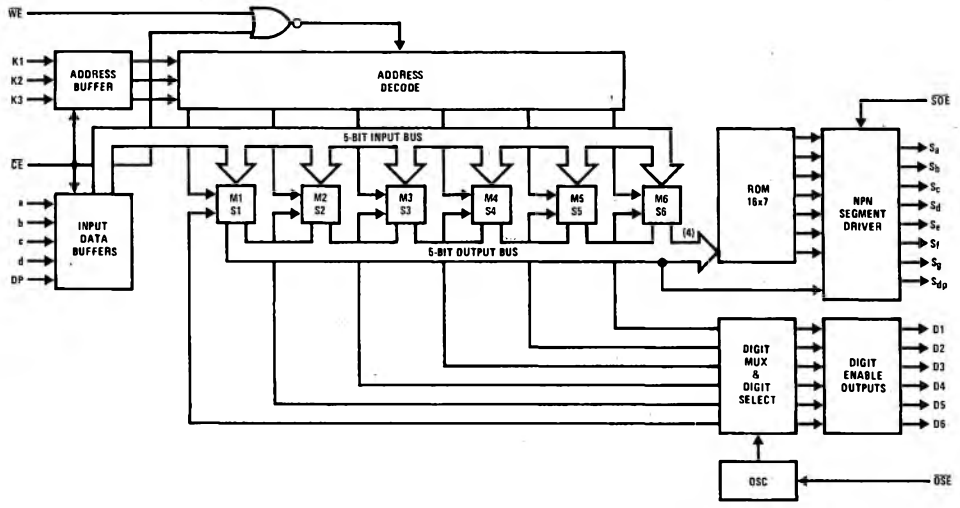
Segment Identification

The MM74C912, MM74C917 display controllers are manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

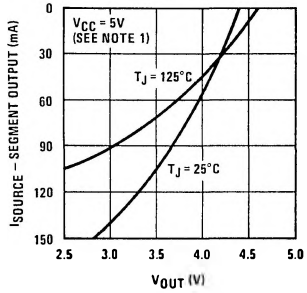
As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an overburdened microprocessor.

Block Diagram

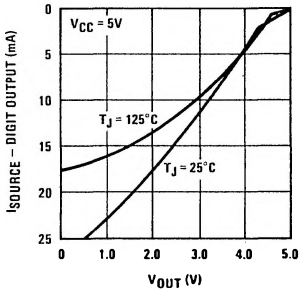


Typical Performance Characteristics

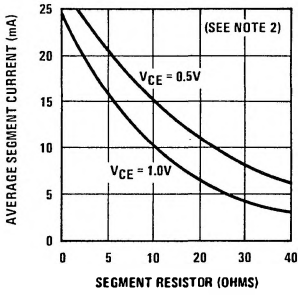
I_{SH} vs V_{OUT}



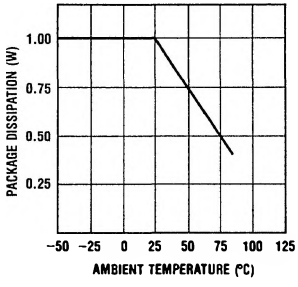
I_{DH} vs V_{OUT}



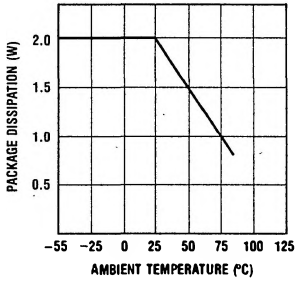
I_{AVG} vs R_{LIM}



Power Dissipation vs. Temperature for Plastic Packages



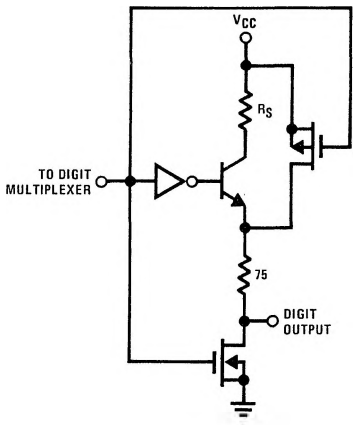
Power Dissipation vs. Temperature for Ceramic Packages



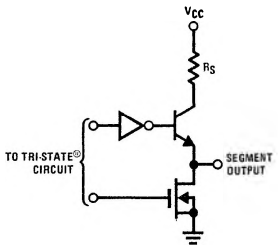
Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

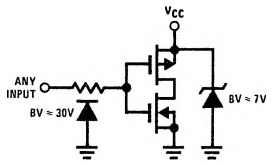
Digit Output Structure



Segment Output Structure



Input Protection



Typical Applications