

MM54C90/MM74C90 4-Bit Decade Counter MM54C93/MM74C93 4-Bit Binary Counter

General Description

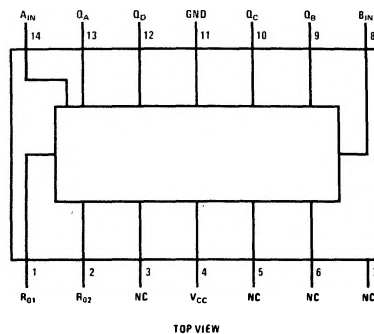
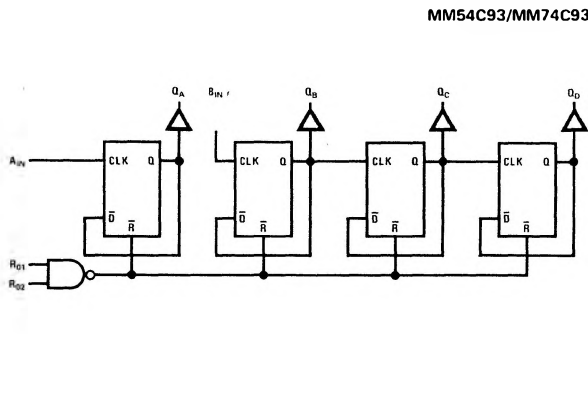
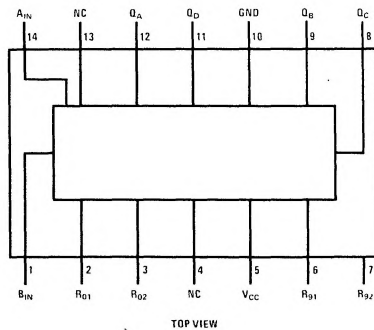
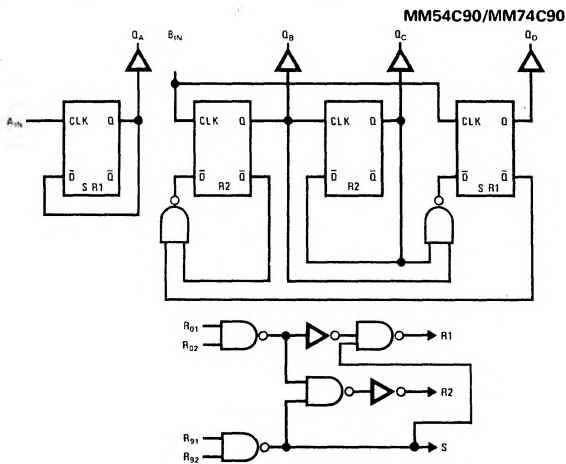
The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the R_{01} , R_{02} , R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02} , and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

Features

- Wide supply voltage range 3V to 15V
- Guaranteed noise margin 1V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power fan out of 2
TTL compatibility driving 74L
- The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout

Logic and Connection Diagrams



Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	-0.3V to $V_{CC} + 0.3V$	Operating V_{CC} Range	3V to 15V
Operating Temperature Range		Absolute Maximum V_{CC}	18V
MM54C90, MM54C93	-55°C to +125°C	Storage Temperature Range	-65°C to +150°C
MM74C90, MM74C93	-40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

DC Electrical Characteristics

Min./max. limits apply across temperature range unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS					
$V_{IN(1)}$ Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8			V V
$V_{IN(0)}$ Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2	V V
$V_{OUT(1)}$ Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10\mu A$ $V_{CC} = 10V, I_O = -10\mu A$	4.5 9			V V
$V_{OUT(0)}$ Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10\mu A$ $V_{CC} = 10V, I_O = +10\mu A$			0.5 1	V V
$I_{IN(1)}$ Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$ Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1	-0.005		μA
I_{CC} Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL Interface					
$V_{IN(1)}$ Logical "1" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	$V_{CC} = 4.5V$ $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$ Logical "0" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	$V_{CC} = 4.5V$ $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$ Logical "1" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	$V_{CC} = 4.5V, I_O = -360\mu A$ $V_{CC} = 4.75V, I_O = -360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$ Logical "0" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	$V_{CC} = 4.5V, I_O = 360\mu A$ $V_{CC} = 4.75V, I_O = 360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)					
I_{SOURCE} Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75	-3.3		mA
I_{SOURCE} Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8	-15		mA
I_{SINK} Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75	3.6		mA
I_{SINK} Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8	16		mA

AC Electrical Characteristics

 $T_A = 25^\circ C, C_L = 50 pF$, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1} Propagation Delay Time from A_{IN} to Q_A	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 150	ns ns
t_{pd0}, t_{pd1} Propagation Delay Time from A_{IN} to Q_B (MM54C93/MM74C93)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	850 300	ns ns
t_{pd0}, t_{pd1} Propagation Delay Time from A_{IN} to Q_B (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	800 300	ns ns

AC Electrical Characteristics (Cont'd.) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified.

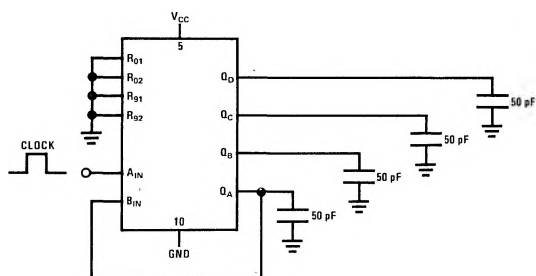
Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C93/MM74C93)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	500 200	1050 400	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	500 200	1000 400	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	600 250	1200 500	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	450 160	800 300	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	150 75	300 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	200 75	400 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{g1} or R_{g2} to Q_A or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	250 100	500 200	ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C93/MM74C93)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	600 300	250 125	ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	600 300	250 125	ns ns
t_{PW}	Min. R_{g1} or R_{g2} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	500 250	200 100	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 10\text{V}$ $V_{CC} = 10\text{V}$		15 5	μs μs
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	250 100	100 50	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$	2 5		MHz MHz
C_{IN}	Input Capacitance	Any Input (Note 2)		5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		45	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

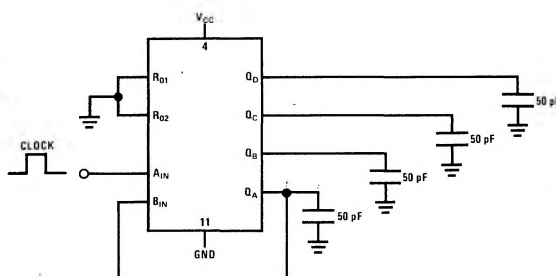
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Test Circuits



Clock rise and fall time $t_r = t_f = 20\text{ ns}$

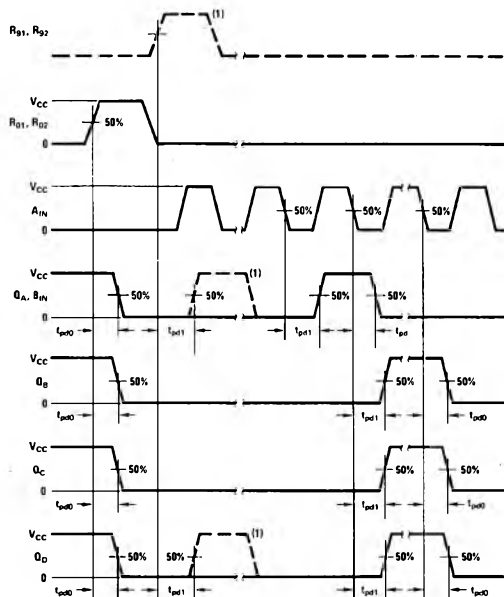
MM54C90/MM74C90



Clock rise and fall time $t_r = t_f = 20\text{ ns}$

MM54C93/MM74C93

Switching Time Waveforms



Truth Tables

MM54C90/MM74C90 4-Bit Decade Counter
BCD Count Sequence

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R ₀₁	R ₀₂	R ₉₁	R ₉₂	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

MM54C93/MM74C93 4-Bit Binary Counter
Binary Count Sequence

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R ₀₁	R ₀₂	Q _D	Q _C	Q _B	Q _A		
H	H	L	L	L	L		
L	X	COUNT					
X	L	COUNT					