

MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

General Description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

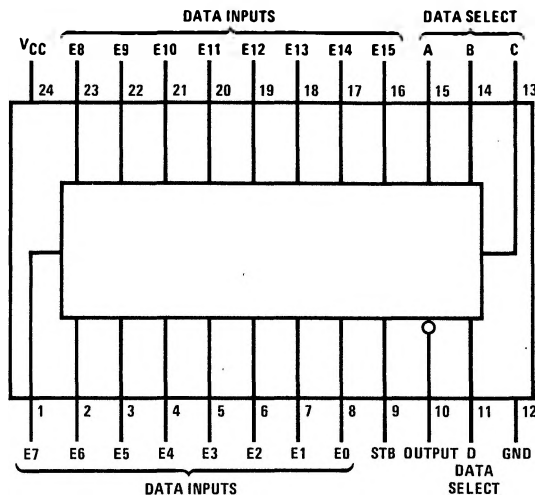
A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range 3.0 V to 15 V
- Guaranteed noise margin 1.0 V
- High noise immunity $0.45 V_{CC}$ (typ.)
- TTL compatibility Drive 1 TTL Load

Connection Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC}+0.3$ V
Operating Temperature Range	
MM54C150, MM72C19	-55°C to +125°C
MM74C150, MM82C19	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$ V, $I_O = -10 \mu A$ $V_{CC} = 10$ V, $I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$ V, $I_O = +10 \mu A$ $V_{CC} = 10$ V, $I_O = +10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$ V, $V_{IN} = 15$ V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15$ V, $V_{IN} = 0$ V	-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State MM73C19/MM82C19	$V_{CC} = 15$ V, $V_O = 15$ V $V_{CC} = 15$ V, $V_O = 0$ V		0.005 -0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15$ V	-1.0	0.05	300	μA
TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, 72C $V_{CC} = 4.5$ V 74C, 82C $V_{CC} = 4.75$ V	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, 72C $V_{CC} = 4.5$ V 74C, 82C $V_{CC} = 4.75$ V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, 72C $V_{CC} = 4.5$ V, $I_O = -1.6$ mA 74C, 82C $V_{CC} = 4.75$ V, $I_O = -1.6$ mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, 72C $V_{CC} = 4.5$ V, $I_O = 1.6$ mA 74C, 82C $V_{CC} = 4.75$ V, $I_O = 1.6$ mA			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0$ V, $V_{OUT} = 0$ V, $T_A = 25^\circ C$	-4.35	-8		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10$ V, $V_{OUT} = 0$ V, $T_A = 25^\circ C$	-20	-40		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0$ V, $V_{OUT} = V_{CC}$, $T_A = 25^\circ C$	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10$ V, $V_{OUT} = V_{CC}$, $T_A = 25^\circ C$	20	40		mA

AC Electrical Characteristics $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0} , t_{pd1} Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0\text{ V}$		250	600	ns
	$V_{CC} = 10\text{ V}$		110	300	ns
	$V_{CC} = 5.0\text{ V}$, $C_L = 150\text{ pF}$		290	650	ns
	$V_{CC} = 10\text{ V}$, $C_L = 150\text{ pF}$		120	330	ns
t_{pd0} , t_{pd1} Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0\text{ V}$		290	650	ns
	$V_{CC} = 10\text{ V}$		120	330	ns
t_{pd0} , t_{pd1} Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM54C150/MM74C150	$V_{CC} = 5.0\text{ V}$		120	300	ns
	$V_{CC} = 10\text{ V}$		55	150	ns
t_{1H} , t_{0H} Delay from Strobe to High Impedance State MM72C19/MM82C19	$V_{CC} = 5.0\text{ V}$, $R_L = 10\text{ k}$, $C_L = 5\text{ pF}$		80	200	ns
	$V_{CC} = 10\text{ V}$, $R_L = 10\text{ k}$, $C_L = 5\text{ pF}$		60	150	ns
t_{H1} , t_{H0} Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM72C19/MM82C19	$V_{CC} = 5.0\text{ V}$, $R_L = 10\text{ k}$, $C_L = 5\text{ pF}$		80	250	ns
	$V_{CC} = 10\text{ V}$, $R_L = 10\text{ k}$, $C_L = 5\text{ pF}$		30	120	ns
C_{IN} Input Capacitance	Any Input, (Note 2)		5.0		pF
C_{OUT} Output Capacitance MM72C19/MM82C19	(Note 2)		11.0		pF
C_{PD} Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Truth Table

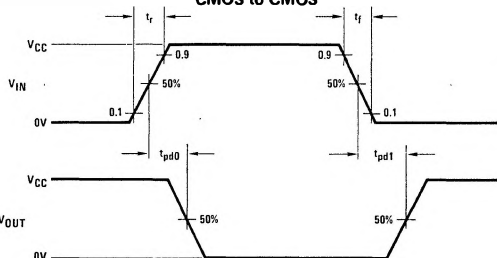
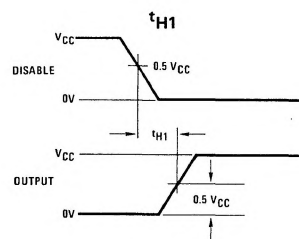
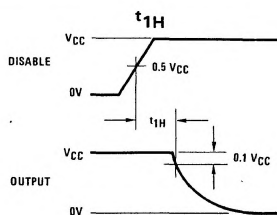
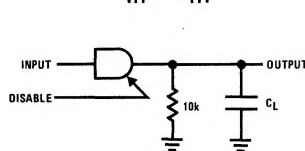
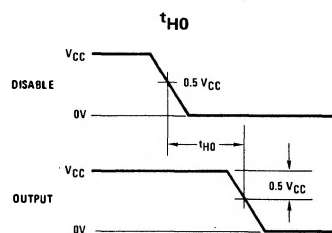
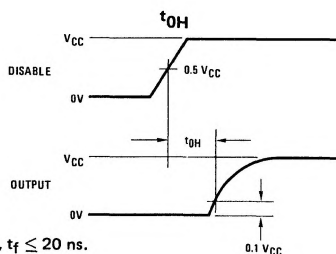
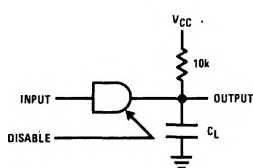
MM54C150/MM74C150

INPUTS																					OUTPUT
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1*
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
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0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
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1	0	0	1	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
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1	0	1	0	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

Switching Time Waveforms

CMOS to CMOS

 t_{1H} and t_{H1}  t_{0H} and t_{H0} 

Note: Delays measured with input $t_r, t_f \leq 20$ ns.

The diagram illustrates a 16-bit parallel adder implemented using 74181 ALUs and 74180 majority gates. The circuit consists of the following components and connections:

- Inputs:** Two 16-bit numbers, E1 and E2, are provided as inputs to the ALUs. A STROBE input is also present.
- 74181 ALUs:** There are four 74181 ALUs arranged in a row. Each ALU has 16 data inputs (E0-E15), a STROBE input, and a carry input. The carry inputs are connected in a chain: the carry input of the first ALU is connected to the carry output of the last ALU, and so on.
- 74180 Majority Gates:** There are four 74180 majority gates, each with three inputs and one output. The outputs of the ALUs are connected to the inputs of the majority gates. The majority gates are used to generate the carry signals for the next stage of the adder.
- Output:** The final output of the adder is the sum of the two input numbers, E1 and E2, which is connected to the output of the majority gates.