

□ MN1021617

Type	MN1021617	
ROM (x8-bit)	128 K	
RAM (x8-bit)	4 K	
Package	LQFP128-P-1818C *Lead-free, FLGA165-C-1111 *Lead-free	
Minimum Instruction Execution Time	With main clock operated	50 ns (at 3.0 V to 3.6 V, 40 MHz)
		100 ns (at 2.0 V to 3.6 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RST pin • Watchdog • NMI pin • Timer counter 4 to 15 • Timer counter 16, 17, 21 • Timer counter 16 to 20 compare capture A • Timer counter 16 to 20 compare capture B • Timer counter 21 capture A • Timer counter 21 capture B • Timer counter 21 capture D • Timer counter 21 compare E • Timer counter 21 compare F • ATC ch.0 to 3 transfer finish • External 0 to 7 • Serial ch.0 to 3 transmission • Serial ch.0 to 3 reception • \overline{KI} pin (OR) • A/D conversion finish 	
Timer Counter	Timer counter 0 : 8-bit × 1 (prescalers)	
		Clock source 1/2 of system clock frequency; timer counter 1 output
	Timer counter 1 : 8-bit × 1 (prescalers)	
		Clock source 1/2 of system clock frequency; timer counter 0 output
	Timer counter 2 : 8-bit × 1 (UART baud rate generator)	
		Clock source 1/2 of system clock frequency; timer counter 0 output
	Timer counter 3 : 8-bit × 1 (UART baud rate generator)	
		Clock source 1/2 of system clock frequency; timer counter 0 output; external clock input
	Timer counter 4 : 8-bit × 1 (timer output, A/D conversion start up)	
		Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output
		Interrupt source underflow of timer counter 4
	Timer counter 5, 9 : 8-bit × 1 (UART baud rate generator)	
		Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output
		Interrupt source underflow of timer counter 5, 9
Timer counter 6, 10, 11 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output	
	Interrupt source underflow of timer counter 6, 10, 11	
Timer counter 7 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output	
	Interrupt source underflow of timer counter 7	
Timer counter 8 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output;	
	timer counter 1 output	
	Interrupt source underflow of timer counter 8	
Timer counter 12 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0	
	output; timer counter 1 output	
	Interrupt source underflow of timer counter 12	
Timer counter 13 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; timer counter 0 output; timer counter 1 output	
	Interrupt source underflow of timer counter 13	
Timer counter 14 : 8-bit × 1 (timer output)		
	Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0	
	output	
	Interrupt source underflow of timer counter 14	

Timer Counter (Continue)	Timer counter 15 : 8-bit × 1 (timer output) Clock source 1/2 of system clock frequency; external clock input with edge; timer counter 0 output Interrupt source underflow of timer counter 15
	Connectable timer counter 0 to 3, 4 to 7, 8 to 11, 12 to 15
	Timer counter 16, 17 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input (with edge, timer counter 17 only); timer counter 0 output; timer counter 1 output (timer counter 16 only) Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 16, 17
	Timer counter 18 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock frequency; external clock input; timer counter 0 output; timer counter 1 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 18, 19, 20
	Timer counter 19, 20 : 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source 1/2 of system clock; timer counter 0 output; timer counter 1 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 18, 19, 20
	Timer counter 21 : 24-bit × 1 (servo control) Clock source 1/2 of system clock frequency; timer counter 1 output Interrupt source when capturing to capture A; when capturing to capture B; when capturing to capture D; when coinciding to compare E; when coinciding to compare F

Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 2 frequency; 1/8, 1/2 of timer counter 5 frequency; external clock
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source 1/8 of timer counter 3 frequency; 1/8, 1/2 of timer counter 9 frequency; external clock
	UART × 4 (common use with serial 0 to 3)
	I ² C × 2 (common use with serial 1, 3; single master)

I/O Pins	I/O	100	• Common use : 56 (address data separate 8-bit mode) • Common use : 73 (address data multiplex 8-bit Mode)
	Input	8	• Common use : 8

A/D Inputs	10-bit × 12-ch. (maximum input is 16) (with S/H)
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PWM	16-bit × 5-ch. (timer counter 16 to 20)
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ICR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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OCR	16-bit × 5-ch., 24-bit × 1-ch. (timer counter 16 to 21)
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Notes	Address / data multiplex bus Interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable
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See the next page for electrical characteristics, pin assignment and support tool.

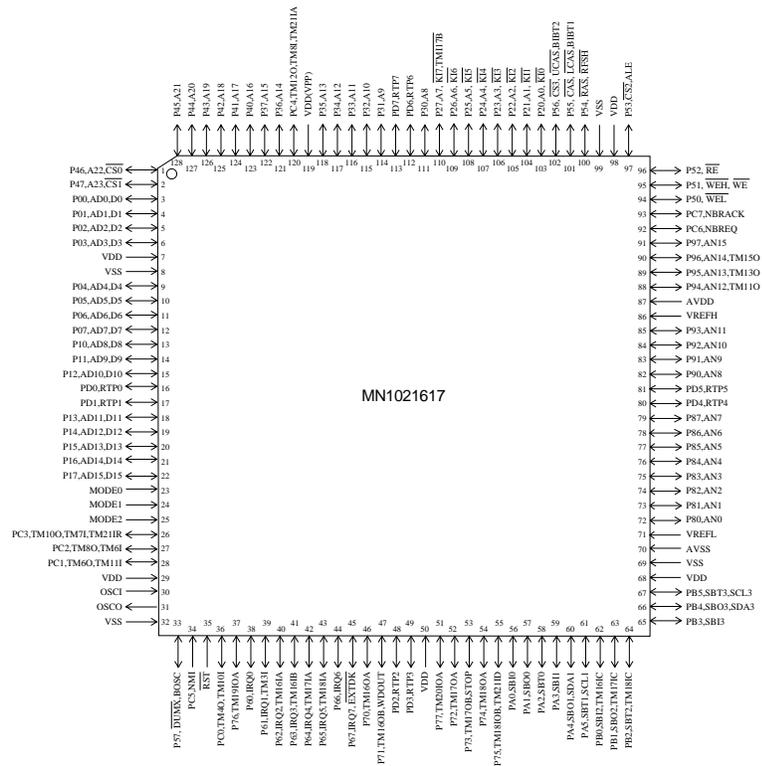
Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 40 MHz, VDD = 3.3 V			50	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open all other input pins and Hi-Z state input/output			50	μA
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level f = 40 MHz, VDD = 3.3 V, output open			25	mA

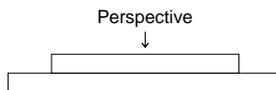
(Ta = -20°C to +70°C, VDD = AVDD = 3.3 V, VSS = AVSS = 0 V)

Pin Assignment



LQFP128-P-1818C *Lead-free

Pin Assignment (Continue)



N.D.	N.D.	PB5.SBT3, SCL3	AVDD	P81.AN1	P83.AN3	P87.AN7	AVDD	P94.AN12, TM110	AVDD	P50./WEL	N.D.	N.D.	N
N.D.	N.D.	PB3.SBI3	VSS	VREFL	P85.AN5	PD5.RTP5	P93.AN11	P96.AN14, TM150	PC6.NBREQ	P52./RE	N.D.	N.D.	M
VSS	PB2.SBT2, TM181C	PB1.SBO2, TM171C	PB4.SBO3, SDA3	P80.AN0	P84.AN4	AVSS	P91.AN9	P95.AN13, TM130	PC7.NBRACK	P51./WEH, /WE	VDD	P54./RAS, /RFSH	L
PB0.SBI2, TM161C	PA4.SBO1, SDA1	PA5.SBT1, SCL1	VDD	AVSS	P86.AN6	P90.AN8	P92.AN10	P97.AN15	VSS	P53./CS2, ALE	P56./CS3, /UCAS, BIBT2	VDD	K
PA1.SBO0	PA3.SB11	PA0.SB10	PA2.SBT0	AVSS	P82.AN2	PD4.RTP4	VREFH	P55./CAS, /LCAS, BIBT1	VPP	P20.A0./K10	P21.A1./K11	P23.A3./K13	J
P75, TM181OB, TM21HD	P73, TM170B, STOP	P77, TM201OA	P72, TM170A	P74, TM180A	N.D.	N.D.	N.D.	P22.A2./K12	P26.A6./K16	P24.A4./K14	P27.A7./K17, TM117B	P25.A5./K15	H
P71, TM160B, WDOU	PD3.RTP3	VDD	VDD	PD2.RTP2	N.D.	N.D.	N.D.	P30.A8	PD7.RTP7	VPP	P31.A9	PD6.RTP6	G
P65.IRQ5, TM181A	P67.IRQ7, EX, TDK	P66.IRQ6	P70, TM160A	P64.IRQ4, TM171A	N.D.	N.D.	N.D.	P34.A12	P32.A10	P33.A11	P35.A13	PC4, TM120, TM81, TM211A	F
P63.IRQ3, TM161B	P61.IRQ1, TM31	P62.IRQ2, TM161A	VDD	P60.IRQ0	MODE0	PD0.RTP0	P05.AD5, D5	P03.AD3, D3	P36.A14	VPP	P41.A17	P37.A15	E
VSS	P76, TM191OA	PC0, TM40, TM101	VDD	PC2, TM80, TM61	P15.AD13, D13	P13.AD11, D11	P11.AD9, D9	VSS	P01.AD1, D1	P42.A18	P40.A16	VDD	D
/RST	P57./DUMX, BOSC	PC5.NMI	OSCO	MODE2	P14.AD12, D12	VSS	P07.AD7, D7	VSS	P47.A23, /CS1	P44.A20	P45.A21	P43.A19	C
N.D.	N.D.	VSS	PC1, TM60, TM111	PC3, TM100, TM71, TM211R	P16.AD14, D14	PD1.RTP1	P10.AD8, D8	VDD	P02.AD2, D2	P46.A22, /CS0	N.D.	N.D.	B
N.D.	N.D.	OSCI	VSS	MODE1	P17.AD15, D15	P12.AD10, D10	P06.AD6, D6	P04.AD4, D4	VDD	P00.AD0, D0	N.D.	N.D.	A

FLGA165-C-1111 *Lead-free

The MN102F1617 is manufactured and sold under license agreement with BULL CP8 Inc. Note that MN102F1617 cannot be used as the IC card.

* A1 has no electrode (pin).

* N.D. (not defined) has an electrode (pin) but not guaranteed for N.C. (not connected). Pay sufficient attention so as not to cause shorting with any other wiring on the user board.

* VPP, VDD, VSS, AVDD and AVSS has multiple electrodes (pins). Electrodes having the same name are shorted internally.

Support Tool

In-circuit Emulator	PX-ICE102H1617-LQFP128-P-1818C	Not applicable to FLGA165-C-1111.
	Minimum instruction execution time	57.1 ns (at 35 MHz)
Flash Memory Built-in Type	Type	MN102F1617
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	62.5 ns (at 3.0 V to 3.6 V, 32 MHz)
		83.3 ns (at 2.7 V to 3.6 V, 24 MHz)
	Package	LQFP128-P-1818C *Lead-free, FLGA165-C-1111 *Lead-free

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