MN1959041

Commercial MPEG-4 Video Codec IC for W-CDMA Mobile Visual Terminals

■ Overview

MN1959041 is an image-processing DSP that adopts a vector pipelined architecture. It provides an extensive set of features that allow it to implement the high-efficiency image and video encoding and decoding required for image communication, recording, and playback. It implements encoding and decoding that conform to the H.263 and MPEG-4 Simple@L1 video encoding standards, and decoding that conforms to the MPEG-4 Simple@L3 video encoding standard. It includes dedicated special-purpose circuits for high-speed decoding of the MPEG-4 core profile.

■ Features

- General-purpose DSP core (MP: Main Processor) that can implement complex processing flexibly
  - Provides an instruction set of 43 instructions, including both scalar and vector instructions.
  - Provides interrupt control and task management functions that issue VCE/VIF/MIF (described later) start/stop instructions and DMA transfer instructions.
- Special-purpose arithmetic circuit (VCE: Video Codec Engine) that implements a high-speed video codec
  - Integer precision and half-pel precision motion detection circuit (MEF/MEH)
  - Discrete cosine transformation/inverse discrete cosine transformation circuits (DCT/IDCT)
  - Variable-length encoding and decoding circuits (VLC/VLD)
  - Blocking noise elimination circuit (PNR)
  - Shape information decoding circuit (CAD)
  - Pixel supplementing circuit (PADDING)
  - Image synthesis circuit (COMPOSITE)
- Full complement of image signal input and output functions
  - Video interface circuit (VIF) that supports both portrait and landscape orientation LCDs
  - Support for CIF and QCIF 4:2:2 format video input from CMOS cameras
  - P in P function that displays a subscreen in the lower right of the main screen
  - Cursor and blue background display functions.
  - Mosquito noise elimination filter
- Functions for picture quality adjustment and for combining video and graphics
  - IIC (Inter IC) interface (Conforms to Version 2.0, standard and fast mode)
  - Video signal format conversion function (YCbCr 4:2:2 → RGB; can be stopped when not needed.)
  - Graphics overlay function (Either post RGB conversion or post dithering can be selected.)
  - Video signal adjustment functions: outline enhancement, tint, color gain, brightness, contrast, and gamma adjustment
  - Dithering function for pseudo 24-bit color (2×2 matrix)
  - Monochrome conversion function (Either monochrome or sepia can be specified.)
  - Allows moving the display area (a 176-pixel × 220-line area placed anywhere within a 352-pixel × 288-line image)
  - YCbCr 4:2:2 test image generation function (75% color bar, horizontal/vertical stripe, arbitrary brightness/color difference)
  - Camera reset control function
- Large on-chip DRAM capacity
  - On-chip 20 Mbit DRAM provided to reduce parts counts and achieve overall system cost reductions

■ Features (continued)

- Built-in multifunction memory interface
  - Memory interface circuit (MIF) for batch centralized management of DMA transfers between internal DRAM and the following internal circuit blocks: main processor (MP) block, host interface (HIF) block, and video interface block (VIF).
  - 16-bit internal DRAM bus width for high-speed data transfers
  - Adopts a DMA transfer reservation and reservation unit prioritization method for efficient data transfers.
  - Ring buffer structure and matrix address access structure
- Extensive set of peripheral functions
  - One nonmaskable and two maskable interrupt systems
  - Parallel I/O functions
  - Timer functions
  - Microcode downloading function
- Program debugging mode
  - Provides a dedicated debugging mode that can access all memory spaces in the IC for easy program debugging during microcode development.
- Supply voltage: 3.3 V external (2.9 V) and 1.8 V internal

  PLL block: 3.3 V (2.9 V)

  DRAM block: 3.3 V and 1.8 V
- Internal operating frequency: 54 MHz (External input frequency: 76.8 kHz)
- Package: 239-pin CSP

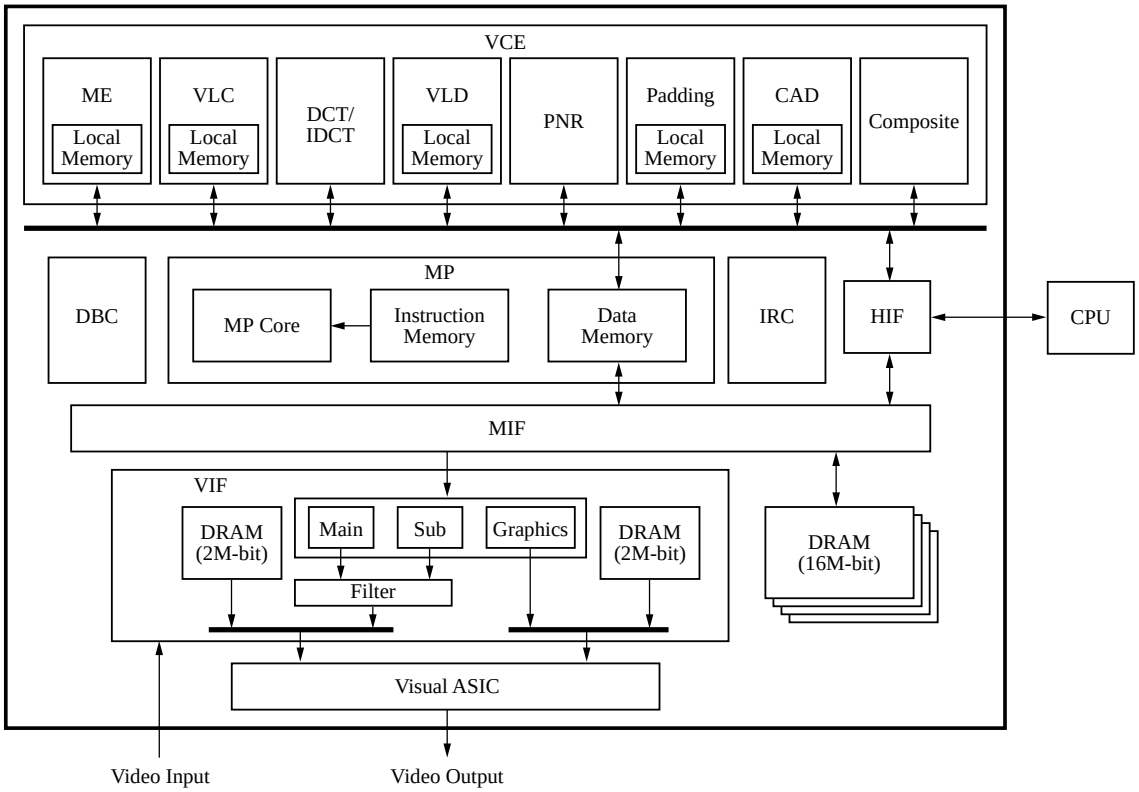
■ Applications

- Cell phones, PDAs, and other communication equipment

■ Block Diagram

MN1959041 consists of the following hardware blocks.

- MP (Main Processor)
- HIF (Host Interface)
- MIF (Memory Interface)
- Visual ASIC
- IRC (Interrupt Controller)
- VCE (Video Codec Engine)
- VIF (Video Interface)
- DBC (Debug Controller)



■ Functional Description

1. MP (Main Processor) Block

The MP block is a processor core that can interpret and execute programs. It has the following features.

- 16-bit fixed-point DSP core
- Instruction cycle: 18.6 ns (53.76 MHz)
- Most instructions execute in a single machine cycle.
- Instruction length: 32 bits, data length: 16 bits
- Program memory: 16K words, boot memory: 1K words
- On-chip data memory: total of 21K words in three areas
- Data path functions: 16-bit extended arithmetic and logic unit (EALU)
  Multiplier: 16-bit × 16-bit
  Arithmetic unit: 32 bits
  Shifter: 32 bits
  General-purpose registers: sixteen 16-bit registers
- Double bank data memory structure that supports parallel execution of DMA transfers and MP internal calculations
- Each data memory has its own matrix addressing generator for accessing matrices in a memory space.
- Provides vector pipelined arithmetic instructions that allow a single engine block to be embedded in a vector pipeline for execution.
- Conditional vector pipeline instructions
- Loop control with four independent loop counters
- Subroutine control with up to 16 levels of nesting
- Dedicated interrupt program counter stack

2. IRC (Interrupt Controller) Block

MN1959041 can temporarily halt an executing program when an interrupt request occurs, transfer control to an interrupt handler, and then continue the interrupted program when the interrupt handling completes.

This interrupt function does not interrupt instruction execution itself, but occurs between instructions. Note that this means that when an instruction that requires multiple clock cycles, such as a vector instruction, is executing, there are periods when interrupts cannot be accepted. Also note that there are cases where the occurrence of an interrupt can result in an MP or VCE state transition.

There are two types of interrupt: internal interrupts that occur within the MP, and external interrupts that occur outside the MP.

Interrupts also are classified into the following two classes:

Maskable interrupts: interrupts that can be enabled or disabled under program control, and

Nonmaskable interrupts: Interrupts that cannot be disabled.

Interrupts are assigned priority levels, and when multiple interrupts occur at the same time, the interrupt with the highest priority is accepted first. When multiple interrupts with the same priority level occur at the same time, either the software must determine the priority level or the priority must be controlled in software using the interrupt mask register.

Table 1 shows the interrupt types.

■ Functional Description (continued)

2. IRC (Interrupt Controller) Block (continued)

Table 1. Interrupt Types

Priority level		Masking	Interrupt
1	High	Nonmaskable	Watchdog timer interrupt
2		Nonmaskable	External pin nonmaskable interrupt
3		Maskable	Stack exception (stack overflow)
		Maskable	Stack exception (stack underflow)
		Maskable	Software interrupt
		Maskable	Interrupt request No. 0
			⋮
	Low		Interrupt request No. 12

3. HIF (Host Interface) Block

The HIF block performs the data transfers between MN1959041 and an external CPU. The IC and the CPU are connected by a 16-bit data bus. During these transfers, the CPU must set, in advance, the bus mode, which determines the physical usage of the data bus. The CPU must set up 16-bit bus mode for transfers with the IC, but can use 8-bit or 16-bit access for other purposes. For example, the CPU can use 8-bit access for bit stream data, and use 16-bit access for all other data transfers.

A total of 32 signal lines are required for to the host memory (HM), and for write operations, the IC uses two write enable lines to distinguish between 8-bit and 16-bit access. For read access, the IC always operates in 16-bit output mode in response to the read enable signal. (The CPU must distinguish between the 16 bits of valid data and 8 bits of valid data cases.)

4. VCE (Video Coded Engine) Block

MN1959041 includes a built-in VCE that executes video codec operations at high speeds. In particular, it includes the following circuits.

- Motion detection circuits (MEF, MEH)
- Discrete cosine transformation/inverse discrete cosine transformation circuits (DCT/IDCT)
- Variable-length encoding and decoding circuits (VLC/VLD)
- Blocking noise elimination circuit (PNR)
- Shape information decoding circuit (CAD)
- Pixel supplementing circuit (PADDING)
- Image synthesis circuit (COMPOSITE)

The tables below shows the special-purpose circuits (engines) that form the VCE classified as encoder engine or decoder engine.

Table 2. Encoder Engines

Engine	Function	Type
MEF	Full pel motion detection	A
MEH	Half pel motion detection	A
VLC	Variable-length coding	A
DCT/IDCT	One-dimensional DCT/IDCT calculation	B

■ Functional Description (continued)

4. VCE (Video Coded Engine) Block (continued)

Table 3. Decoder Engines

Engine	Function	Type
MEH	Half pel generation	A
IDCT	One-dimensional IDCT calculation	B
VLD	Variable-length decoding	A
PNR	Blocking noise elimination	B
PADDING	Horizontal/vertical, expanded, and fixed-value padding	A
CAD	Shape information decoding	A
COMPOSITE	Image composition	B
THROUGH	Data through (Data is output without processing)	B

The CAD, PADDING, and COMPOSITE items in the above table are core profile engines.

The engines in the VCE block are classified into type A and type B engines. Type A engines operate independently of the MP block, and type B engines operate in conjunction with the MP block.

5. MIF (Memory Interface) Block

The MIF block arbitrates and controls DMA transfers between the MP, HIF, and VIF functional blocks. The following are the main types of DMA transfers provided.

- Data transfers with the MP DM (Data Memory). These are used for functions such as motion detection and compensation.
- Data transfers with the HIF HM (HIF Memory). These are used for bit stream data.
- Image data I/O transfers with VIF performed at fixed periods.

Requests for DMA transfers other than video I/O are issued with priorities assigned from the MP. Although VIF DMA transfers are performed with the highest priority (level 0), the transfer priority for other DMA transfers can be specified. Table 4 lists the types of priority level.

Table 4. Priority Level Types

Level	Priority	Usage
Level 0	High	Only used for image I/O
Level 1	↕	Programmable
Level 2		
Level 3	Low	

The MIF supports the four addressing modes listed below.

1) P+ : Consecutive access
2) Sag+ : Matrix access
3) RP+ : Ring buffer access
4) RP+DF : Ring buffer access with start address offset (every transfer)

MN1959041 provides two large-capacity DRAMs; working memory and frame memory. Working memory is mainly used for image compression and expansion, and frame memory is mainly used as the frame buffer used for VIF image output. Working memory is 16 Mbits of DRAM formed from four 4 Mbit DRAMs. Frame memory consists of a video buffer and a graphics buffer, each of which formed from a single 2 Mbit DRAM for a total of 2 DRAM chip. The operation frequency used is 53.76 MHz. Table 5 lists the internal DRAM structures and details of these memories.

■ Functional Description (continued)

5. MIF (Memory Interface) Block (continued)

Table 5. Internal DRAM Structure

	Work Memory	Frame Memory
Capacity	16M-bit (4M-bit × 4)	2 M-bit × 2
Bus width	16-bit	64-bit
Transfer speed	53.76 MHz	53.76 MHz
Use	Used by the MP.	Used by the VIF for video and graphics.

6. VIF (Video Interface) Block

MN1959041 includes the VIF block as the interface that passes image data between the IC and the image sensor and the LCD display.

The VIF input system provides functions for acquiring, at the stipulated frame rate, CIF or QCIF images sent from an external image sensor at 15 fps, and storing those images in working memory (internal DRAM) as object images for encoding.

The VIF output system provides functions for output of images encoded internally in the IC for LCD display at 60 fps. It also provides image size conversion from QCIF to CIF, mosquito noise elimination filter execution as required for QCIF images, functions for subscreen generation and display at lower right of the main screen, and a cursor display function.

In the VIF block, video images are processed in YCbCr format, and graphics images are processed in RGB format.

The VIF block supports two screen display modes. The first is a full-screen mode that displays all of the image data in the CIF size on the LCD, and the other is a window display mode in which an arbitrary part (176 × 220) of the CIF size output from the VIF is displayed on the LCD. Actual output to the LCD is performed through the Visual ASIC block.

7. Visual ASIC Block

The Visual ASIC block takes the video and graphics data output from the VIF block as input, synthesizes the final images, and adjusts the image. The features of the Visual ASIC block are listed below.

- IIC (Inter IC) interface (Conforms to Version 2.0, standard and fast mode)
- Video signal format conversion function (YCbCr 4:2:2 → RGB, can be stopped when not needed.)
- Graphics overlay function (Either post RGB conversion or post dithering can be selected.)
- Video signal adjustment functions: outline enhancement, tint, color gain, brightness, contrast, and gamma adjustment
- Dithering function for pseudo 24-bit color (2 × 2 matrix)
- Monochrome conversion function (Either monochrome or sepia can be specified.)
- Allows moving the display area (a 176-pixel × 220-line area placed anywhere within a 352-pixel × 288-line image)
- Provides a 4-format LCD connection interface.
- YCbCr 4:2:2 test image generation function (75% color bar, horizontal/vertical stripe, arbitrary brightness/color difference)
- Camera reset control function

■ Functional Description (continued)

8. DBC (Debug Controller) Block

MN1959041 provides its own debugging mode functions, and, when it is in HOLD mode, provides functions for reading and writing internal registers and memory, setting MP breakpoints, and other debugging operations. These functions can contribute to improved efficiency when debugging actual end products, and improved efficiency in system debugging.

The IC provides the following functions in debug mode.

- Read and write operation to internal registers
- Read and write operation to internal memory spaces
- Read and write operation to internal DRAM
- Breakpoint setting functions
  - PC value break
  - DM1 address break
  - DM2 address break
  - GM address break
  - CM address break
- PC trace function
  - 1-bit trace
  - 7-bit trace

9. Operating States and State Transition Control

MN1959041 has 4 operating states: RUN, HOLD, SLEEP, and WAIT.

RUN mode is the state where the program is executing, and HOLD mode is the state where program execution is stopped. SLEEP mode and WAIT mode are both program stopped states, but WAIT mode is a state that waits for the completion of specific processing (specified by the program) and switches to RUN mode automatically at the point completion is verified.

Of these four modes, HOLD mode can be used for program debugging, and allows the IC internal memory (instruction memory and data memory) to be read and written from external circuits.

The IC is started externally by clearing a reset applied with an external pin (the NVRST pin). After startup, the IC can be stopped and restarted with an external pin (the VHOLD pin).

The IC operating state can be observed from the VST[2:0] pins. Table 6 lists the processor states as indicated by these pins.

Always set the IC to HOLD mode before accessing internal resources when debugging. Operation is not guaranteed if resources are accessed in other modes.

Table 6. Internal Operating States

		VST[2]	VST[1]	VST[0]
RUN mode		Low	Low	Low
HOLD mode	For the RUN to HOLD transition	High	Low	Low
	For the SLEEP to HOLD transition	High	High	Low
	For the WAIT to HOLD transition	High	Low	High
SLEEP mode		Low	High	Low
WAIT mode		Low	Low	High

■ Pin Arrangement

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
T	NC	NC	IN YD12	IN YD15	IN CD10	IN CD13	IN CD16	IN NHDI	OUT CAMCK	OUT LRDO2	OUT LRDO5	OUT LGDO2	OUT LGDO5	OUT LBDO0	NC	NC
R	NC	NC	IN YD11	IN YD14	IN YD17	IN CD12	IN CD15	IN NVDI	OUT CIFRQ	OUT LRDO1	OUT LRDO4	OUT LGDO1	OUT LGDO4	OUT LBDO1	NC	NC
P	OUT TEST7	OUT TEST8	IN YD10	IN YD13	IN YD16	IN CD11	IN CD14	IN CD17	IN VCKI	OUT LRDO0	OUT LRDO3	OUT LGDO0	OUT LGDO3	OUT LBDO2	OUT LBDO3	OUT LBDO4
N	OUT TEST6	OUT TEST5	OUT TEST4	GND VSSDRAM	GND VSS	GND VSS	GND VSSDRAM	GND VSSDRAM	2.9 V VDDH	2.9 V VDDH	2.9 V VDDH	2.9 V VDDH	2.9 V VDDH	OUT LBDO5	OUT LVCKO	OUT VFLG
M	OUT TEST3	OUT TEST2	OUT TEST1	GND VSS	GND VSS	NC	NC	NC	NC	NC	NC	2.9 V VDDH	2.9 V VDDH	OUT NLVSYNCO	OUT NLHSYNCO	OUT LVVALIDO
L	IN TESTMODE3	IN TESTMODE2	IN TESTMODE1	GND VSS	NC	NC	NC	NC	NC	NC	NC	NC	2.9 V VDDH	2.9 V VDDH	OUT LHVALIDO	OUT NYRESETO
K	IN TESTMODE0	IN TESTER	GND VSS	GND VSSDRAM	NC	NC	NC	NC	NC	NC	NC	NC	2.9 V VDDH	2.9 V VDDH	OUT PO0	OUT PO1
J	IN NTDRAM	IN PTESTDRAM1	GND VSS	GND VSS	NC	NC	NC	NC	NC	NC	NC	NC	2.9 V VDDH	2.9 V VDDH	IN/OUT I2CSD	IN I2CSCKI
H	IN PTESTDRAM0	IN PSCMR	2.9 V AVDD	GND AVSS	NC	NC	NC	NC	NC	NC	NC	NC	3.3 V VDDDRAMH	3.3 V VDDDRAMH	IN PI0	IN PI1
G	IN VCOI	IN MINTEST	GND VSS	GND VSS	NC	NC	NC	NC	NC	NC	NC	NC	3.3 V VDDDRAMH	1.8 V VDDDRAM	IN NVCS	IN VA0
F	IN CFO	IN VMCK	GND VSS	GND VSS	NC	NC	NC	NC	NC	NC	NC	NC	1.8 V VDDDRAM	1.8 V VDDDRAM	IN VA1	IN VA2
E	IN NPLLRST	IN PLLEN	IN NPLLEN	GND VSS	GND VSS	NC	NC	NC	NC	NC	NC	1.8 V VDD	1.8 V VDDDRAM	IN VA3	IN VA4	IN VA5
D	IN NYGCMD	IN VTSTMD	OUT VTDO	GND VSS	GND VSS	GND VSS	GND VSS	GND VSS	1.8 V VDD	1.8 V VDD	1.8 V VDD	1.8 V VDD	1.8 V VDD	IN VA6	IN VA7	IN VA8
C	IN/OUT VTRWEN	IN/OUT VTDI	IN/OUT VTCK	IN NVBTRO	IN NVIRQ0	IN NVWE1	IN/OUT VPIO3	IN/OUT VPIO0	IN/OUT VD13	IN/OUT VD10	IN/OUT VD7	IN/OUT VD4	IN/OUT VD1	IN VA10	IN VA9	NC
B	NC	NC	OUT VST2	IN VHOLD	IN NVIRQ1	IN NVRE	OUT TEST0	IN/OUT VPIO1	IN/OUT VD14	IN/OUT VD11	IN/OUT VD8	IN/OUT VD5	IN/OUT VD2	IN VA11	NC	NC
A	NC	NC	OUT VST1	OUT VST0	IN NVNMI	IN NVRST	IN NVWE0	IN/OUT VPIO2	IN/OUT VD15	IN/OUT VD12	IN/OUT VD9	IN/OUT VD6	IN/OUT VD3	IN/OUT VDO	NC	NC

■ Pin Descriptions

Pin	I/O	Description		Normal usage
YDI[7:0]	I	Video input	Luminance data input	
CDI[7:0]	I		Color difference input	
NVDI	I		Vertical sync signal	
NHDI	I		Horizontal sync signal	
VCKI	I		Input system video clock (2.250 MHz)	
CIFRQ	O		CIF size request signal	
CAMCK	O		Camera block operating clock (9.000 MHz)	
VFLG	O	Video output	MMP1 output frame update flag	
I2CSCKI	I		I2C interface serial clock input	
I2CSD	I/O/Z		I2C interface serial data I/O	
LRDO[5:0]	O		Red data (Outputs the MMP1 YDO[7:2] bits in V-ASIC through mode.)	
LGDO[5:0]	O		Green data (Outputs the MMP1 YDO[1:0] and CDO[7:4] bits in V-ASIC through mode.)	
LBDO[5:0]	O		Blue data (Outputs the MMP1 CDO[3:0] and 2'b00 bits in V-ASIC through mode.)	
NLVSYNCO	O		Vertical sync signal	
NLHSYNCO	O		Horizontal sync signal	
LVVALIDO	O		Vertical data valid flag	
LHVALIDO	O		Horizontal data valid flag	
LVCKO	O		Output system video clock (9.000 MHz)	
PI[1:0]	I		General-purpose input port	
PO[1:0]	O		General-purpose output port	
NVRESETO	O		Camera vertical sync and horizontal sync output reset signal	
NVCS	I	Host interface	Chip enable from the MMP-C	
VA[11:0]	I		Input address bus from the MMP-C	
VD[15:0]	I/O/Z		I/O data bus from the MMP-C	Pull Up
NVWE[1:0]	I		Write enable from the MMP-C	
NVRE	I		Read enable from the MMP-C	
VPIO[3:0]	I/O		Parallel I/O with the MMP-C	Pull Up
TEST0	O		Contention access signal between the MP and the MMP-C to the HM.	NC
NVIRQ[1:0]	I	Misc	Maskable interrupt request signal from the MMP-C	Pull Up
NVNMI	I		Nonmaskable interrupt request from the MMP-C	Pull Up
NVRST	I		MMP-V reset request signal from the MMP-C	
NVBTRQ	I		Boot request at MMP-V reset clear	
VHOLD	I		MMP-V hold signal from the MMP-C	
VST[2:0]	O		MMP-V operating state signals to the MMP-C	

■ Pin Descriptions (continued)

Pin	I/O	Description		Normal usage
VTCK	I/O/Z	Debugging interface	Debugging clock PC value serial output clock (VTCK pin shared function)	Low
VTDI	I/O/Z		Serial debugging data input PC value serial output start bit flag (VTDI pin shared function)	Low
VTDO	O		Serial debugging data output PC value serial output	
VTRWEN	I/O/Z		Serial debugging data I/O enable PC value increment flag (VTRWEN pin shared function)	Low
NVGCMD	I		MMP-V internal 54 MHz clock gated mode setting	Low
VTSTMD	I		TEST pin output mode setting	Low
TEST1	O		MMP-V internal VIF signal debugging output or PC value [1] output	NC
TEST2	O		MMP-V internal VIF signal debugging output or PC value [2] output	NC
TEST3	O		MMP-V internal VIF signal debugging output or PC value [3] output	NC
TEST4	O		MMP-V internal VIF signal debugging output or PC value [4] output	NC
TEST5	O		MMP-V internal VIF signal debugging output or PC value [5] output	NC
TEST6	O		MMP-V internal VIF signal debugging output or PC value [6] output	NC
TEST7	O		MMP-V internal MIF signal debugging output	NC
TEST8	O		MMP-V internal MIF signal debugging output	NC
MINTEST	I	Test mode	Buffer test control input	Low
TESTER	I		Normal mode/test mode switching	Low
TESTMODE0	I		Test mode setting	Low
TESTMODE1	I		Test mode setting	Low
TESTMODE2	I		Test mode setting	Low
TESTMODE3	I		Test mode setting	Low
PTESTDRAM0	I		DRAM test mode setting 0	Low
PTESTDRAM1	I		DRAM test mode setting 1	Low
NTDRAM	I		Normal mode/shift mode switching during DRAM scan testing	Low

■ Pin Descriptions (continued)

Pin	I/O	Description		Normal usage
VMCK	I	PLL	MMP-V operation reference clock (input to the PLL)	76.8 KHz
NPLLEN	I		MMP1 internal operating clock selection	Low
PLLEN	I		Selection of the clock input the MMP1 internal divide-by-two circuit	High
NPLLRST	I		MMP-V internal PLL reset	High
VCOI	I		VCO analog voltage input	
AVDD	—		PLL power supply: +2.9 V	2.9 V
AVSS	—		PLL ground	AVSS
CFO	—	Power supply	Test pin	High
PSCMR	I		Test pin	High
VDDH	—		Power supply: +2.9 V	2.9 V
VDD	—		Power supply: +1.8 V	1.8 V
VSS	—		Ground	DGND
VDDDRAMH	—		DRAM power supply: +3.3 V	3.3 V
VDDDRAM	—		DRAM power supply: +1.8 V	1.8 V
VSSDRAM	—		DRAM ground	GND
PVBBDRAM	—		P detection substrate power supply monitor output	
PVBPDRAM	—		P detection test bit line precharge power supply monitor output	

■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
External supply voltage *	V_{DD}	– 0.3 to +4.6	V
Internal supply voltage *	V_{DDI}	– 0.3 to +2.5	V
Input pin voltage	V_I	– 0.3 to V_{DD} + 0.3 (Upper limit: 4.6)	V
Output pin voltage	V_O	– 0.3 to V_{DD} + 0.3 (Upper limit: 4.6)	V
Output current (Type HL4 pins)	I_O	±20	mA
Power supply input current	I_V	±70 (Per pin)	mA
Power dissipation	P_D	1.77	mW
Operating temperature	T_{opr}	–20 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. *: When one of VDD and VDDI is off and the other on, through currents flow and the outputs will be undefined. There are no stipulation on the power on and power off sequences. The power supply levels should be applied as close to simultaneously as possible. However, this does no apply when CFO is controlled.

2. Type HL4 pins: CIFRQ, CAMCK, VFLG, I2CSD, LRDO[0] to LRDO[5], LGDO[0] to LGDO[5], LBDO[0] to LBDO[5], NLVSYNCO, NLHSYNCO, LVVALIDO, LHVALIDO, LVCKO, PO[0], PO[1], NVRESRTO, VD[0] to VD[15], VPIO[0] to VPIO[3], VST[0] to VST[2], VTCK, VTDI, VTDO, VTRWEN, TEST[0] to TEST[8]

3. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Functional operation is not guaranteed over the complete span of these ranges.

4. All of the VDD and VSS pins must be connected directly to their corresponding power supply and ground levels.

■ Electrical Characteristics (continued)

2. Recommended Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External supply voltage	V_{DD}		2.7	2.9	3.1	V
Internal supply voltage	V_{DDI}		1.65	1.8	1.95	V
DRAM supply voltage	V_{DD18D}		1.65	1.8	1.95	V
DRAM step-up supply voltage	V_{DD33D}		3.0	3.3	3.6	V
Analog supply voltage	AV_{DD}		2.7	2.9	3.1	V
Ambient temperature	T_a		–20	—	70	°C

3. I/O Capacitances

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input pins	C_{IN}	$V_{DD} = V_{DDI} = V_I = 0$ V	—	7	8	pF
Output pins	C_{OUT}	f = 1 MHz, T_a = 25°C	—	7	8	pF
I/O pins	C_{IO}		—	7	8	pF

4. DC Characteristics at V_{DD} = 2.7 V to 3.1 V, V_{DDI} = 1.65 V to 1.95 V, V_{SS} = 0 V, f_{TEST} = 54 MHz, T_a = -20°C to +70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I/O power supply operating supply current	I_{DDO}	$V_I = V_{DD}$ or V_{SS}, f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, outputs open	—	4	12.0	mA
Internal power supply operation supply current	I_{DDIO}	$V_I = V_{DD}$ or V_{SS}, f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, outputs open	—	50	85.0	mA
DRAM 3.3 V power supply operating supply current (Normal mode) *	I_{DDDO}	$V_I = V_{DD}$ or V_{SS}, f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	0.3	2.0	mA
DRAM 3.3 V power supply operating supply current (Standby test mode)	I_{DDDO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	0.3	4.1	mA
DRAM 3.3 V power supply operating supply current (Dynamaic test mode)	I_{DDDO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	1.3	5.7	mA
DRAM 3.3 V power supply operating supply current (Page mode test mode)	I_{DDDO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	0.1	5.0	mA
DRAM 3.3 V power supply operating supply current (Self refre test mode)	I_{DDDO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	0.3	4.4	mA

Note) *: Design value

■ Electrical Characteristics (continued)

4. DC Characteristics at V_{DD} = 2.7 V to 3.1 V, V_{DDI} = 1.65 V to 1.95 V, V_{SS} = 0 V, f_{TEST} = 54 MHz, T_a = -20°C to +70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DRAM internal power supply operating supply current (Normal mode) *	I_{DDDIO}	$V_I = V_{DD}$ or V_{SS}, f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	6.0	12.0	mA
DRAM internal power supply operating supply current (Standby test mode)	I_{DDDIO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	3.0	10.0	mA
DRAM internal power supply operating supply current (Dynamaic test mode)	I_{DDDIO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	25.0	50.0	mA
DRAM internal power supply operating supply current (Page mode test mode)	I_{DDDIO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	25.0	50.0	mA
DRAM internal power supply operating supply current (Self refre test mode)	I_{DDDIO}	$V_I = V_{DD}$ or V_{SS}, f = 30 MHz, $V_{DDDRAMH}$ = 3.3 V, V_{DDDRAM} = 1.8 V, outputs open	—	3.0	15.0	mA
Analog power supply operating supply current	I_{DDAO}	$V_I = V_{DD}$ or V_{SS}, fin = 76.8 kHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, AV_{DD} = 2.9 V, outputs open	—	0.5	1.0	mA
I/O power supply quiescent supply current	I_{DDQO}	$V_I = V_{DD}$ or V_{SS}, f = 0 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, AV_{DD} = 2.9 V, outputs open	—	1	20.0	µA
Analog power supply quiescent supply current	I_{DDQAO}	$V_I = V_{DD}$ or V_{SS}, fin = 0 kHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, AV_{DD} = 2.9 V, outputs open	—	1	20.0	µA

Note) *: Design value.

■ Electrical Characteristics (continued)

4. DC Characteristics at V_{DD} = 2.7 V to 3.1 V, V_{DDI} = 1.65 V to 1.95 V, V_{SS} = 0 V, f_{TEST} = 54 MHz, T_a = -20°C to +70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1) LVCMOS level inputs: I2CSCKI, PI[0], PI[1], NVCS, VA[0] to VA[11], NVWE[0], NVWE[1], NVRE, NVIRQ[0], NVIRQ[1], NVNMI, NVRST, NVBTRQ, VHOLD, NVGCMD, VTSTMD, TESTER, TESTMODE[0] to TESYMODE[3], PTESTDRAM[0], PTESTDRAM[1], NTDRAM, VMCK, NPLLEN, PLLEN, NPLLRST, CFO, PSCMR						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	—	±10	µA
2) LVCMOS level inputs with pull-down resistors: YDI[0] to YDI[7], CDI[0] to CDI[7], NVDI, NHDI, VCKI, MINTEST						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Pull-down resistance	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Output leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
3) LVCMOS level I/O pins: CIFRQ, CAMCK, VFLG, I2CSD, LRDO[0] to LRDO[5], LGDO[0] to LGDO[5], LBDO[0] to LBDO[5], NLVSYNCO, NLHSYNCO, LVVALIDO, LHVALIDO, LVCKO, PO[0], PO[1], NVRESETO, VD[0] to VD[15], VPIO[0] to VPIO[3], VST[0] to VST[2], VTCK, VTDI, VTDO, VTRWEN, TEST[0] to TEST[8]						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
High-level output voltage	V_{OH}	I_{OH} = 4.0 mA, $V_I = V_{DD}$ or V_{SS}	$V_{DD} \times 0.8$	—	V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL} = 4.0 mA, $V_I = V_{DD}$ or V_{SS}	0	—	$V_{DD} \times 0.2$	V
Output leakage current	I_{LO}	V_O = High-impedance state, $V_I = V_{DD}$ or V_{SS}, $V_D = V_{DD}$ or V_{SS}	—	—	±10	µA
PLL oscillator frequency	F_{OSC}	F_{IN} = 76.8 kHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V, AV_{DD} = 2.9 V, R_2 = 390 Ω, C_1 = 1.0 µF, C_2 = 0.047 µF	—	53.76	—	MHz

■ Electrical Characteristics (continued)

5. AC Characteristics

1) Video input interface timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video Input Timing						
YC data setup time from the VCKI rising edge *	t_{VISD}	$V_I = V_{DD}$ or V_{SS} , f = 54 MHz,	1	12	—	cycle
YC data hold time from the VCKI rising edge *	t_{VIHD}	V_{DD} = 2.9 V, V_{DDI} = 1.8 V	5	12	—	cycle
VCKI low-level period	t_{VICWVL}		—	12	—	cycle
VCKI high-level period	t_{VICWVH}		—	12	—	cycle
VCKI frequency	t_{VICWV}		—	24	—	cycle
Sync setup time from the VCKI rising edge *	t_{VISS}		2	12	—	cycle
Sync hold time from the VCKI rising edge *	t_{VIHS}		3	12	—	cycle
CAMCK output frequency	t_{VICWC}		—	6	—	cycle

Note) 1. The stipulated values that follow are all design values. Note that the unit "cycle" in the table refers to one clock period of internal operating frequency.

2. *: This must be used within ±1 of the typical value if at all possible.

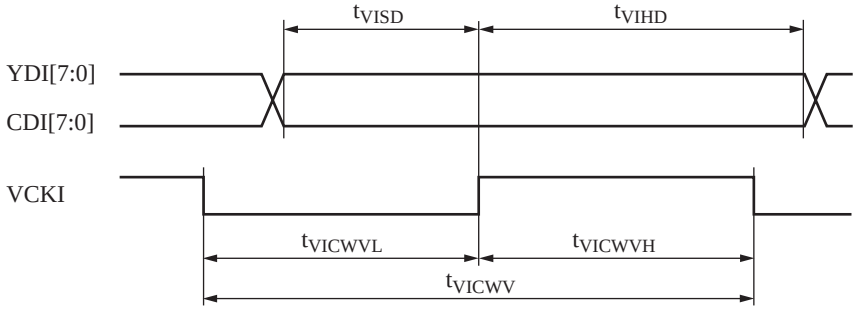


Figure 1. YC data input timing

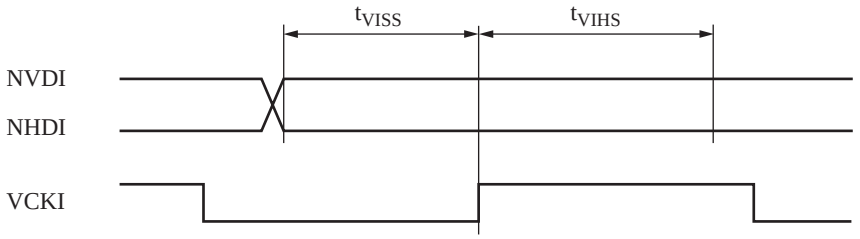


Figure 2. Vsync and Hsync input timing

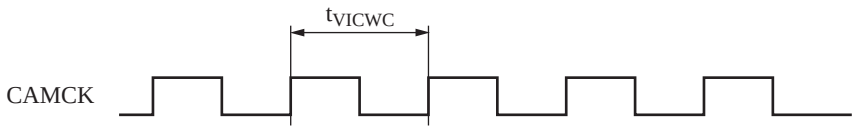


Figure 3. CAMCK output timing

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

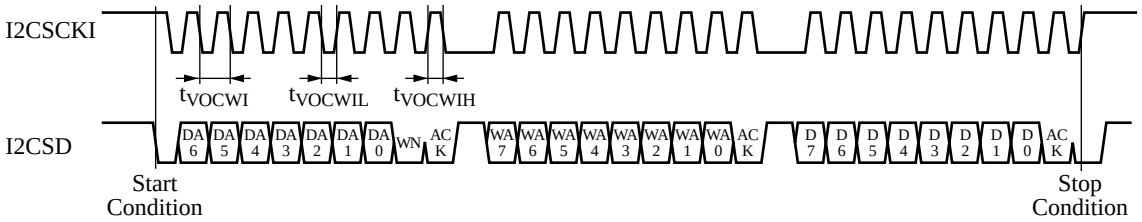
2) Video output interface timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video Output Timing						
I2CSCKI cycle time	t_{VOCWI}	$V_I = V_{DD}$ or V_{SS} ,	2.5	10	—	µs
I2CSCKI high-level pulse width	t_{VOCWIH}	f = 54 MHz,	0.6	4.0	—	µs
I2CSCKI low-level pulse width	t_{VOCWIL}	V_{DD} = 2.9 V,	1.3	4.7	—	µs
I2CSD setup time	t_{VOSI}	V_{DDI} = 1.8 V	250	—	—	ns
I2CSD hold time	t_{VOHI}		300	—	—	ns
NLVSYNCO cycle time	t_{VOCWV}		16.7	16.7	16.7	ms
NLVSYNCO high-level pulse width	t_{VOCWVH}		16	16	16	ms
NLVSYNCO low-level pulse width	t_{VOCWVL}		665.7	666.7	667.7	µs
NLHSYNCO cycle time	t_{VOCWH}		54.6	55.6	56.6	µs
NLHSYNCO high-level pulse width	t_{VOCWHH}		38.1	39.1	40.1	µs
NLHSYNCO low-level pulse width	t_{VOCWHL}		15.4	16.4	17.4	µs
LVCKO cycle time	t_{VOCWL}		80	111	140	ns
LVCKO high-level pulse width	t_{VOCWLH}		40	55	70	ns
LVCKO low-level pulse width	t_{VOCWLL}		40	55	70	ns
Delay time from the NLVSYNCO rising edge to the LVVALIDO rising edge	t_{VODV}		0	—	3.78	ms
LVVALIDO high-level pulse width	t_{VOPWVH}		12.2	12.2	12.2	ms
Delay time from the NLHSYNCO rising edge to the LHVALIDO rising edge	t_{VODH}		0	—	19.6	µs
LHVALIDO high-level pulse width	t_{VOPWHH}		19.54	19.65	19.76	µs
Delay time from the LHVALIDO falling edge to the point the LVCKO stops	t_{VODHC}		1.67	1.78	1.89	µs
Delay time from the LVCKO falling edge to LRDO, LGDO, and LBDO	t_{VODCD}		0	—	9.25	ns

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

2) Video output interface timing (continued)



Note) DA6 to DA0 : Device Address = 1 000 100
WA7 to WA0 : Word Address = n
D : Word Address n Data

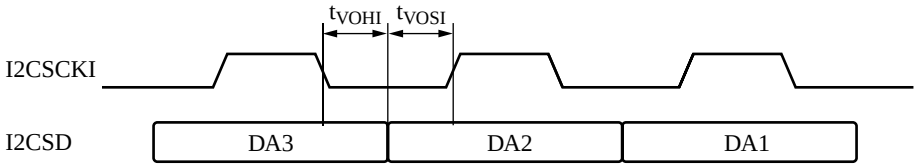
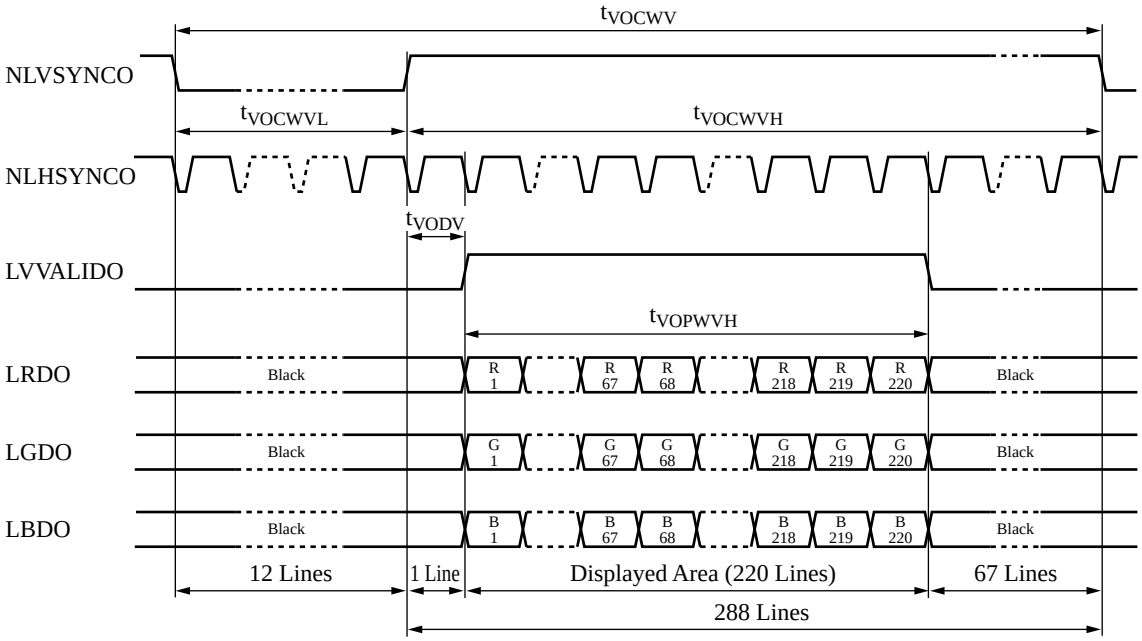


Figure 4. Random write timing



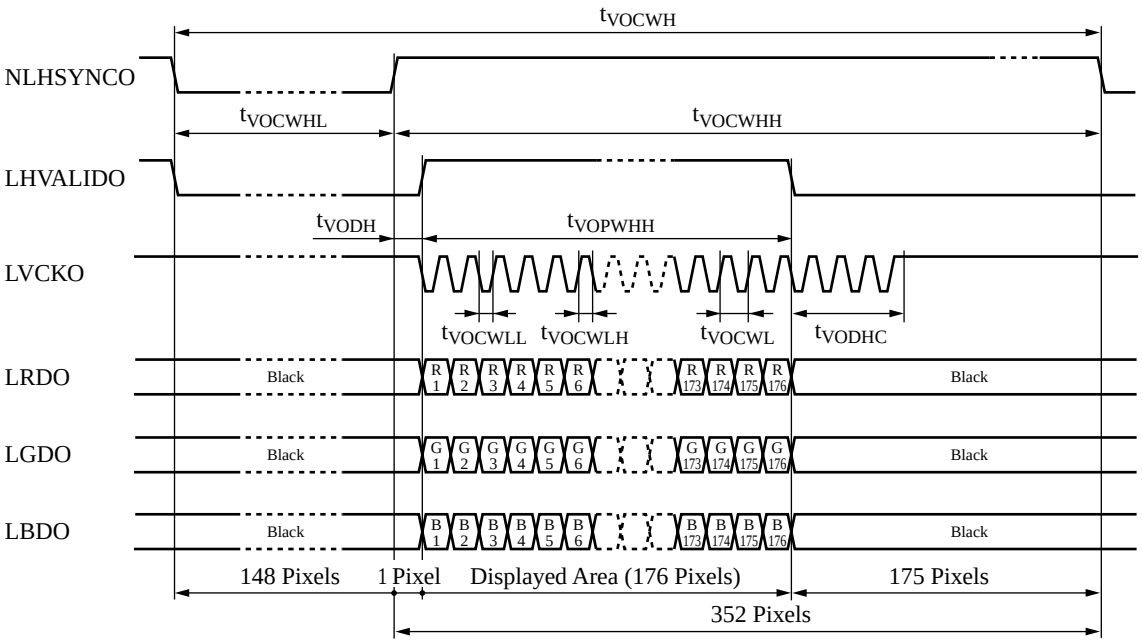
Note) When V_POS = 1, line 0 and lines 221 to 287 will be filled with black in the LCD RGB, and only lines 1 to 220 will be output.

Figure 5. Vertical timing (When V_POS = 1)

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

2) Video output interface timing (continued)



Note) When H_POS = 1, pixel 0 and pixels 177 to 351 will be filled with black in the LCD RGB, and only pixels 1 to 176 will be output.

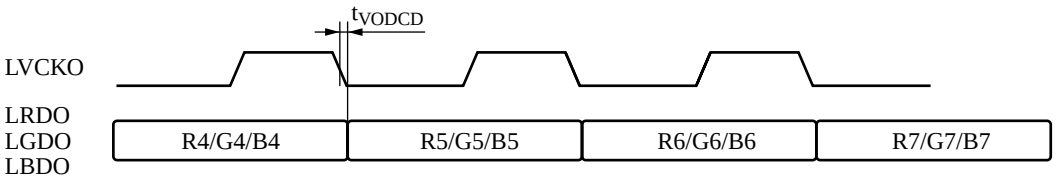


Figure 6. Horizontal timing (When V_POS = 1)

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

3) Host interface timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Host Memory and Register Access Timing						
Address and data setup time after NVCS and NVWE[1:0] go low	t_{HSD}	$V_I = V_{DD}$ or V_{SS} , f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V	0	—	—	cycle
Period that NVCS and NVWE[1:0] are both low	t_{HCWWL}		4	5	—	cycle
Address and data hold time after NVCS and NVWE[1:0] go low	t_{HHD}		0	—	—	cycle
Period that NVCS and NVWE[1:0] are both high	t_{HCWWH}		1	2	—	cycle
Address setup time after NVCS and NVRE are both low	t_{HSR}		0	—	—	cycle
Period that NVCS and NVRE go low	t_{HCWRL}		5	5.5	—	cycle
Address hold time after NVCS and NVRE go low	t_{HHA}		0	—	—	cycle
Period that NVCS and NVRE are both high	t_{HCWRH}		1	1.5	—	cycle
Data output delay time after NVCS and NVRE go low	t_{HDD}		—	—	4	cycle
Data hold time after NVCS and NVRE go high	t_{HHD}		—	—	1	cycle

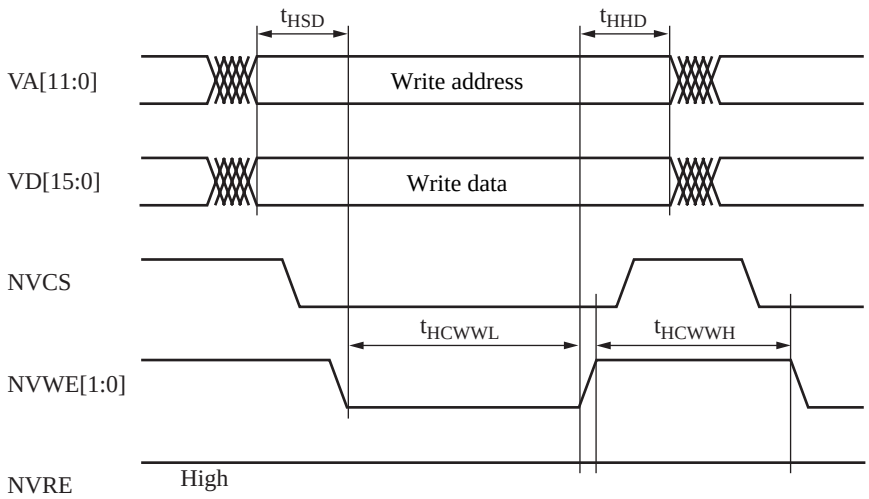


Figure 7. Host memory and register write timing

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

3) Host interface timing (continued)

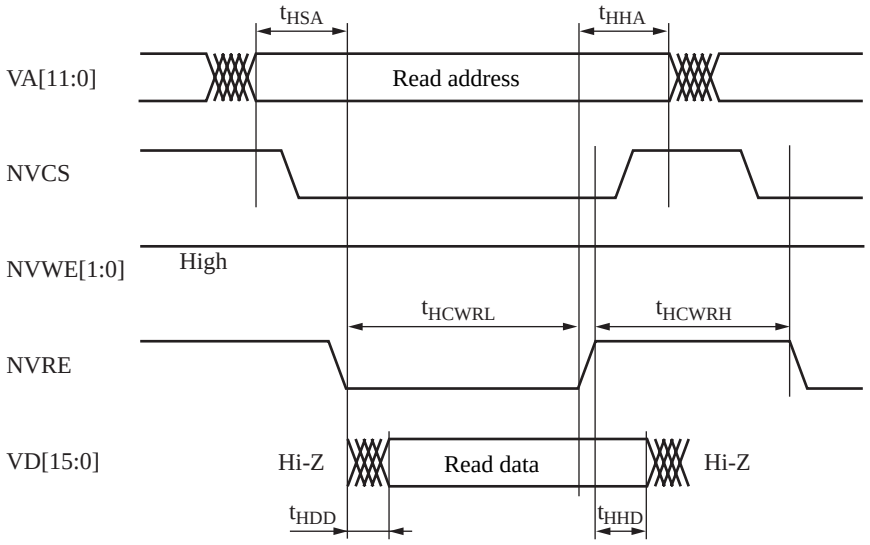


Figure 8. Host memory and register read timing

4) Interrupt input timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input Timing						
Low-level setup time after an NVNMI rising edge	t_{ISL}	$V_I = V_{DD}$ or V_{SS} , f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V	3	6	—	cycle
High-level hold time after an NVNMI rising edge	t_{IHH}		3	6	—	cycle
High-level setup time after an NVIRQ falling edge	t_{ISH}		3	6	—	cycle
Low-level hold time after an NVIRQ falling edge	t_{IHL}		3	6	—	cycle

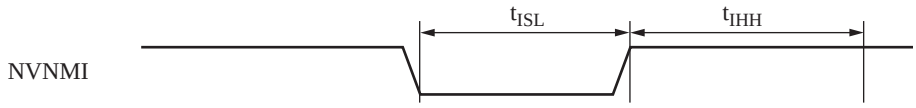


Figure 9. NVNMI interrupt input timing

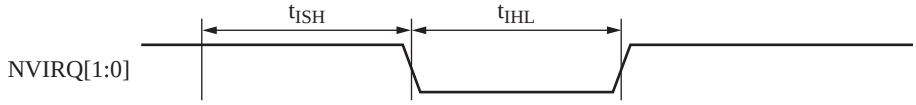


Figure 10. NVNMI interrupt input timing

■ Electrical Characteristics (continued)

5. AC Characteristics (continued)

5) Reset and boot timing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reset and Boot Timing						
Reset low-level period	t_{CWRS}	$V_I = V_{DD}$ or V_{SS} , f = 54 MHz, V_{DD} = 2.9 V, V_{DDI} = 1.8 V	6000	6000<	—	cycle
Boot request high-level setup time after the reset rising edge	t_{BSH}		3	3<	—	cycle
Boot request high-level hold time after the reset rising edge	t_{BHH}		3	3<	—	cycle

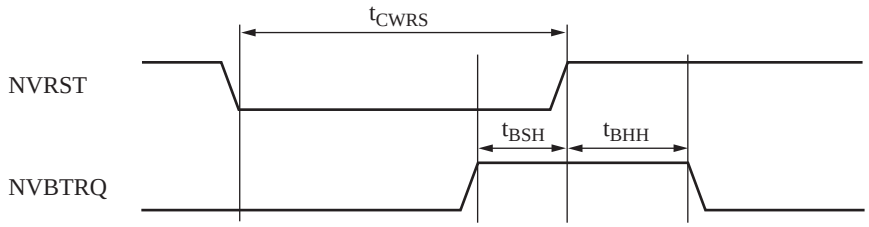
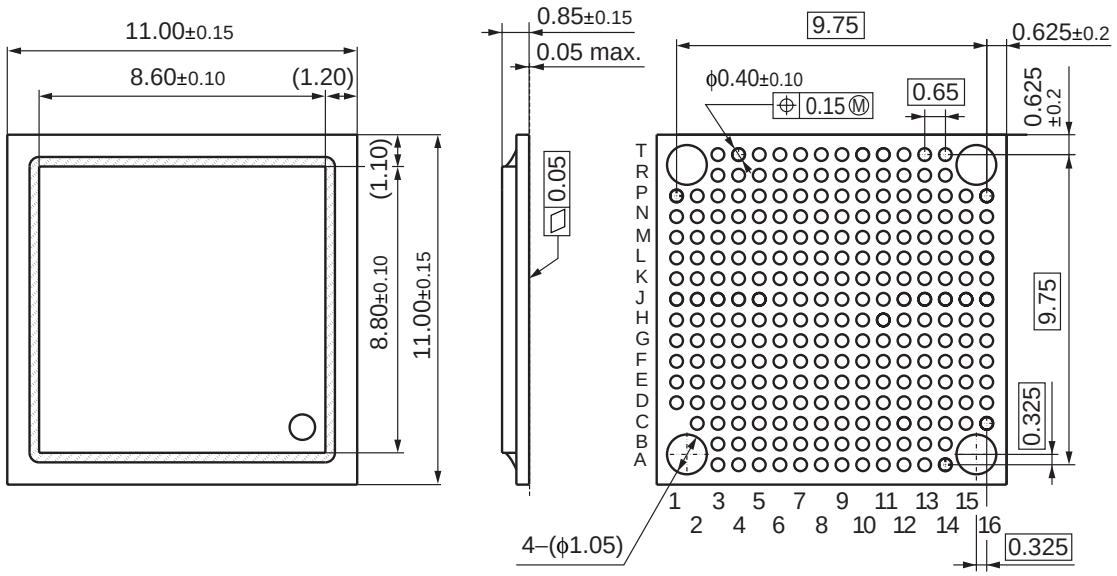


Figure 11. Reset and boot timing

■ Package Dimensions (Units: mm)

• MLGA239-C-1111 (lead free)



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