MN662792AB

1. Overview

MN662792AB is a signal processing IC for CDs. This IC integrates an optical servo (focus, tracking, and traverse servos) processing function, digital signal processing function (EFM demodulation and CIRC/CD-ROM error correction), digital servo processing function for spindle motor, anti-shock memory control function supporting 64-Mbit, 16-Mbit, 4-Mbit, or 1-Mbit DRAM that enables compression/decompression for a disc rotation synchronous playback (i.e., jitter free), a decode function for MP3/WMA†, Fs conversion processing function, a digital filter, and D/A converter. All the processing functions after the head amplifier (RF amplifier) are integrated into a single chip.
This IC includes Microsoft's technology and cannot be used and distributed without a license from Microsoft Corporation.

†: WINDOWS MEDIA AUDIO (WMA)
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2. Functions and Features

(Optical servo)

- Focus (Fo), tracking (Tr), and traverse (TRV) servos
- Automatic adjustment functions (Fo/Tr gain, Fo/Tr offset, Fo/Tr balance)
- Provided with a countermeasure for dropout
- Provided with an anti-shock function
- Provided with a track-cross detection function
- Drive output PWM drive function supported
- Provided with supply voltage monitoring and a servo gain automatic adjustment function

(Digital signal processing)

- Containing DSL and analog/digital PLL
- Provided with a frame synchronous detection/protection/interpolation
- Subcode data processing

  Q-data CRC check

  On-chip Q-data register

  On-chip CD-TEXT data register

- CIRC error correction
  - C1 decoder: double error correction
  - C2 decoder: triple/quadruple error correction
  - On-chip deinterleaving 16K RAM
- CD-ROM error correction
  - Q decoder: an error correction
  - P decoder: an error correction
  - Mode1 and Mode2 compatible
- Audio data interpolation processing
  - 4-sampling average value interpolation and previous value hold

(Spindle motor servo)

- CLV digital servo
- Servo gain setting function
- Shaft loss compensation setting function

(Audio circuit)

- Soft muting
- Digital attenuation (2048 levels)
- Soft attenuation (2048 levels)
- Digital audio interface (EIAJ format)
- 8 × oversampling digital filter
- On-chip low-voltage op amp
- Bass boost filter, high-band notch filter, and surround function
- On-chip digital de-emphasis

(MP3 decoding)

- Decoding of signals recorded in MPEG1-layer3 or MPEG2-layer3 format
- Decoding of signals recorded in MPEG1-layer2 or MPEG2-layer2 format
- Decoding of signals recorded in MPEG2.5 format
- Sampling rate conversion from signals recorded at Fs=32 kHz or 48 kHz to 44.1 kHz

(WMA decoding)

- Decoding of signals recorded in WMA Ver.8 format (Sampling rate: 48 kHz to 22.05 kHz)
- Supporting special playback (forward, reverse, and resume playback)

(SD interface)

- Stream serial input from SD available

(Anti-shock memory controller)

- ADPCM 4-bit compression or expansion/decompression in full-bit (16 bits) mode
- External DRAM selectable

  64-Mbit DRAM (16M addresses × 4 bits) × 1

  16-Mbit DRAM (4M addresses × 4 bits) × 2

  16-Mbit DRAM (4M addresses × 4 bits) × 1 + 4-Mbit DRAM (1M addresses × 4 bits) × 1

  16-Mbit DRAM (4M addresses × 4 bits) × 1

  4-Mbit DRAM (1M addresses × 4 bits) × 2

  4-Mbit DRAM (1M addresses × 4 bits) × 1

  1-Mbit DRAM (256 addresses × 4 bits) × 2

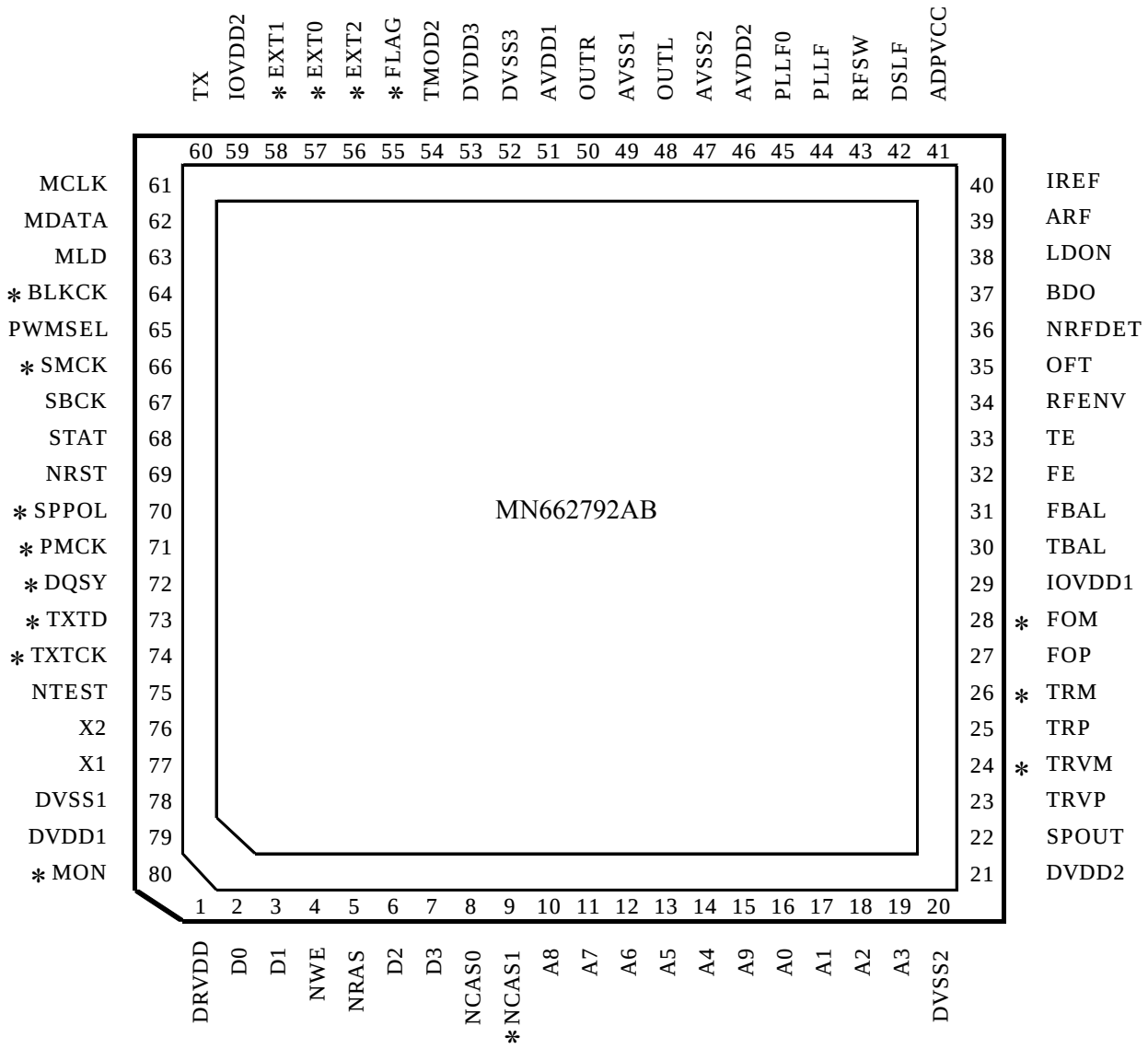
  1-Mbit DRAM (256 addresses × 4 bits) × 1

(Others)

- Disc rotation mechanism has a synchronous playback (jitter-free) mode (−50% to +50%)
- 4 × speed playback (when using jitter-free function)
- TX output (1 × , 2 × , and 3 × speed) supported
- Serial data output pitch shift function

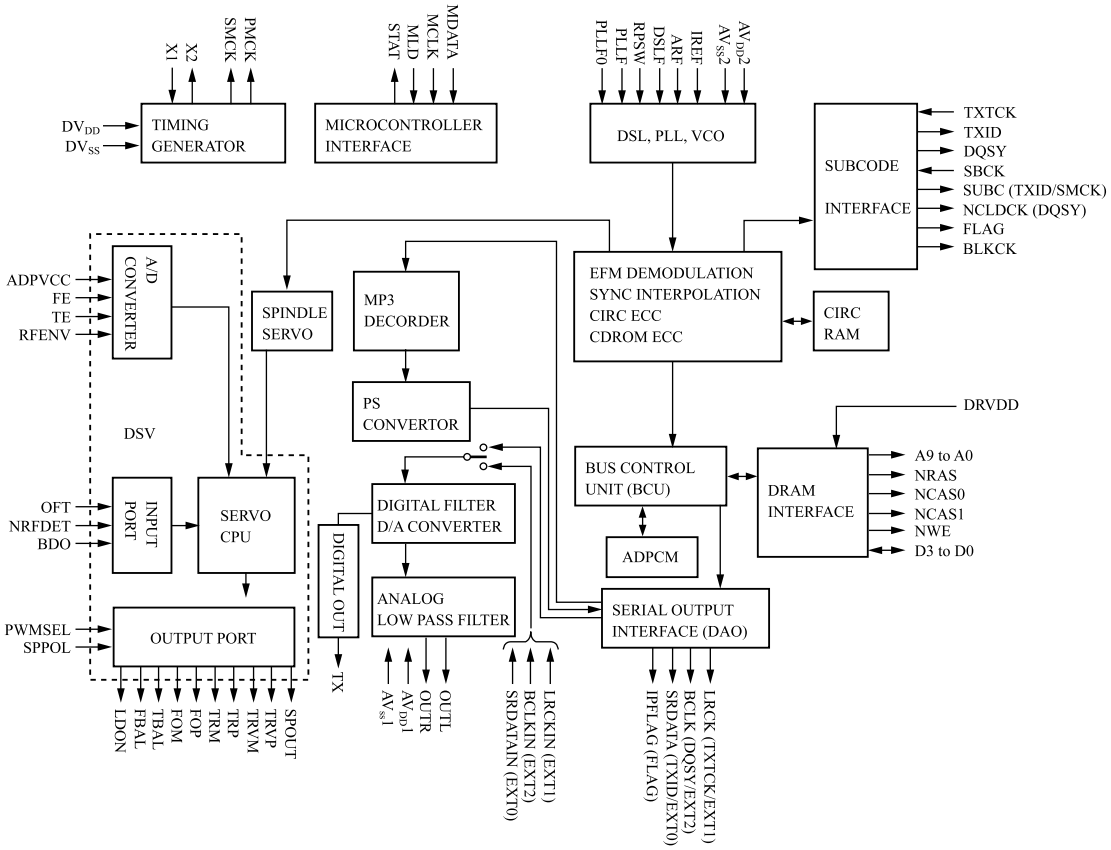
3. Pin Assignment

80-pin flat package (LQFP080-P-1414A)



Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

4. Block Diagram



5. Pin Descriptions

Pin No.	Symbol	I/O	Function
1	DRV_{DD}	I	Power supply for DRAM interface (Pins 2 to 19 and 80)
2	D0	I/O	DRAM data I/O signal 0
3	D1	I/O	DRAM data I/O signal 1
4	NWE	O	DRAM write enable signal
5	NRAS	O	DRAM RAS control signal
6	D2	I/O	DRAM data I/O signal 2
7	D3	I/O	DRAM data I/O signal 3
8	NCAS0	O	DRAM CAS control signal 0
9	*NCAS1	O	DRAM CAS control signal 1
10	A8	O	DRAM address signal 8
11	A7	O	DRAM address signal 7
12	A6	O	DRAM address signal 6
13	A5	O	DRAM address signal 5
14	A4	O	DRAM address signal 4
15	A9	O	DRAM address signal 9
16	A0	O	DRAM address signal 0
17	A1	O	DRAM address signal 1
18	A2	O	DRAM address signal 2
19	A3	O	DRAM address signal 3
20	$DV_{SS}2$	I	Ground for digital circuits
21	$DV_{DD}2$	I	Power supply for digital circuits
22	SPOUT	O	Spindle motor drive signal output (absolute value output)
23	TRVP	O	Traverse drive output (positive polarity output)
24	*TRVM	O	Traverse drive output (negative polarity output)
25	TRP	O	Tracking drive output (positive polarity output)
26	*TRM	O	Tracking drive output (negative polarity output)
27	FOP	O	Focus drive output (positive polarity output)
28	*FOM	O	Focus drive output (negative polarity output)
29	$IOV_{DD}1$	I	Power supply for I/O
30	TBAL	O	Tracking balance adjustment output
31	FBAL	O	Focus balance adjustment output
32	FE	I	Focus error signal input (analog input)
33	TE	I	Tracking error signal input (analog input)
34	RFENV	I	RF envelope signal input (analog input)
35	OFT	I	Off-track signal input High: Off-track
36	NRFDET	I	RF detection signal input Low: Detection
37	BDO	I	Dropout signal input High: Dropout
38	LDON	O	Laser ON signal output High: ON
39	ARF	I	RF signal input
40	I_{REF}	I	Reference current input

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

Pin No.	Symbol	I/O	Function
41	ADPVCC	I	Voltage input for supply voltage monitor (analog input)
42	DSLF	O	DSL loop filter
43	RFSW	I	DSL loop filter
44	PLLF	O	PLL loop filter
45	PLLFO	O	PLL loop filter
46	AVDD2	I	Power supply for analog circuits (for DSL, PLL, and A/D)
47	AVSS2	I	Ground for analog circuits (for DSL, PLL, and A/D)
48	OUTL	O	L-ch audio output
49	AVSS1	I	Ground for analog circuits (for audio output stage)
50	OUTR	O	R-ch audio output
51	AVDD1	I	Power supply for analog circuits (for audio output stage)
52	DVSS3	I	Ground for digital circuits
53	DVDD3	I	Power supply for digital circuits
54	TMOD2	I	Test input pin Low: Normal
55	∗FLAG	O	Flag signal output
56	∗EXT2	I/O	Expansion I/O port 2
57	∗EXT0	I/O	Expansion I/O port 0
58	∗EXT1	I/O	Expansion I/O port 1
59	IOVDD2	I	Power supply for I/O
60	TX	O	Digital audio interface output signal
61	MCLK	I	Microcontroller command clock signal input
62	MDATA	I	Microcontroller command data signal input
63	MLD	I	Microcontroller command load signal input Low: Load
64	∗BLKCK	O	Subcode block clock signal (f=75 Hz in normal-speed playback mode)
65	PWMSEL	I	PWM output mode selection input Low: Direct High: 3-state
66	∗SMCK	O	4.2336 MHz/8.4672 MHz clock signal output
67	∗SBCK	I/O	Clock input for subcode serial output
68	STAT	O	Status signal output
69	NRST	I	Reset input Low: Reset
70	∗SPPOL	O	Spindle motor drive signal output (polarity output)
71	∗PMCK	O	88.2-kHz clock signal output
72	∗DQSY	O	Pack signal output for CD-TEXT data
73	∗TXTD	O	CD-TEXT data signal output
74	∗TXTCK	O	External clock signal input for CD-TEXT register
75	NTEST	I	Test input pin High: Normal
76	X2	O	Crystal oscillator circuit output pin (f=16.9344 MHz, 33.8688 MHz)
77	X1	I	Crystal oscillator circuit input pin (f=16.9344 MHz, 33.8688 MHz)
78	DVSS1	I	Ground for digital circuits
79	DVDD1	I	Power supply for digital circuits
80	∗MON	O	Monitor for evaluation

Note) Pins marked with an asterisk can be switched to different signals by using microcontroller commands.

6. List of the Selection Pins

A. List of the selection pins

Pin No.	Initial setting signal	Selection signal				
9	NCAS1	A10				
24	TRVM	PC				
26	TRM	EXT4				
28	FOM	EXT3				
55	FLAG	MON2	TXNCLDCK	NRQ		
56	EXT2	SRF	BCLKIN	BCLK	EXSCK	
57	EXT0	MON3	SRDATAIN	SRDATA	STRIN	
58	EXT1	VDET	PCK	CK16M	CK8M	LRCKIN
		LRCK	VAL			
64	BLKCK	ZBLKCK	DQSY	SSYNC	DABLKCK	
66	SMCK	SUBC				
67	SBCK	WAIT				
70	SPPOL	CK16M (see note 1)				
71	PMCK	SBLKCK				
72	DQSY	BCLK	TXNCLDCK	NCLDCK		
73	TXTD	SUBC	VDET	SRDATA	SRF	
74	TXTCK	PCK	LRCK			
80	MON	NCAS1	A11			

Note 1) The CK16M is output with PWMSEL set to high and D15 of 4Eh command set to 1.
Note 2) The others are selected by using the microcontroller command.

B. Signal descriptions

Signal name	I/O	Function
MON2	O	Fixed for evaluation / Serial monitor signal output 2
MON3	O	Fixed for evaluation / Serial monitor signal output 3
BCLKIN	I	Bit clock signal input for serial data
SRDATAIN	I	Serial data signal input
LRCKIN	I	L/R identification signal input
BCLK	O	Bit clock signal output for serial data
SRDATA	O	Serial data signal output
LRCK	O	L/R identification signal output
SSYNC	O	CD-ROM sector sync signal output
DABLKCK	O	Block clock signal output after adding the track buffer
ZBLKCK	O	Interpolation block clock signal output (f=75 kHz in normal-speed playback mode)
TXNCLDCK	O	Subcode serial output sync frame clock
NCLDCK	O	Subcode frame clock signal output (f=7.35 kHz in normal-speed playback mode)
SBLKCK	O	Subcode serial output sync block clock
SUBC	O	Subcode serial output
CRC	O	Subcode CRC check result output High: OK Low: NG
RESY	O	Frame re-sync signal High: Synchronous Low: Asynchronous
FCLV	O	Frame sync detection signal High: Detection Low: No detection
BSSEL	O	PLL frequency pull-in operating signal Low: Pulling in
FLAG0	O	C1 error detection flag output signal High: Detection
IPFLAG1	O	Interpolation flag signal output High: Interpolation (synchronized with serial output only when in MSOFF.) Compatible with conventional products
IPFLAG2	O	Interpolation flag signal output High: Interpolation (synchronized with disc rotation when in MSON.)
FLAG6	O	Address reset signal for error correction de-interleave RAM Low: Address reset generated
A10	O	DRAM address A10 signal output
A11	O	DRAM address A11 signal output (available when 64M DRAM mode is used.)
NCAS1	O	CAS control signal when 16M+16M, 16M+4M, 4M+4M, or 1M+1M DRAMs are used
CLVS	O	Spindle servo operating condition output signal High: CLV Low: Rough servo
PC	O	Spindle motor ON signal output Low: ON
VDET	O	Vibration detection signal output High: Detection
NFLOCK	O	Focus servo pull-in signal Low: Pull-in state
NTLOCK	O	Tracking servo pull-in signal Low: Pull-in state
SENSE	O	Sense signal output
PCK	O	PLL extraction clock output (f=4.3218 MHz in normal-speed playback mode)
SRF	O	DSL comparator output signal
CK16M	O	16.9344-MHz clock signal output
CK8M	O	8.4672-MHz clock signal output
EXT3	O	Expansion output port 3
EXT4	O	Expansion output port 4
WAIT	O	WAIT signal output for DRAM data reading
NRQ	O	SD bit stream input request signal output
STRIN	I	SD audio bit stream serial input signal
VAL	I	SD bit stream input enable signal
EXSCK	I	SD bit stream data input clock signal

Electrical Characteristics

A. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Note
A1	Supply voltage	DRV_{DD} $IOV_{DD1,2}$ $AV_{DD1,2}$	−0.3 to +4.6	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A2	Internal supply voltage	$DV_{DD1,2,3}$	−0.3 to +4.6	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A3	Input voltage	V_I	DV_{SS}−0.3 to DRV_{DD}+0.3 DV_{SS}−0.3 to IOV_{DD}+0.3 AV_{SS}−0.3 to AV_{DD1}+0.3 AV_{SS}−0.3 to AV_{DD2}+0.3	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A4	Output voltage	V_O	DV_{SS}−0.3 to DRV_{DD}+0.3 DV_{SS}−0.3 to IOV_{DD}+0.3 AV_{SS}−0.3 to AV_{DD1}+0.3 AV_{SS}−0.3 to AV_{DD2}+0.3	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A5	Power dissipation	P_D	570	mW	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A6	Operating ambient temperature	Topr	−30 to +85	°C	
A7	Storage temperature	Tstg	−50 to +125	°C	

Note 1) The absolute maximum ratings are the limit values beyond which the IC may be broken. They do not assure operations.
Note 2) Connect each of the DV_{SS1}, DV_{SS2}, AV_{SS1}, and AV_{SS2} pins directly to ground and use at the same voltage.
Note 3) Connect each of the DRV_{DD}, IOV_{DD1}, IOV_{DD2}, AV_{DD1}, and AV_{DD2} pins directly to the specified power supply and use at the same voltage.
Note 4) DV_{DD1}, DV_{DD2}, DV_{DD3}, DRV_{DD}, IOV_{DD1}, IOV_{DD2}, AV_{DD1}, and AV_{DD2} should be powered up at the same time.
Note 5) Connect a bypass capacitor of 0.1 µF or larger between each of the power supply pins and ground.

B. OPERATING CONDITIONS

$DV_{SS1,2}$=0 V
$AV_{SS1,2}$=0 V
Topr=−30°C to +85°C

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
B1	I/O system supply voltage	$IOV_{DD1,2}$		2.2	3.3	3.6	V
B2	Digital system supply voltage	$DV_{DD1,2,3}$	MP3, WMA†: ON	1.65	1.8	2.7	V
		$DV_{DD1,2,3}$	MP3, WMA: OFF	1.50	1.8	2.7	V
B3	Audio system supply voltage	AV_{DD1}		2.7	3.3	3.6	V
B4	Analog system supply voltage	AV_{DD2}		2.7	3.3	3.6	V
B5	D-RAM interface voltage	DRV_{DD}		2.2	3.3	3.6	V

Note 6) Each operation of the digital system supply voltages, DV_{DD1}, DV_{DD2}, and DV_{DD3}, is guaranteed only when the voltages are lower than the other supply voltages, IOV_{DD1}, IOV_{DD2}, AV_{DD1}, AV_{DD2}, and DRV_{DD}.

†: WINDOWS MEDIA AUDIO (WMA)
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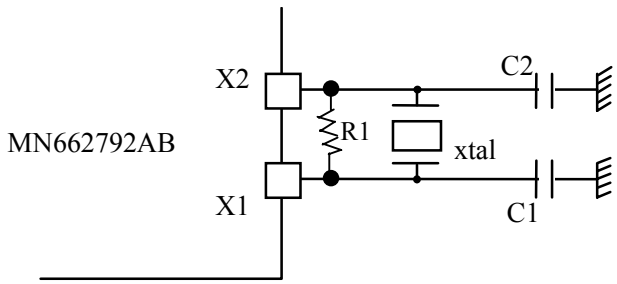
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Self-excited Oscillation 1 (Note 7)							
B6	Oscillator frequency	fxtal	16.9344-MHz Xtal		16.9344		MHz
B7	Recommended external capacitance 1	C1			47		pF
B8	Recommended external capacitance 2	C2			47		
B9	Recommended external feedback resistance	R1			470		kΩ
Self-excited Oscillation 2 (Note 7)							
B10	Oscillator frequency	fxtal	33.8688-MHz Xtal		33.8688		MHz
B11	Recommended external capacitance 1	C1			10		pF
B12	Recommended external capacitance 2	C2			10		
B13	Recommended external feedback resistance	R1			4.7		kΩ

Note 7) Oscillation circuit



Values for C1 and C2 specified above are standard values.
The appropriate capacitors' values differ according to the crystal oscillator used.
Use the values specified by the crystal oscillator manufacturer.

C. ELECTRICAL CHARACTERISTICS

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

(1) DC Characteristics

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
C1	Supply current	$I_{DD(D)}$	Anti-shock memory function used. No external load connected. (in 2x-speed playback mode) MP3 decode: OFF CD-ROM decode: OFF Digital PLL: OFF		25	50	mA
C2	I/O / analog system supply current	$I_{DD(A)}$			12	24	
C3	Total power consumption	P_T			84.6	169.2	mW
C4	Supply current	$I_{DD(D)}$	Anti-shock memory function used. No external load connected. (in 4x-speed playback mode) MP3 decode: ON CD-ROM decode: ON Digital PLL: OFF		50	100	mA
C5	I/O / analog system supply current	$I_{DD(A)}$			20	40	
C6	Total power consumption	P_T			156.0	312.0	mW
C7	Supply current	$I_{DD(D)}$	Anti-shock memory function used. No external load connected. (in 4x-speed playback mode) WMA decode: ON CD-ROM decode: ON Digital PLL: OFF		56	100	mA
C8	I/O / analog system supply current	$I_{DD(D)}$			23	40	
C9	Total power consumption	P_T			176.7	312.0	mW

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Input Pins (1) †1							
C10	High-level input voltage	V_{IH1}		2.31		3.30	V
C11	Low-level input voltage	V_{IL1}		0.00		0.99	V
C12	Input leakage current	I_{LK1}	V_{IN}=0 V or 3.3 V			±1	µA
Input Pins (2) †2							
C13	High-level input voltage	V_{IH2}		2.31		3.30	V
C14	Low-level input voltage	V_{IL2}		0.00		0.99	V
C15	Input leakage current	I_{LK2}	V_{IN}=0 V or 3.3 V			±1	µA

†1 D0, D1, D2, D3
†2 PWMSEL, TMOD2, EXT0, EXT1, EXT2, OFT, NRFDET, BDO, NTEST, MCLK, MDATA, MLD, NRST, SBCK, TXTCK

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Output Pins (1) †3							
C16	High-level output voltage	V_{OH1}	I_{OH1}=−1.0 mA	2.7			V
C17	Low-level output voltage	V_{OL1}	I_{OL1}=1.0 mA			0.4	
Output Pins (2) †4							
C18	High-level output voltage	V_{OH2}	I_{OH2}=−1.0 mA	2.7			V
C19	Low-level output voltage	V_{OL2}	I_{OL2}=1.0 mA			0.4	
Output Pins (3) †5							
C20	High-level output voltage	V_{OH3}	I_{OH3}=−1.0 mA	2.7			V
C21	Low-level output voltage	V_{OL3}	I_{OL3}=1.0 mA			0.4	
C22	Output leakage current	O_{LK3}	Hi-Z state V_O=0 V or 3.3 V			±1	µA

†3 D0, D1, NWE, NRAS, D2, D3, NCAS0, NCAS1, A8, A7, A6, A5, A4, A9, A0, A1, A2, A3, MON
†4 TRVM, TRM, FOM, LDON, FLAG, EXT0, EXT1,EXT2, TX, BLKCK, STAT, SPPOL, PMCK, SMCK, DQSY, TXTD
†5 SPOUT, TRVP, TRP, FOP

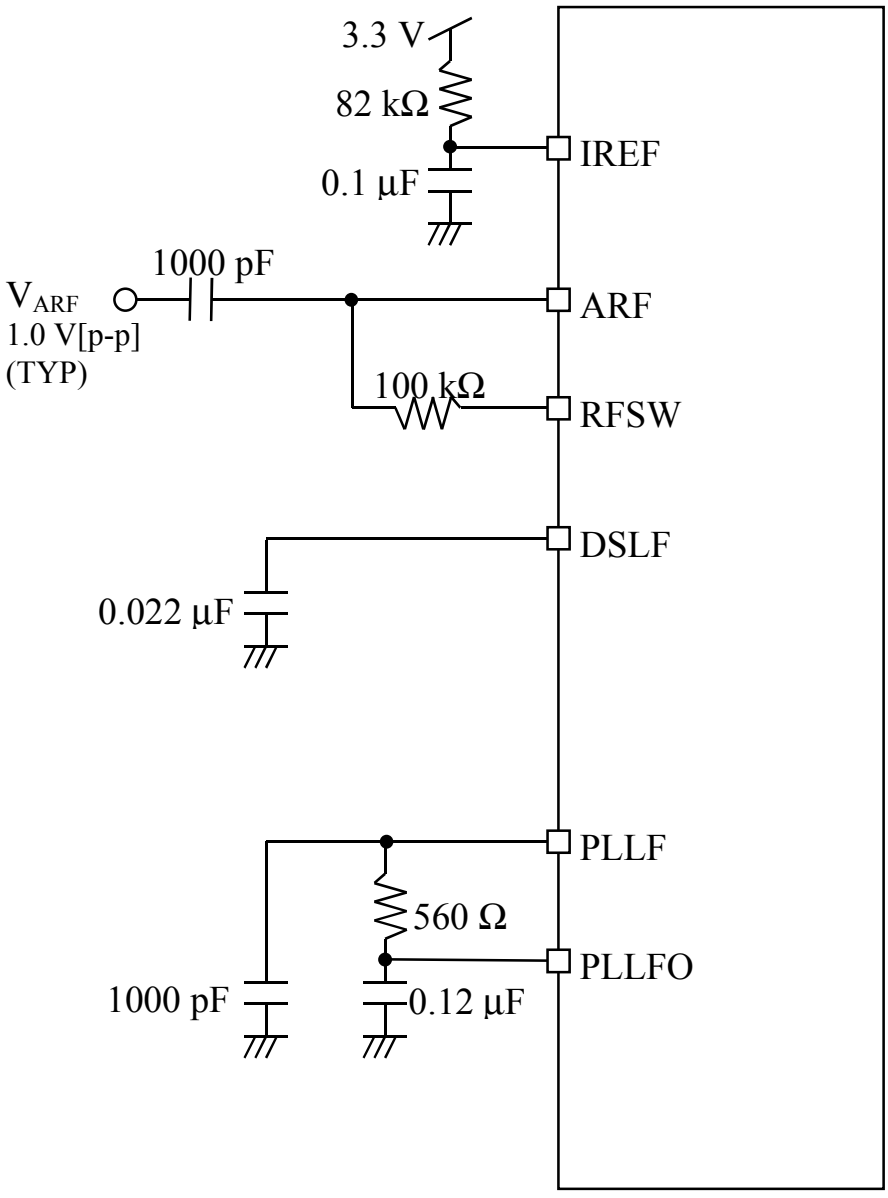
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Analog System Input Pin 1: IREF							
C23	Input current	IREF	When pulled with an 82-kΩ resistor.	19	28	37	μA
Analog System Input Pin 2: ARF							
C24	Input signal amplitude	VARF	EFM signal input level in an application circuit of DSL block.	0.5	1.0		V[p-p]
C25	Internal resistance between ARF and DSLF pins	RARF	REGSEL: R1+R2+R3 setting	65	100	135	kΩ
			REGSEL: R2+R3 setting	26	40	54	
			REGSEL: R3 setting	13	20	27	
Analog System Input Pin 3: RFSW							
C26	Input leakage current	ILKR				±1.0	μA
C27	Internal resistance between ARF and RFSW pins	RRFSW				200	kΩ
Analog System Input Pin 4: TE, FE, RFENV, ADPVCC							
C28	High-level input voltage	VIH4				2.97	V
C29	Low-level input voltage	VIL4		0.33			
A/D Converter (for servo)							
C30	Resolution	RES				8	bit
C31	Integral nonlinearity	INL	A/D output =99 to 66 (2's complement)			±2	LSB
C32	Differential nonlinearity	DNL				±3	

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Analog System Output Pin 1: DSLF (IREF pin is pulled up to AVDD2 with an 82-kΩ resistor)							
C33	Output current (N)	IDSH	BDO: Low, Tracking ON state DSLF=1.65 V	59	85	111	µA
C34	Output current (P)	IDSH	BDO: Low, Tracking ON state DSLF=1.65 V	−111	−85	−59	
C35	Output unbalance current	IDSEL	BDO: Low, Tracking ON state Normal current mode	−7	0	7	
Analog System Output Pin 2: PLLF (IREF pin is pulled up to AVDD2 with an 82-kΩ resistor)							
C36	Phase comparator output current (N)	IPFH	PLLF=1.65 V	59	85	111	µA
C37	Phase comparator output current (P)	IPFH	PLLF=1.65 V	−111	−85	−59	
C38	Input leakage current	ILKP	Hi-Z state			±1.0	
C39	Output unbalance current	IPLBL	PLLF=1.65 V	−10	0	10	
C40	VCO oscillator frequency for PLL	fVCO1		12.96		69.17	MHz
Analog System Output Pin 3: PLLFO (IREF pin is pulled up to AVDD2 with an 82-kΩ resistor)							
C41	Output current (N)	IPFHO		63	90	117	µA
C42	Output current (P)	IPFHO		−117	-90	−63	
C43	Input leakage current	ILKPO	Hi-Z state			±1.0	
Analog System Output Pin 4: TBAL, FBAL (IREF pin is pulled up to AVDD2 with an 82-kΩ resistor)							
C44	Output current (N)	IBAH	At default setting (×1)	17	25	33	µA
C45	Output current (P)	IBAL	At default setting (×1)	−33	−25	−17	

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V



Recommended Circuit for DSL and PLL Blocks

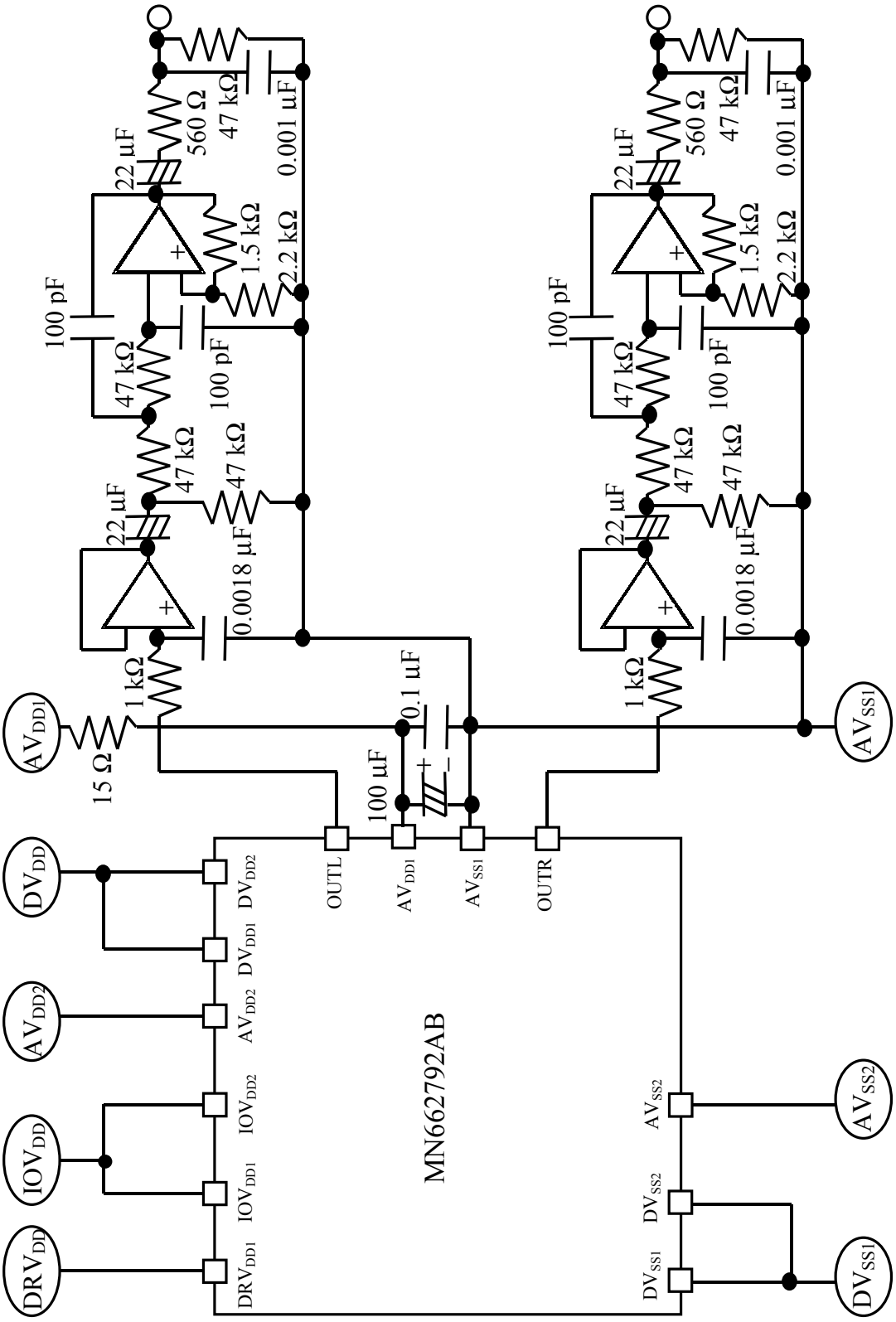
Note 8) The above is a basic circuit. Calculate the constants and other factors of the circuit in consideration of playability when making use of this circuit for actual applications.

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Converter Analog Characteristics (Notes 9 and 12)							
C43	Signal-to-noise ratio	S/N	EIAJ	90	97		dB
C44	Dynamic range	D.R.	EIAJ	80	88		dB
C45	Total harmonic distortion ratio	THD+N	EIAJ		0.02	0.04	%
C46	Crosstalk		EIAJ	70	80		dB
C47	Output level 1		1 kHz F.S. (Note 10)	1.04	1.33	1.62	Vrms
C48	Output level difference		Difference between OUT and OUTR pins at output level 20 log (V_R/V_L)	–0.99		+0.99	dB
C49	Output level 2		1 kHz F.S. (Note 11)	0.69	0.88	1.07	Vrms

Note 9) The analog characteristics show the measured values when inserting 15-Ω resistor between AV_{DD1} and power supply. The above typical values are only reference values and not guaranteed.
Note 10) The output level 1 shows the measured value at the output pin of the application circuit below.
Note 11) The output level 2 shows a value at the output pin of the IC and is calculated by taking the measured value of output level 1, dividing it by the circuit gain.
Note 12) With no anti-shock memory function used, the operation of the D/A converter will not be guaranteed in modes other than normal-speed playback.

[Application Circuit with D/A Converter]

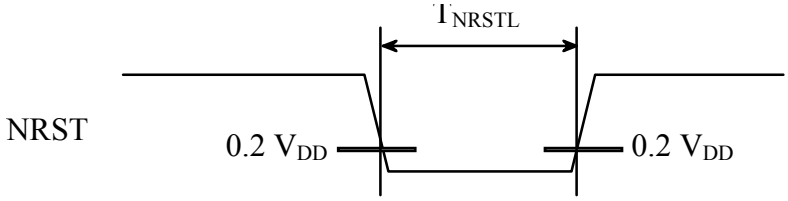


(2) AC Characteristics

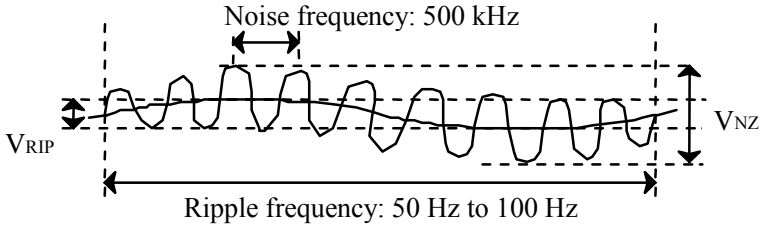
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Reset Timing (Note 13)							
C50	NRST pulse width	T_{NRSTL}		200			µs
Power Supply Ripple Noise (Note 14)							
C51	Ripple amplitude	V_{RIP}				15	mV[p-p]
C52	Ripple noise amplitude	V_{NZ}				30	mV[p-p]

Note 13) When the power is turned on, reset with the NRST pulse which is equal to or exceeds the above pulse width only after the clock oscillation is stabilized within ±10% of error of the specified oscillator frequency.



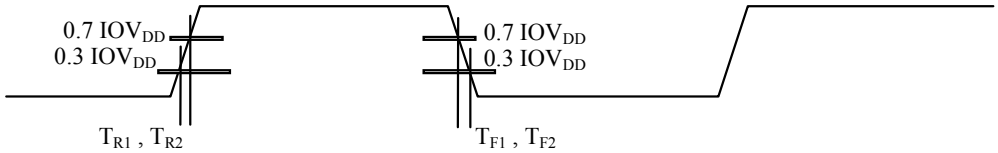
Note 14) The standard ripple noise values of the IC are guaranteed on condition that the values apply to typical 50-Hz to 100-Hz ripples with 500-kHz typical noise and that both the ripples and noise are in sine waveform as shown below.
The values, however, vary under the influence of other parts located on the PCB.
Therefore, be sure to apply the IC to practical applications and check the actual ripple noise values.



$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

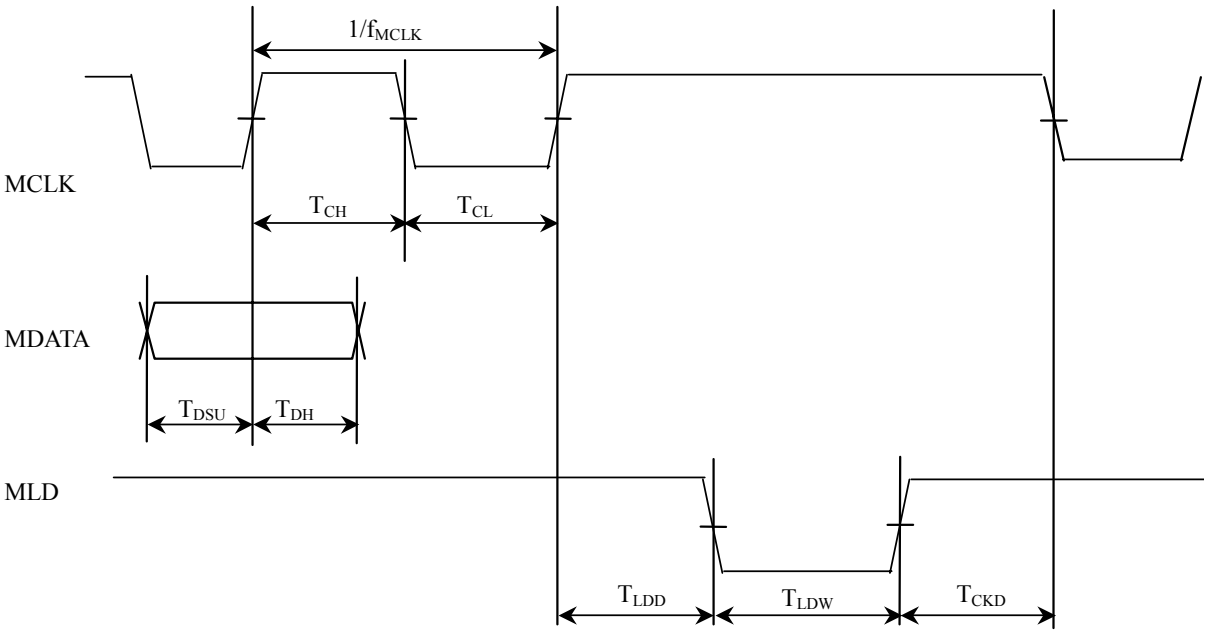
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Transition Time 1 (Note 15)							
C53	Rise time	T_{R1}				250	ns
C54	Fall time	T_{F1}				250	ns
Transition Time 2 (Note 16)							
C55	Rise time	T_{R2}				50	ns
C56	Fall time	T_{F2}				50	ns

(Note 15) MCLK, MLD
(Note 16) SBCK, TXTCK



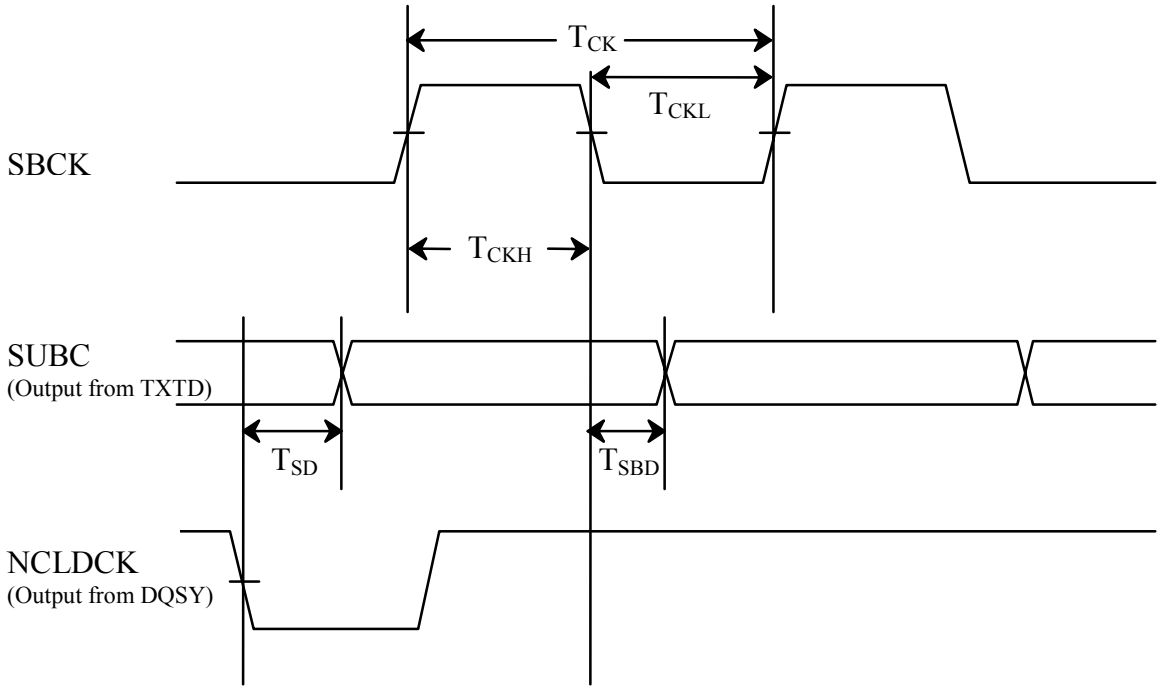
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Microcontroller Command Input Timing							
C57	Clock frequency	f_{MCLK}				1.1	MHz
C58	Clock pulse width	$T_{CH,CL}$		300			ns
C59	Data setup time	T_{DSU}		300			ns
C60	Data hold time	T_{DH}		300			ns
C61	MLD delay time	T_{LDD}		300			ns
C62	Latch pulse time	T_{LDW}		0.5		10	µs
C63	MCLK delay time	T_{CKD}		300			ns



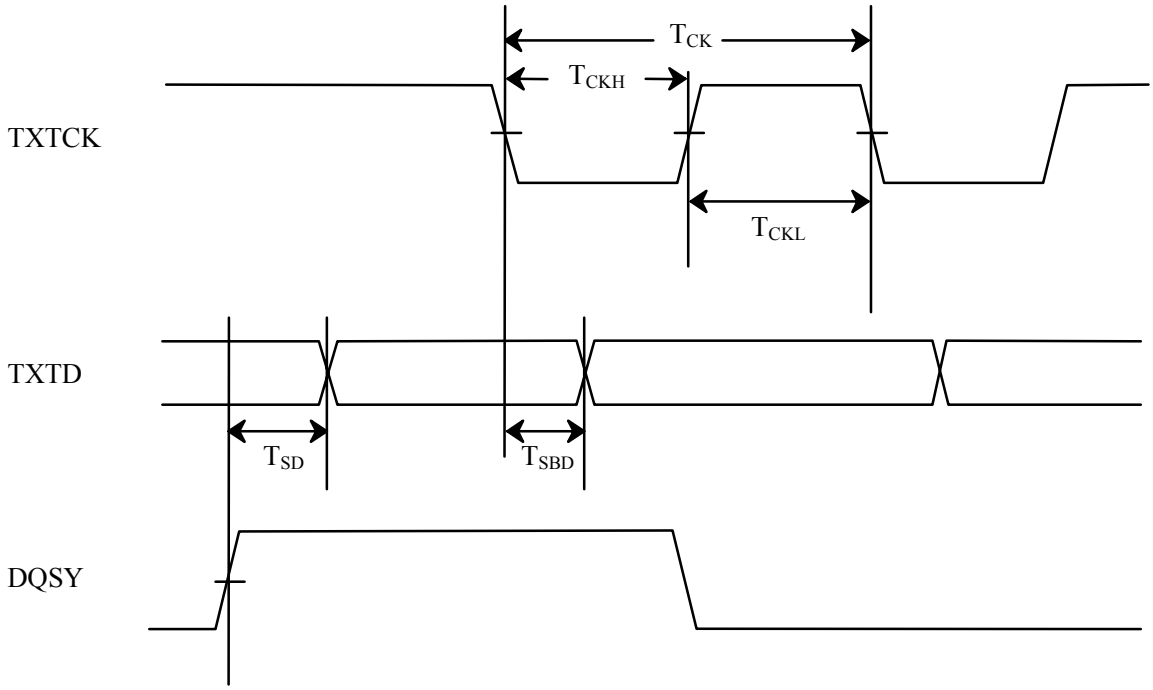
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Subcode Interface (SBCK, TXTD (SUBC), DQSY (NCLDCK))							
C64	Clock width	T_{CK}		909			ns
C65	High-level pulse width	T_{CKH}		400			ns
C66	Low-level pulse width	T_{CKL}		400			ns
C67	Delay time	T_{SBD}	When noise filter is used.			350	ns
			When no noise filter is used.			173	ns
C68	Setup delay time	T_{SD}				150	ns



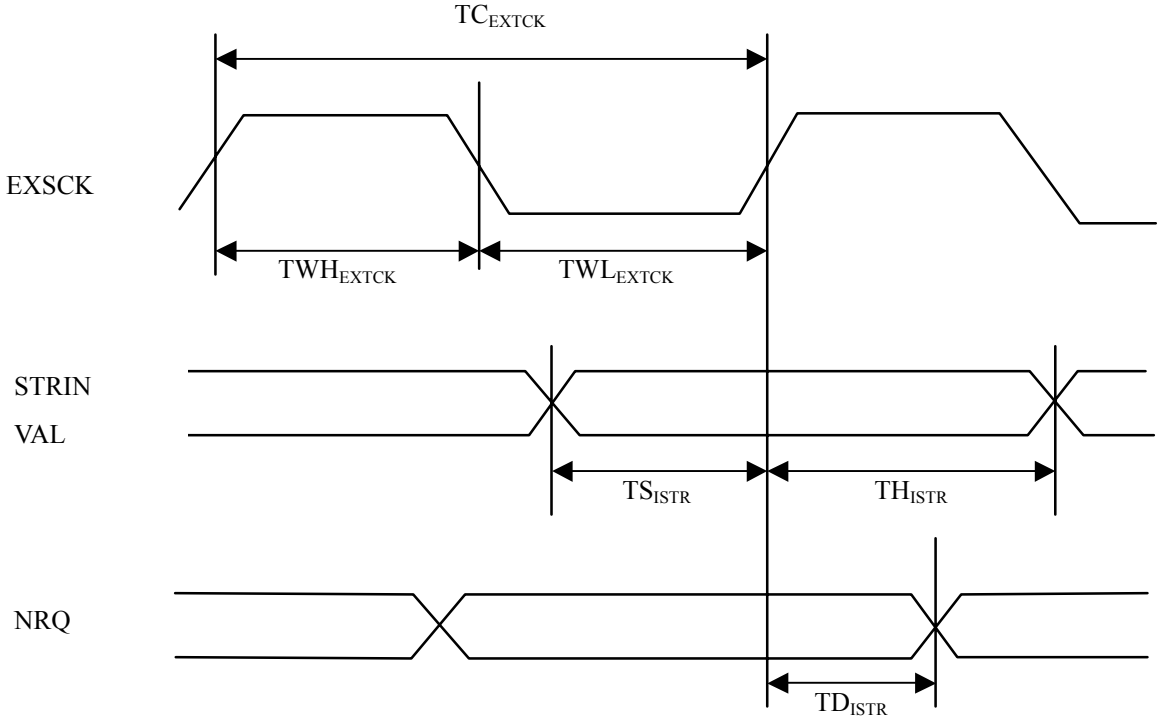
$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Subcode Interface (TXTCK, TXTD, DQSY)							
C69	Clock width	T_{CK}		2500			ns
C70	High-level pulse width	T_{CKH}		1200			ns
C71	Low-level pulse width	T_{CKL}		1200			ns
C72	Delay time	T_{SBD}				1150	ns
C73	Setup delay time	T_{SD}				1100	ns



$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

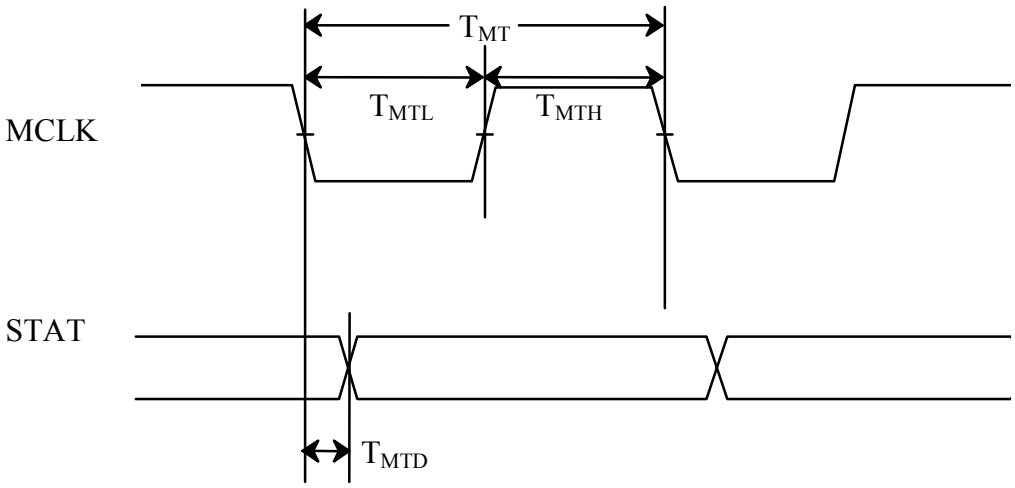
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Stream Interface (STRIN, EXSCK, VAL, NRQ)							
C74	Clock frequency	TC_{EXTCK}				10	MHz
C75	High-level pulse width	TWH_{EXTCK}		50			ns
C76	Low-level pulse width	TWL_{EXTCK}		50			ns
C77	Hold time	TH_{ISTR}		40			ns
C78	Setup time	TS_{ISTR}		10			ns
C79	Delay time	TD_{OSTR}		0			ns



(Note 17) EXSCK, STRIN, and VAL are input from EXT2 (EXSCK), EXT0 (STRIN), and VAL (EXT1) pins respectively. NRQ is output from FLAG (NRQ) pin.

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

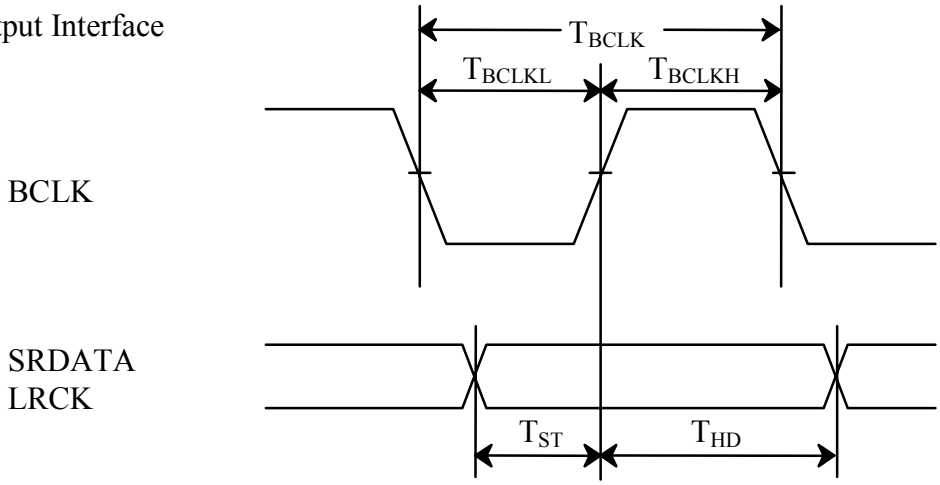
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
STAT Output Interface							
C80	Clock width	T_{MT}		909			ns
C81	High-level pulse width	T_{MTH}		400			ns
C82	Low-level pulse width	T_{MTL}		400			ns
C83	Delay time	T_{MTD}	When noise filter is used.			350	ns
			When no noise filter is used.			173	ns



$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Output Interface 1							
C84	Clock width	T_{BCLK}	In normal-speed playback mode		354		ns
C85	High-level pulse width	T_{BCLKH}			177		ns
C86	Low-level pulse width	T_{BCLKL}			177		ns
C87	Setup time	T_{ST}		70			ns
C88	Hold time	T_{HD}		70			ns
D/A Output Interface 2							
C89	Clock width	T_{BCLK}	In 4x-speed playback mode		118		ns
C90	High-level pulse width	T_{BCLKH}			59		ns
C91	Low-level pulse width	T_{BCLKL}			59		ns
C92	Setup time	T_{ST}		30			ns
C93	Hold time	T_{HD}		30			ns

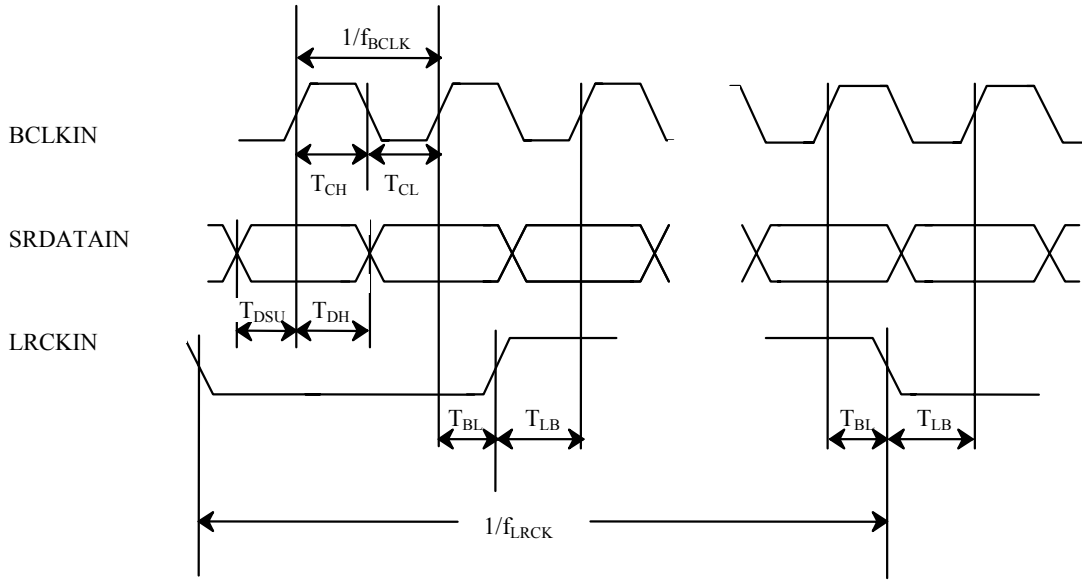
D/A Output Interface



(Note 18) SRDATA, BCLK, and LRCK are output in combination with DQSY (BCLK), TXTD (SRDATA), and TXTCK (LRCK) or EXT0 (SRDATA), EXT1 (LRCK), and EXT2 (BCLK).

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Converter Input Timing							
C94	BCLK frequency	f_{BCLK}			2.8		ns
C95	SCLK pulse width	$T_{CH,CL}$		100			ns
C96	Data setup time	T_{DSU}		100			ns
C97	Data hold time	T_{DH}		100			ns
C98	LRCK frequency	f_{LRCK}			44.1		kHz
C99	BCLK-LRCK timing	$T_{BL,}T_{LB}$		100			ns



(Note 19) SRDATAIN, LRCKIN, and BCLKIN are input from EXT0 (SRDATAIN), EXT1 (LRCKIN), EXT2 (BCLKIN) respectively.

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

(In BCKSEL=0 mode)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
DRAM Interface Read/Write Cycle							
C100	A0 to A11 row address setup time	tASR			2		cycle
C101	A0 to A11 row address hold time	tRAH			1		cycle
C102	A0 to A11 column address setup time	tASC			1		cycle
C103	A0 to A11 column address hold time	tCAH			2		cycle
C104	RAS-CAS delay time (NCAS0, NCAS1)	tRCD			2		cycle
C105	RAS access time	tRAC			4		cycle
C106	CAS access time	tCAC			2		cycle
C107	Write enable signal NWE setup time	tWCS			2		cycle
C108	Write enable signal NWE hold time	tWCH			2		cycle
C109	D0 to D3 write data setup time	tDWDS			1		cycle
C110	D0 to D3 write data hold time	tDWDH			2		cycle
DRAM Interface Page Mode Data Transfer							
C111	CAS pre-charge pulse width	tCP			1		cycle
C112	CAS low-level pulse width	tCAS			2		cycle
C113	RAS hold time	tRSH			2		cycle
DRAM Interface CAS Before RAS Refresh							
C114	CAS-RAS delay time	tCRD			1		cycle
C115	Refresh RAS low-level pulse width	tRRAS			4		cycle
C116	Refresh CAS low-level pulse width	tRCAS			5		cycle

A11 and A10 indicate the output from MON pin and NCAS1 pin respectively.
One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].
The system clock frequencies, 16.9344 MHz and 33.8688 MHz, are determined according to the IC's DRAM interface clock frequency.

$DV_{DD1,2,3}$=1.8 V, DRV_{DD}=3.3 V, $IOV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
AV_{DD1}=3.3 V, AV_{DD2}=3.3 V, $AV_{SS1,2}$=0 V

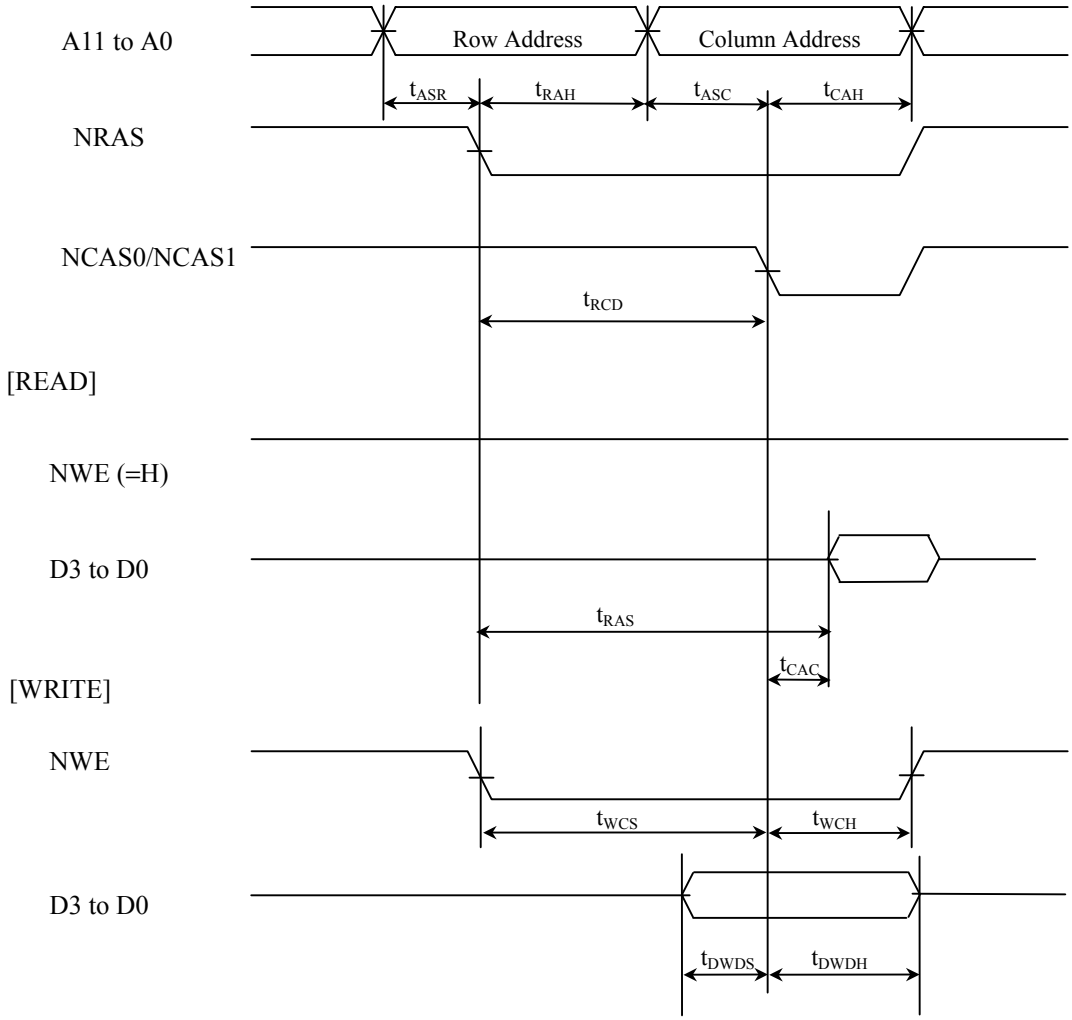
(In BCKSEL=1 mode)

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
DRAM Interface Read/Write Cycle							
C117	A0 to A11 row address setup time	tASR			2		cycle
C118	A0 to A11 row address hold time	tRAH			1		cycle
C119	A0 to A11 column address setup time	tASC			1		cycle
C120	A0 to A11 column address hold time	tCAH			1		cycle
C121	RAS-CAS delay time (NCAS0, NCAS1)	tRCD			2		cycle
C122	RAS access time	tRAC			4		cycle
C123	CAS access time	tCAC			1		cycle
C124	Write enable signal NWE setup time	tWCS			2		cycle
C125	Write enable signal NWE hold time	tWCH			1		cycle
C126	D0 to D3 write data setup time	tDWDS			1		cycle
C127	D0 to D3 write data hold time	tDWDH			1		cycle
DRAM Interface Page Mode Data Transfer							
C128	CAS pre-charge pulse width	tCP			1		cycle
C129	CAS low-level pulse width	tCAS			1		cycle
C130	RAS hold time	tRSH			1		cycle
DRAM Interface CAS Before RAS Refresh							
C131	CAS-RAS delay time	tCRD			1		cycle
C132	Refresh RAS low-level pulse width	tRRAS			4		cycle
C133	Refresh CAS low-level pulse width	tRCAS			5		cycle

A11 and A10 indicate the output from MON pin and NCAS1 pin respectively.
One cycle is the system clock cycle of 1 / (16.9344 MHz or 33.8688 MHz) [s].
The system clock frequencies, 16.9344 MHz and 33.8688 MHz, are determined according to the IC's DRAM interface clock frequency.

DRAM Access Timing (NRAS, NCAS0, NCAS1, NEW, A0 to A9, D0 to D3)

<Normal mode>



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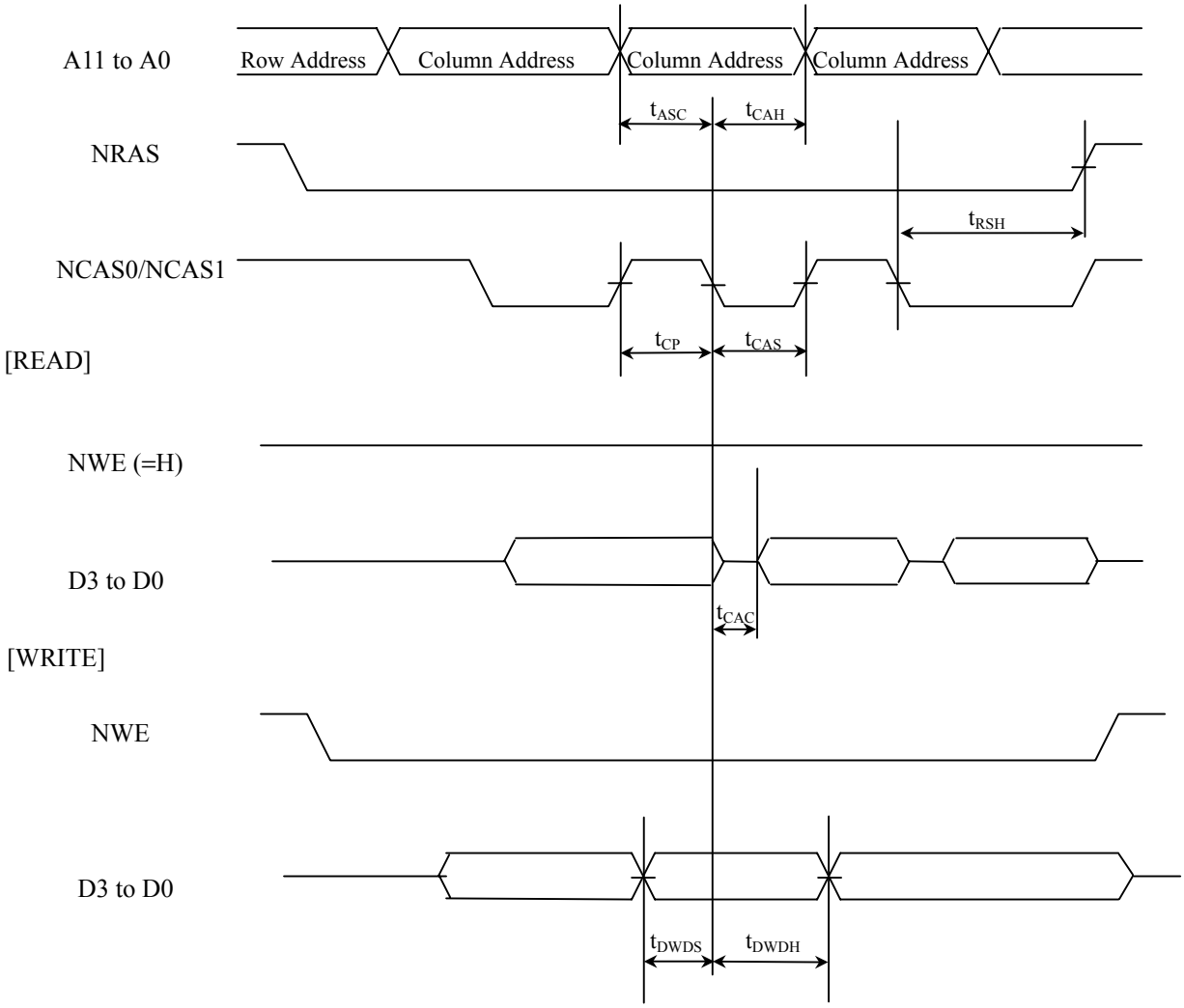
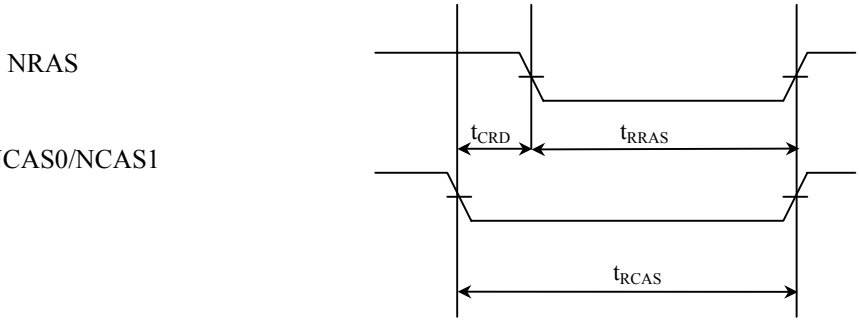


<CAS Before RAS Refresh Mode>



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(4) The products described in this material are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
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Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

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