

# MN88413

## Channel Decoder LSI for Digital Satellite Broadcast Reception

### ■ Overview

The MN88413 is a channel decoder LSI that integrates functions for digital satellite communications and broadcast reception on a single chip.

The MN88413 supports both the Digital Video Broadcast (DVB) and the Digital Satellite System (DSS®) specifications. It also supports a variable transport rate that can be set under program control using a fixed system clock frequency and can implement a channel decoder with a minimal number of external components.

### ■ Features

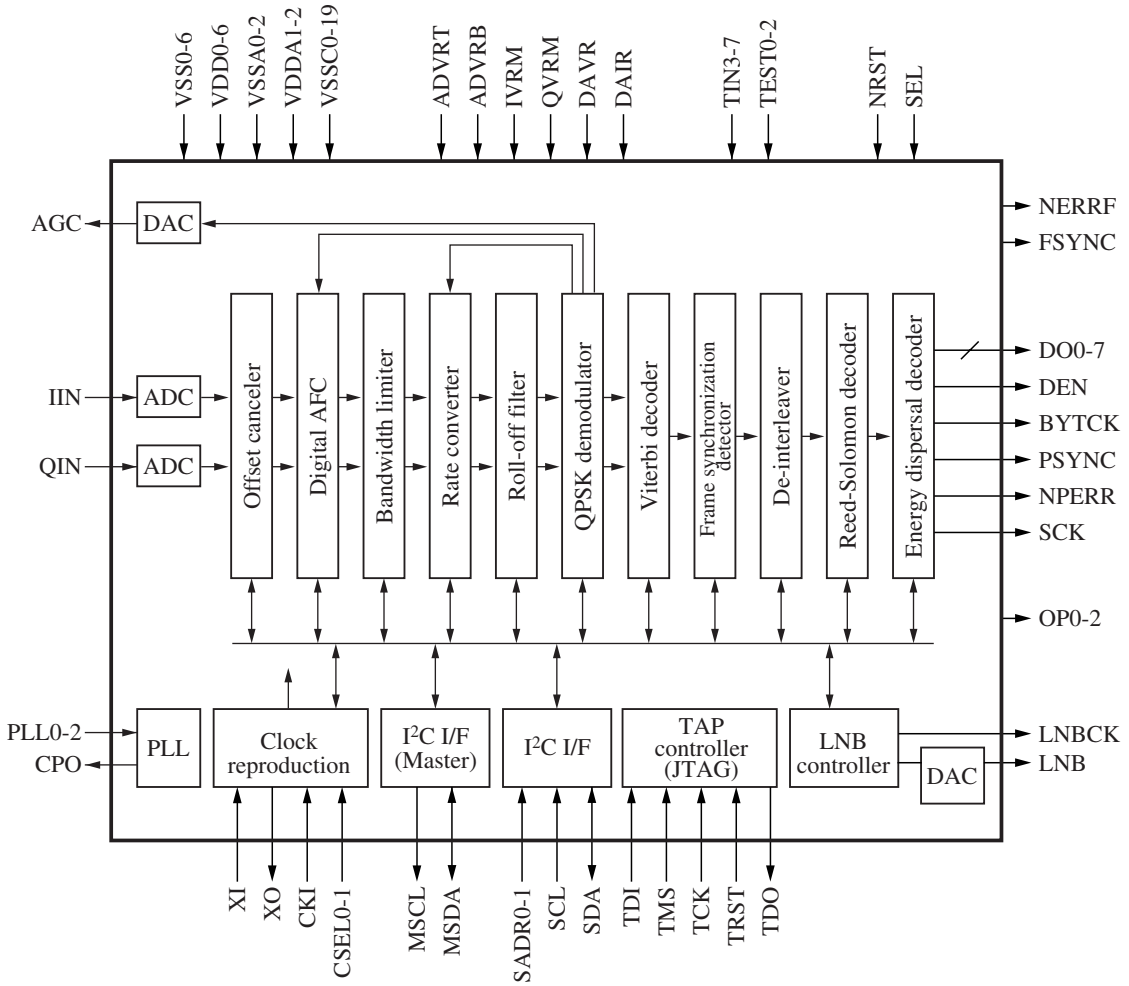
- Can be used in systems conforming to DVB, in US DIRECTV® systems, and in single carrier per channel (SCPC) communication systems.
- Integrates a 2-channel A/D converter, a variable rate QPSK demodulator, and forward error correction (FEC) on a single chip.
- Supports transfer rates from 1 Mbps to 90 Mbps.
- On-chip I/Q baseband signal offset voltage circuit and on-chip reference voltage circuit for the A/D and D/A converters.
- On-chip PLL circuit
- BER monitor function
- I<sup>2</sup>C bus master circuit for tuner control
- Supports LNB control clock and DiSEqC 1.0/1.1 and can output DiSEqC messages.
- General-purpose input and output ports
- On-chip boundary scan test circuit conforming to IEEE 1149.1

### ■ Applications

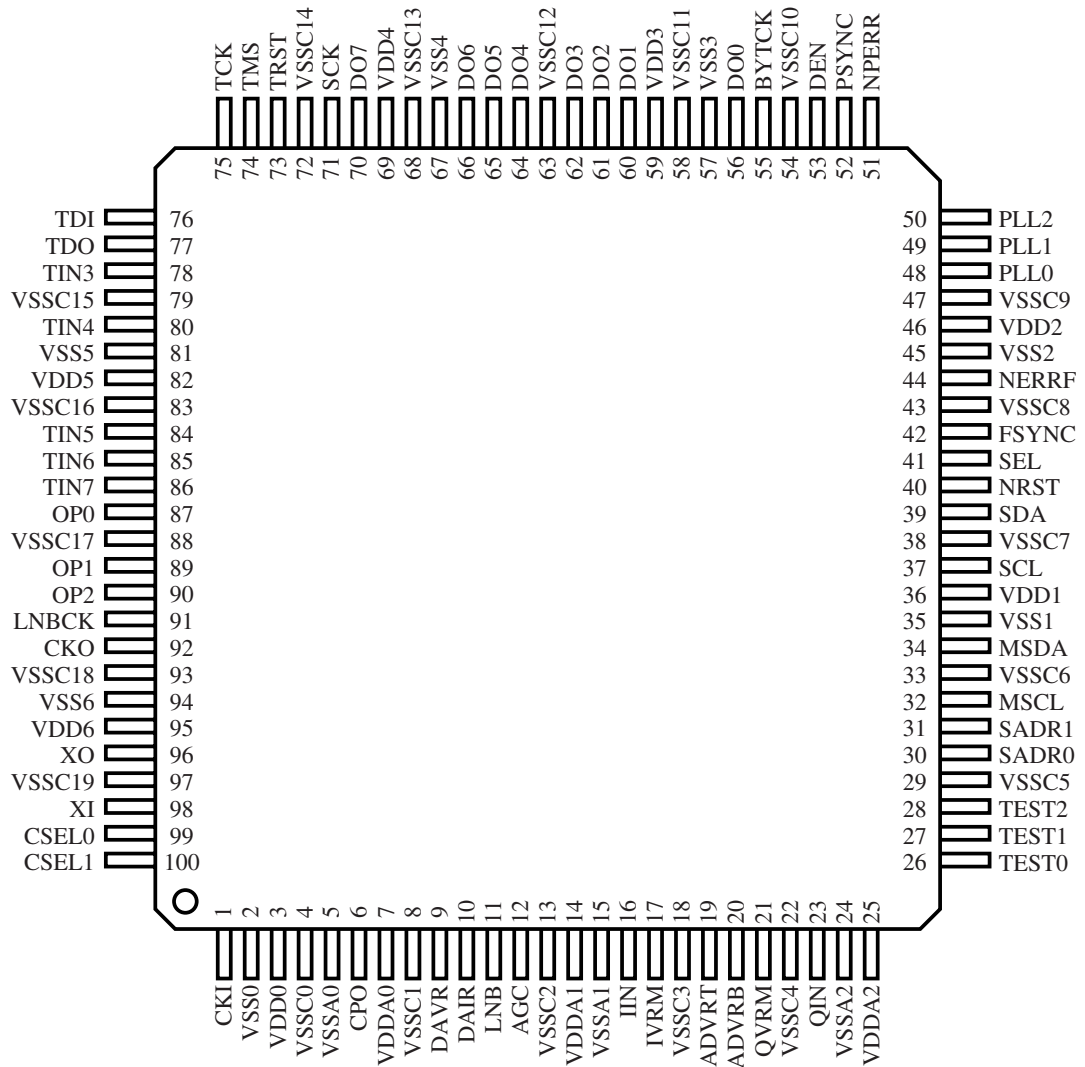
- Digital satellite broadcast receivers

Note: DSS® and DIRECTV® are registered trademarks of DIRECTV, Inc.

■ Block Diagram



■ Pin Assignment



## ■ Specifications Overview

- QPSK demodulator

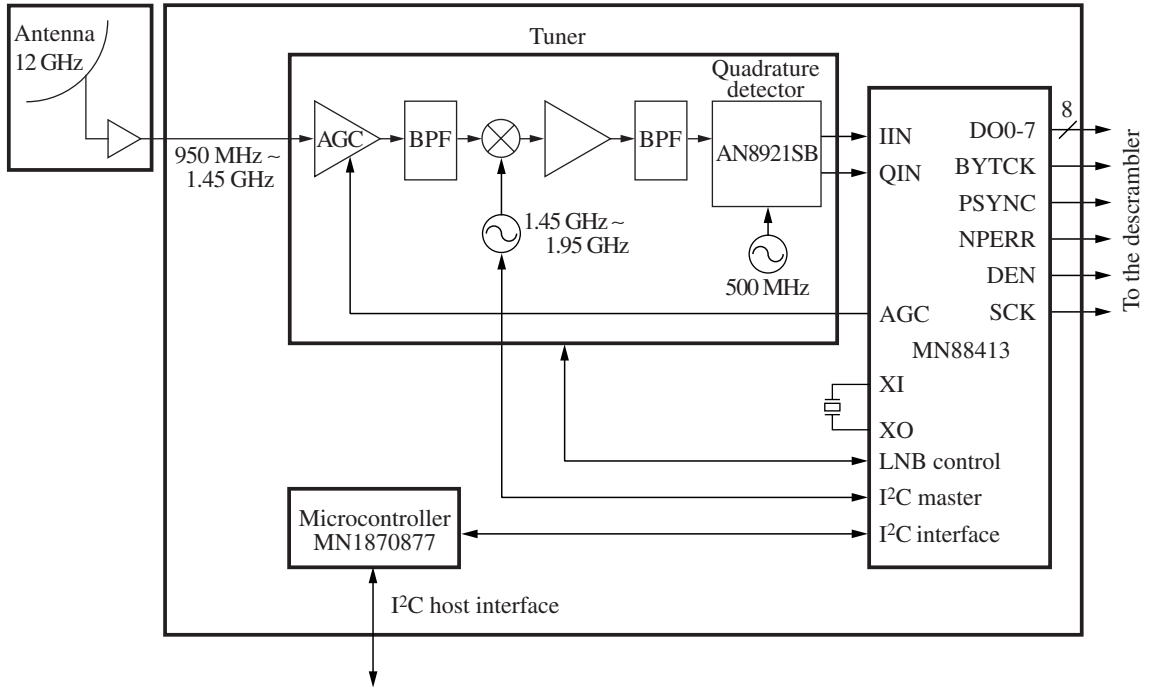
Data rate	: 1 Mbps to 90 Mbps
A/D converter resolution	: 6 bits
Linearity error	: $\pm 0.5$ LSB (typical)
Differential linearity error	: $\pm 0.5$ LSB (typical)
Input voltage level	: 1.5 V [p-p] (typical) [On-chip self-bias circuit]
Roll-off rate	: Switchable between the DVB and the DSS <sup>®</sup> specifications.
AFC range	: $\pm$ (<symbol rate>/8)
Synchronization establishment time	: 100 ms or less.

D/A converter used for LNB/AFC and AGC

Resolution	: 8 bits
Linearity error	: $\pm 0.5$ LSB (typical)
Differential linearity error	: $\pm 0.5$ LSB (typical)
Output voltage level	: 1.0 V [p-p] (typical) [0.0 V to 1.0 V]

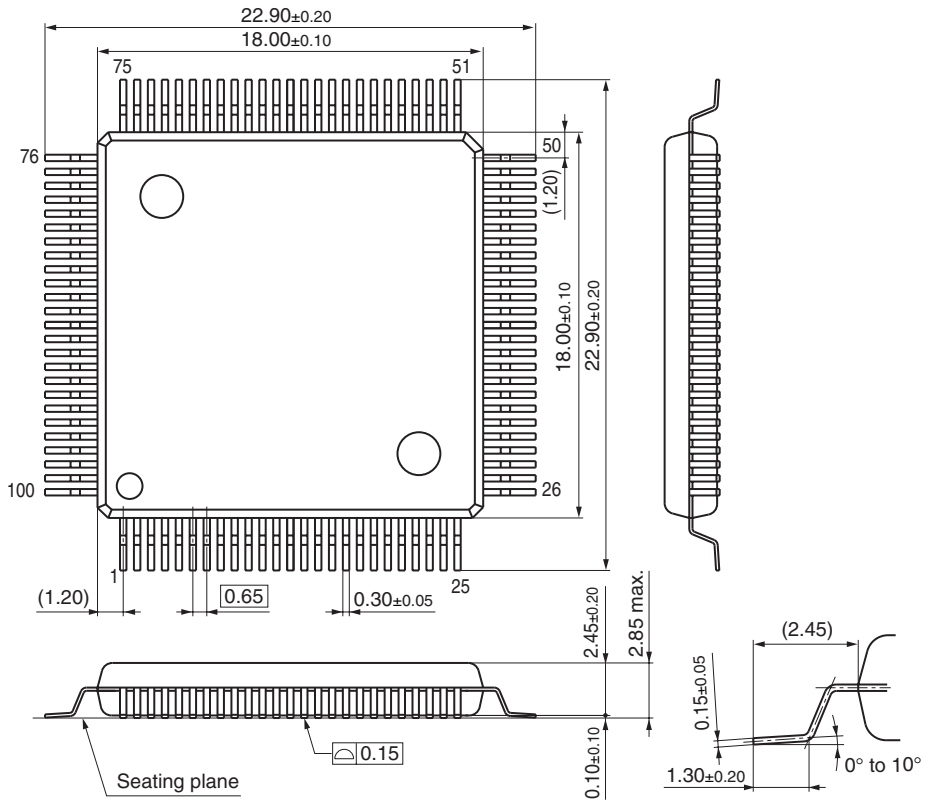
- Viterbi decoder : Switchable between the DVB and the DSS<sup>®</sup> specifications.  
: Automatic detection of encoding ratios in the range 1/2 to 7/8.  
: Auto-synchronous operation
- Frame synchronization detection, De-interleaver, Reed-Solomon decoding, and Energy dispersal  
: Switchable between the DVB and the DSS<sup>®</sup> specifications.
- PLL circuit : Reference clock input frequency: 4 MHz to 30 MHz
- CPU interface : I<sup>2</sup>C bus interface
- Supply voltage : 3.3 V  $\pm 0.165$  V
- Power dissipation : 990 mW (typical) [at VDD = 3.3 V, 60 Mbps, R = 7/8]
- Package : QFP100-P-1818B (18  $\times$  18 mm)

■ System Application Example



■ Package Dimensions (Unit: mm)

- QFP100-P-1818B (Lead-free package)



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