Freescale Semiconductor
Product Brief

MPC5534 Microcontroller Product Brief

The MPC5534 MCU is the third member of the family of next generation microcontrollers based on the PowerPC^{TM} Book E architecture. This family of parts contains many new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement over the MPC500 family.

The host processor core of the MPC5534 is compatible with the PowerPC Book E architecture. It is 100% user mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the PowerPC architecture's fit in embedded applications. This core also has additional instructions, including digital signal processing (DSP) instructions, beyond the classic PowerPC instruction set.

The host processor core of the MPC5534 also includes an instruction set enhancement allowing variable length encoding (VLE). This allows optional encoding of mixed 16- and 32-bit instructions. With this enhancement, it is possible to achieve significant code size footprint reduction.

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The MPC5534 has a single level of memory hierarchy consisting of 64-Kbyte on-chip SRAM and 1 Mbyte of internal Flash memory. Both the SRAM and the Flash memory can hold instructions and data. The External Bus Interface has been designed to support most of the standard memories used with the MPC5xx family. The MPC5534 does not support arbitration between itself and other masters on the external bus. It must be either the only master on the external bus or act as a slave-only device.

The complex I/O timer functions of MPC5534 are performed by an Enhanced Time Processor Unit engine (eTPU). The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the MPC500 family's TPU by providing 24-bit timers, double action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU can be programmed using a high-level programming language.

The less complex timer functions of MPC5534 are performed by the enchanced Modular Timer System (eMIOS). The eMIOS 24 hardware channels are capable of single action, double action, pulse width modulation (PWM) and modulus counter operation. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including CANs, enhanced SPIs (Deserialize/Serialize Peripheral Interface) and SCIs. The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and GPIO signals.

The MPC5534 MCU has an on-chip 40-channel Enhanced Queued Dual Analog-to-Digital Converter (eQADC), with 5V conversion range.

The System Integration Unit (SIU) performs several chip-wide configuration functions. Pad configuration and General-Purpose Input and Output (GPIO) are controlled from the SIU. External interrupts and reset control are also found in the SIU. The Internal Multiplexer sub-block (IMUX) provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs and external interrupt signal multiplexing.
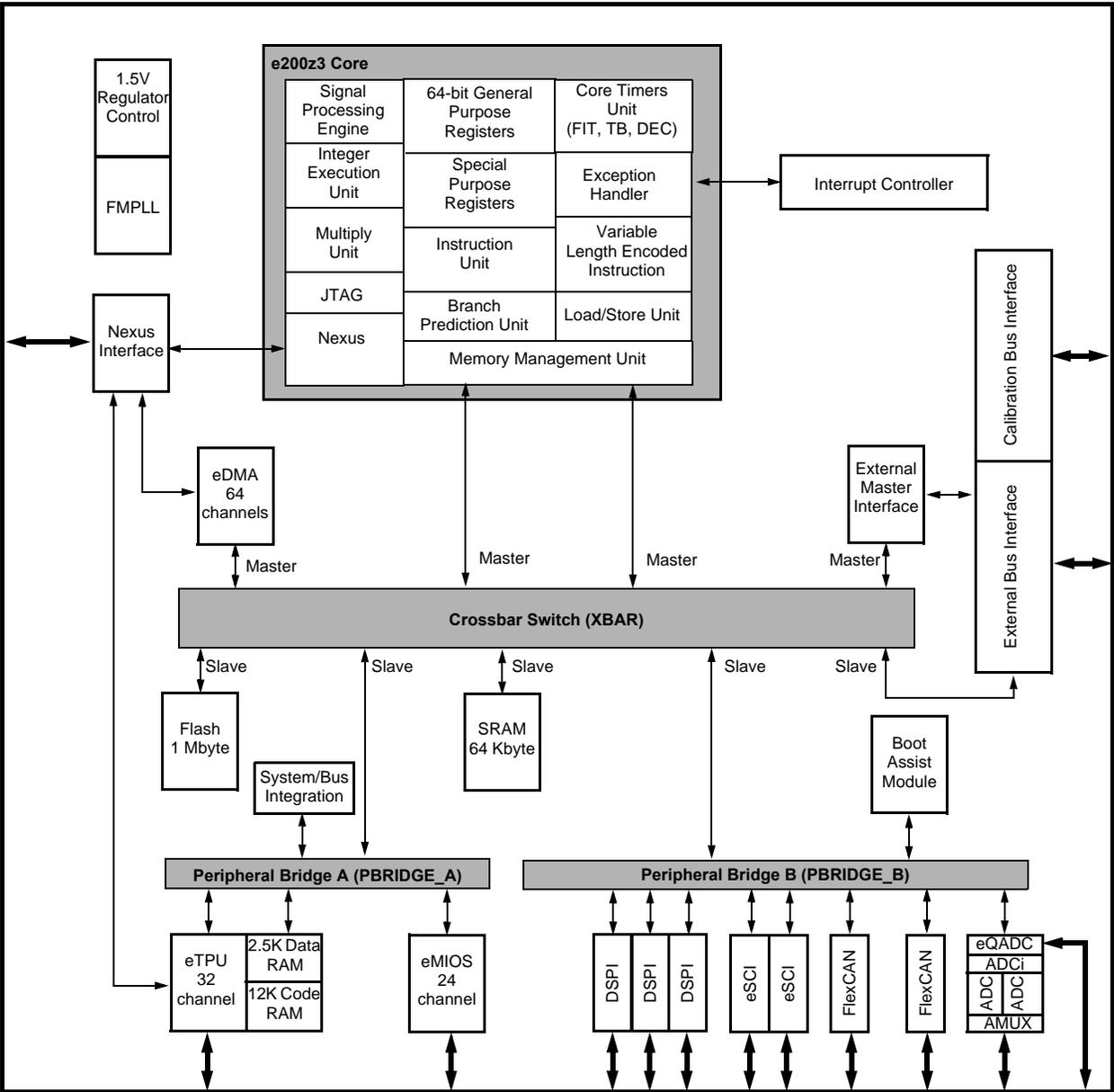
On-chip modules include:

- Single issue, 32-bit PowerPC Book E compatible CPU core complex
  — Includes VLE enhancements for code size footprint reduction
- 32-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 210 selectable-priority interrupt sources
- Frequency Modulated Phase-locked loop (PLL)
- External bus interface (EBI) with error correction status module (ECSM)
- System integration unit (SIU)
- 1-Mbyte on-chip Flash with Flash control unit (FCU)
- 64-Kbytes on-chip static RAM
- Boot assist module (BAM)
- 32-channel enhanced time processor unit (eTPU)
- 24-channels enhanced modular Input Output System (eMIOS)
- 2 Enhanced 5V queued analog-to-digital converters (eQADC)
- 3 deserial serial peripheral interface (DSPI) modules

- 2 enhanced serial communication interface (eSCI) modules (with LIN support)
- 2 controller area network (FlexCAN) modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator controller for regulating 3.3V down to 1.5V for core logic

1 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5534.

e200z3 Core

Signal Processing Engine | 64-bit General Purpose Registers | Core Timers Unit (FIT, TB, DEC)
Integer Execution Unit | Special Purpose Registers | Exception Handler
Multiply Unit | Instruction Unit | Variable Length Encoded Instruction
JTAG | Branch Prediction Unit | Load/Store Unit
Nexus | Memory Management Unit

1.5V Regulator Control

FMPLL

Nexus Interface

Interrupt Controller

Calibration Bus Interface

External Bus Interface

eDMA 64 channels

External Master Interface

Master Master Master Master

Crossbar Switch (XBAR)

Slave Slave Slave Slave Slave

Flash 1 Mbyte

SRAM 64 Kbyte

Boot Assist Module

System/Bus Integration

Peripheral Bridge A (PBRIDGE_A)

Peripheral Bridge B (PBRIDGE_B)

eTPU 32 channel

2.5K Data RAM | 12K Code RAM

eMIOS 24 channel

DSPI DSPI DSPI eSCI eSCI FlexCAN FlexCAN

eQADC
ADCi
ADC | ADC
AMUX

LEGEND

MPC5500 Device Module Acronyms

CAN	– Controller area network (FlexCAN)
DSPI	– Deserial/serial peripheral interface
DMA	– Enhanced direct memory access
eMIOS	– Enhanced modular I/O system
eQADC	– Enhanced queued analog/digital converter
eSCI	– Enhanced serial communications interface
eTPU	– Enhanced time processing units
FMPLL	– Frequency modulated phase-locked loop
SRAM	– Static RAM

e200z3 Core Component Acronyms

DEC	– Decrementer
FIT	– Fixed interval timer
TB	– Time base
WDT	– Watchdog timer

Figure 1. MPC5534 Block Diagram

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2 MPC5500 Family Comparison

Table 1. MPC5500 Family Members

MPC5500 Device		MPC5533	MPC5534	MPC5553	MPC5554
Power PC Core		e200z3	e200z3	e200z6	e200z6
Variable Length Instruction support		Yes	Yes	No	No
Cache		None	None	8k Unified[1]	32k Unified[2]
Memory Management Unit		16 entry	16 entry	32 entry	32 entry
Crossbar		4x5	4x5	4x5	3x5
Core Nexus		Class 3+ (NZ3C3)	Class 3+ (NZ3C3)	Class 3+ (NZ6C3	Class 3+ (NZ6C3)
SRAM		48k	64k	64k	64k
FLASH	Main Array	768K[3]	1M[3]	1.5M[4]	2M[4]
	Shadow Block	1K	1K	1K	1K
External bus (EBI)	Data Bus	16-bit[5]	16 bit[5]	32 bit[5]	32 bit[5]
	Address Bus	24	24	24	24
Calibration Bus		Yes	Yes	Partial	No
Direct Memory Access (DMA)		32 channel	32 channel	32 channel	64 channel
DMA Nexus		None	None	Class 3	Class 3
Serial		1	2	2	2
	eSCI_A	Yes	Yes	Yes	Yes
	eSCI_B	No	Yes	Yes	Yes
Controller Area Network (CAN)		2	2	2	3
	CAN_A	64 buf	64 buf	64 buf	64 buf
	CAN_B	No	No	No	64 buf
	CAN_C	64 buf	64 buf	64 buf	64 buf
	CAN_D	No	No	No	No
	CAN_E	No	No	No	No
SPI		2	3	3	4
	DSPI_A	No	No	No	Yes
	DSPI_B	No	Yes	Yes	Yes
	DSPI_C	Yes	Yes	Yes	Yes
	DSPI_D	Yes	Yes	Yes	Yes
eMIOS		0 channel	24 channel	24 channel	24 channel
eTPU		32 channel	32 channel	32 channel	64 channel
	eTPU_A	Yes	Yes	Yes	Yes
	eTPU_B	No	No	No	Yes
	Code memory	12k	12k	12k	16k

Table 1. MPC5500 Family Members

MPC5500 Device		MPC5533	MPC5534	MPC5553	MPC5554
eTPU (continued)					
	Parameter RAM	2.5k	2.5k	2.5k	2.5k
	Nexus	Class 3	Class 3	Class 3	Class 3
Interrupt controller		178 channel	210 channel	210 channel	300 channel
Analog to Digital Converter (eQADC)		40 channel	40 channel	40 channel	40 channel
	ADC_0	Yes	Yes	Yes	Yes
	ADC_1	No	Yes	Yes	Yes
Fast Ethernet Controller (FEC)		No	No	Yes[6]	No
FlexRay		No	No	No	No
FlexRay Nexus		No	No	No	No
Phase Lock Loop (PLL)		FM	FM	FM	FM
Voltage Regulator Controller (VRC)		Yes	Yes	Yes	Yes

NOTES:
[1] 2-way associative
[2] 8-way associative
[3] 16-Byte flash page size for programming.
[4] 32-Byte flash page size for programming.
[5] May not be externally available in some package configurations.
[6] The FEC signals are shared with Data Bus pins DATA[16:31].

3   MPC5534 Features List

This section provides a high-level description of the features found on the MPC5534.

3.1   Operating Parameters

- Fully static operation, 0 MHz - 80 MHz
- -40° to 150° C junction temperature (125° C ambient temperature)
- Low power design
  — Less than 0.8 Watts power dissipation
  — Designed for dynamic power management of core and peripherals
  — Software controlled clock gating of peripherals
  — Separate power supply for stand-by operation for a portion of SRAM
- Fabricated in 0.13 μm process
- 1.5V internal logic
- Input and output pins with 3.0V - 5.5V range

— 35%/70% V_{DDE} CMOS switch levels (with hysteresis)
— Selectable hysteresis
— Selectable slew rate control
- External bus and Nexus pins support 1.6V - 3.6V operation
— Selectable drive strength control
— Unused pins configurable as GPIO
- Designed with EMI reduction techniques
— Frequency Modulated Phase-locked loop
— On-chip bypass capacitance
— Selectable slew rate and drive strength

3.2   e200z3 Core processor

- Single issue, 32-bit PowerPC Book E compatible CPU
— In-order execution and retirement
— Precise exception handling
— User-mode binary compatible with MPC5xx except floating point instructions
- Variable Length Encoding Enhancements
— e200z3 core supports both PowerPC Book E and VLE instruction sets
— Allows optional encoding of mixed 16- and 32-bit instructions
— Results in smaller code size footprint
— Regions of the memory map are designated as PowerPC book E or VLE based on configuration of the Memory Management Unit
- Branch processing unit
— Dedicated branch address calculation adder
— Branch acceleration using Branch Lookahead Instruction Buffer
- Load/store unit
— Fully pipelined
— Big and Little endian support
— Misaligned access support
— Zero load-to-use pipeline bubbles
— Supports throughput of one load or store operation per cycle
— Memory interface support for saving and restoring two registers per cycle
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 16-entry fully-associative translation look-aside buffer (TLB)

- Separate instruction bus and load/store bus
- Vectored interrupt support
- Interrupt latency < 116ns at 80MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (CPU master only)
- Numerics and DSP
  - Saturated, unsaturated, and fractional arithmetic
  - Support for DSP addressing modes
  - Pipelined dual 32x32 MAC with 1 clock throughput
- Signal processing extension APU
  - Operating on all 32 GPRs that are all extended to 64 bits wide
  - SIMD - Single Instruction Multiple Data. Provides a full compliment of vector and scalar integer and floating point arithmetic operations (including integer vector MAC and MUL operations)
  - Provides rich array of extended 64-bit loads and stores to/from extended GPRs
  - Fully code compatible with e200z6 core
- Floating point
  - IEEE 754 compatible with software wrapper
  - Scalar single precision in hardware, double precision with software library
  - Conversion instructions between single precision floating point and fixed point
  - Fully code compatible with e200z6 core
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port

3.3   Crossbar Switch (XBAR)

- 4 master ports, 5 slave ports
  - Masters: CPU Instruction bus; CPU Load/store bus; eDMA; EBI
  - Slave: Flash; SRAM; Peripheral Bridge A; Peripheral Bridge B; EBI
- 32-bit internal address bus, 64-bit internal data bus

3.4   Enhanced direct memory access (eDMA) controller

- 32 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request

- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a "minor" byte transfer count
- An outer data transfer loop defined by a "major" iteration count
- Channel activation via one of three methods:
  — Explicit software initiation
  — Initiation via a channel-to-channel linking mechanism for continuous transfers
  — Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing
- Channel transfers can be suspended by a higher priority channel

3.5   Interrupt Controller (INTC)

- Unique 9-bit vector per interrupt source for 210 interrupt sources
- 8 software setable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

3.6   Frequency Modulated Phase-locked Loop (FMPLL)

- Input clock frequency from 8 MHz to 20 MHz
- Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to re-lock
- Four modes of operation
  — Bypass mode
  — PLL normal mode with crystal reference (default)
  — PLL normal mode with external oscillator reference
  — PLL dual controller mode for EXTAL to CLKOUT skew minimization
- Programmable frequency modulation

- — Modulation enabled/disabled through software
- — Triangle wave modulation
- — Programmable modulation depth (1% or 2% deviation from center frequency)
- — Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Programmable interrupt request on system reset or loss of lock
- Loss of clock (LOC) detection for reference and feedback clocks
- Programmable interrupt request on system reset or loss of clock
- Self-clocked mode (SCM) operation

3.7   External bus interface (EBI)

- 1.8V - 3.3V I/O
- Up to 24-bit address bus (available on 416 and 324 BGA, not available on 208 BGA)
  - — 4 most significant signals multiplexed with 4 chip selects
- 16-bit data bus (available on 416 and 324 BGA, not available on 208 BGA)
- Memory controller with support for various memory types:
  - — Synchronous burst SDR Flash and SRAM
  - — Asynchronous/legacy Flash and SRAM
- Most standard memories used with the MPC5xx family
- Burst support
- Single-master only or slave only operation
- Bus monitor
  - — User selectable
  - — Programmable time-out period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- Four chip-select (CS[0:4]) signals (Multiplexed with 4 most significant address signals)
- Two write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - — system frequency
  - — 1/2 of system frequency
  - — 1/4 of system frequency
- Configurable wait states
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)

- Selectable drive strengths through pad control in SIU; 10pF, 20pF, 30pF, 50pF

3.8 Calibration Bus

- 21-bit address bus (2 most significant signals multiplexed with 2 chip selects)(Least significant address bit is not supported - CAL_ADDR31)
- 16-bit data bus
- Memory controller with support for various memory types:
  — non-burst SDR Flash and SRAM
  — Asynchronous/legacy Flash and SRAM
  — Most standard memories used with the MPC5xx family
- Bus monitor (shared with EBI)
  — User selectable
  — Programmable timeout period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- Three chip-select (CAL_CS[0],CAL_CS[2:3]) signals (CAL_CS[2:3] multiplexed with 2 most significant address signals CAL_ADDR[10:11])
- Two write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes (shared with EBI)
  — system frequency
  — 1/2 of system frequency
  — 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations)
- Selectable drive strengths; 10pF, 20pF, 30pF, 50pF

3.9 System Integration Unit (SIU)

- System configuration
  — MCU reset configuration via external pins
  — Pad configuration control
- System reset monitoring and generation
  — Power-on reset support
  — Reset status register provides last reset source to software
  — Glitch detection on reset input
  — Software controlled reset assertion
- External interrupt

— Sixteen interrupt requests

— Rising or falling edge event detection

— Programmable digital filter for glitch rejection

- GPIO

— GPIO function on 155 I/O pins

— Dedicated input and output registers for setting each GPIO pin

- Internal Multiplexing

— Allows serial and parallel chaining of DSPIs

— Allows flexible selection of eQADC trigger inputs

— Allows selection of interrupt requests between external pins and DSPI

3.10 Error correction status module (ECSM)

- Configurable error-correcting codes (ECC) reporting

3.11 On-chip Flash

- 1 Mbyte burst Flash memory

— Configured as 64K x 128 bits

— 12 blocks (2×16K + 2×48K + 2×64K + 6×128 Kbytes) to support features such as boot block, operating system block and EEPROM emulation

— 1-Kbyte shadow row compatible with all other parts in the family for storing censorship and configuration information (censorship protection scheme to prevent Flash content visibility)

— Accessed via a 64-bit wide bus interface

- Quadruple 128-bit wide prefetch/burst buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)

- Hardware read-while-write feature that allows blocks to be erased/programmed while other blocks are being read (used for EEPROM emulation and data calibration)

- Page mode (128-bits) programming for rapid end-of-line programming

- Hardware programming state machine

- Supports a 64-bit data bus. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.

- Hardware and software configurable read and write access protections on a per-master basis.

- Interface to the Flash array controller is pipelined with a depth of 1, allowing overlapped accesses to proceed in parallel for interleaved or pipelined Flash array designs.

- Configurable access timing allowing use in a wide range of system frequencies.

- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.

- Software programmable block program/erase restriction control.
- Erase of selected block(s)
- Read page size of 128 bits (4 words)
- ECC with single-bit correction, double-bit detection.
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

3.12 On-chip static RAM (SRAM)

- Supports read/write accesses mapped to the SRAM memory from any master
- 64-Kbyte general purpose RAM of which 32 Kbytes are on standby power
- 32-Kbyte block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single bit correction, double bit detection on 32-bit data element

3.13 Boot assist module (BAM)

- Enables and manages the transition of MCU from reset to user code execution in the following configurations:
  — Execution from internal or external Flash
  — Download and execution of code via FlexCAN or eSCI
- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation
- Sets up the MMU to allow user boot code to execute as either PowerPC Book E code (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal or external Flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI
- Supports serial bootloading of either PowerPC Book E code (default) or VLE code
- Supports censorship protection for internal Flash memory
- Provides an option to enable the core watchdog timer

3.14 Enhanced modular I/O system (eMIOS)

- 24 unified channels

- Unified channel features:
  — 24-bit registers for captured/match values
  — 24-bit internal counter
  — Global prescaler
  — Separate input and output pins
  — Dedicated output pin for buffer direction control
  — Selectable time base
  — Can generate its own time base
- Four 24-bit wide counter buses
  — Counter Bus A can be shared among all unified channels and can be driven by either UC23 or by the STAC bus
  — Counter Bus B is driven by UC0, Counter Bus C is driven by UC8, Counter Bus D is driven by UC16 (then, UC0-UC7 can share Counter Bus B, UC8-UC15 can share Counter Bus C and UC16-UC23 can share Counter Bus D)
- Synchronization among internal and external time bases
- Shadow FLAG register
- State of block can be frozen for debug purposes
- Supports all DASM and PWM modes of MIOS14 (MPC5xx)
- DMA and interrupt request support
- Motor control capability

3.15 Enhanced time processor unit (eTPU)

- eTPU engine is an event triggered VLIW processor timer subsystem
- High level assembler/compiler
- 32 channels
- 24-bit timer resolution
- 12 Kbyte code memory and 2.5 Kbyte data memory
- Variable number of parameters allocatable per channel
- Double match/capture channels
- Angle clock hardware support
- Shared time or angle counter bus (STAC) for all eTPU and eMIOS channels
- DMA and interrupt request support
- Nexus Class 3 Debug support (with some Class 4 support)

3.16 Enhanced queued A/D converter (eQADC)

- Two independent ADCs

- — 12 Bit AD Resolution

- — Up to 10 bit accuracy at 400 ksample/s and 8 bit accuracy at 800 ksample/s

- — Differential conversions

- — Single-ended signal range from 0 to 5V

- — Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

- — Provides time stamp information when requested

- — Parallel interface to eQADC CFIFOs and RFIFOs

- — Supports both right-justified unsigned and signed formats for conversion results

- 0 - 5V common mode conversion range

- 40 single ended inputs channels (40 in 416 BGA; 40 in 324 BGA; 34 in 208 BGA), with support for up to 25 additional channels using external multiplexers (on all packages)

- 8 channels can be used as 4 pairs of differential analog input channels

- 10 bit accuracy at 400 ksample/s, 8 bit accuracy at 800 ksample/s

- Supports six FIFO queues with fixed priority.

- Queue modes with priority-based preemption, initiated by software command or internal (eTPU and eMIOS) or external triggers

- DMA and interrupt request support

- Supports all functional modes from QADC (MPC5xx family)

- 4 pairs of differential analog input channels

- Full duplex synchronous serial interface (SSI) to an external device

- — Free-running clock for use by an external device

- — Supports a 26-bit message length

- Priority based CFIFOs

- — Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first

- — Supports software and hardware trigger modes to arm a particular CFIFO

- — Generates interrupt when command coherency is not achieved

- External hardware triggers

- — Supports rising edge, falling edge, high level and low level triggers

- — Supports configurable digital filter

- Supports 4 external 8-to-1 muxes which can expand the input channels

3.17 Deserial serial peripheral interface module (DSPI)

- 3 DSPI modules

- SPI

— Full duplex communication ports with interrupt and DMA request support

— Supports all functional modes from QSPI sub-block of QSMCM (MPC5xx family)

— Support for queues in RAM

— 6 chip selects, expandable to 64 with external demultiplexers

— Programmable frame size, baud rate, clock delay and clock phase on a per frame basis

— Modified SPI mode for interfacing to peripherals with longer setup time requirements

- Deserial serial interface (DSI)

   — Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels

   — Chaining of DSI sub-blocks

   — Triggered transfer control and change in data transfer control (for reduced EMI)

3.18 Enhanced serial communication interface (eSCI) module

- 2 eSCI modules
- UART mode provides NRZ format and half or full duplex interface
- eSCI bit rate up to 1 Mbps
- Advanced error detection, and optional parity generation and detection
- Separately enabled transmitter and receiver
- eDMA support (on one of the eSCI modules only)
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit word length (data format)
- LIN support
   — Autonomous transmission of entire frames
   — Configurable to support all revisions of the LIN standard
   — Automatic parity bit generation
   — Double stop bit after bit error
   — 10-bit or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- Two receiver wake-up methods, idle line and address mark
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- 2 channel eDMA interface

3.19 FlexCAN

- 2 FlexCAN modules
- 64 message buffers each (0 to 8 bytes data length)
- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
  — Standard data and remote frames
  — Extended data and remote frames
  — Zero to eight bytes data length
  — Programmable bit rate up to 1 Mb/sec
- Programmable acceptance filters
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen only mode capabilities
- Programmable clock source: system clock or oscillator clock
- Content-related addressing
- Each MB configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1056 bytes of embedded memory for MB storage
- Programmable loop-back mode supporting self-test operation
- Three programmable Mask Registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

3.20 Nexus development interface (NDI)

- Per IEEE-ISTO 5001-2003
- Real time development support for e200z3 core and eTPU engine through Nexus Class 3 (selected Class 4 support)
- Read and write access
  — Run-time access of entire memory map

— Calibration (table constants calibrated using MMU and internal and external RAM; scalar constants calibrated using cache line locking)

- Configured via the IEEE 1149.1 (JTAG) port

- High bandwidth mode for fast message transmission

- Reduced bandwidth mode for reduced pin usage

3.21 IEEE 1149.1 JTAG controller (JTAGC)

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)

- A JCOMP input that provides the ability to share the TAP (selectable modes of operation include JTAGC/debug or normal system operation)

- Selectable modes of operation include JTAGC/debug or normal system operation.

- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:

  — BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP

- A 5-bit instruction register that supports the additional following public instructions:

  — ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE, ACCESS_AUX_TAP_eTPU

- Three test data registers: a bypass register, a boundary scan register, and a device identification register

- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

3.22 On-chip Voltage Regulator Controller

- Uses external NPN bipolar transistor

- Regulates 3.3V down to 1.5V for the core logic

4   MPC5534 Memory Map

This section describes the MPC5534 memory map. All addresses in the device, including those that are reserved, are identified in the tables. The addresses represent the physical addresses assigned to each IP block. Logical addresses are translated by the MMU into physical addresses.

Under software control of the Memory Management Unit (MMU), the logical addresses allocated to IP blocks may be changed on a minimum of a 4-Kbyte boundary. Table 2 shows the MPC5534 memory map.

Table 2. MPC5534 Memory Map

Address Range[1]	Allocated Size (bytes)	Used Size (bytes)	Use
0x0000_0000 - 0x000F_FFFF	1 M	1 M	Flash Array
0x0010_0000 - 0x00FF_FBFF	15 M	N/A	Reserved
0x00FF_FC00 - 0x00FF_FFFF	1 K	1 K	Flash Shadow Block

Table 2. MPC5534 Memory Map

0x0100_0000 - 0x1FFF_FFFF	496 M	1 M	Emulation mapping of Flash Array
0x2000_0000 - 0x3FFF_FFFF	256 M	N/A	External Memory[2]
0x4000_0000 - 0x4000_7FFF	32 K	32 K	SRAM Array, Standby Powered
0x4000_8000 - 0x4000_FFFF	32 K	32 K	SRAM Array
0x4001_0000 - 0xBFFF_FFFF	(2048 M - 64 K)	N/A	Reserved
Bridge A Peripherals			
0xC000_0000 - 0xC3EF_FFFF	63 M	N/A	Reserved
0xC3F0_0000 - 0xC3F0_3FFF	16 K	4	Bridge A Registers
0xC3F0_4000 - 0xC3F7_FFFF	496K	N/A	Reserved
0xC3F8_0000 - 0xC3F8_3FFF	16 K	20	FMPLL
0xC3F8_4000 - 0xC3F8_7FFF	16 K	48	External Bus Interface (EBI) Configuration
0xC3F8_8000 - 0xC3F8_BFFF	16 K	28	Flash Configuration
0xC3F8_C000 - 0xC3F8_FFFF	16 K	N/A	Reserved
0xC3F9_0000 - 0xC3F9_3FFF	16 K	2.5 K	System Integration Unit (SIU)
0xC3F9_4000 - 0xC3F9_FFFF	48 K	N/A	Reserved
0xC3FA_0000 - 0xC3FA_3FFF	16 K	1056	Modular Timer System (eMIOS)
0xC3FA_4000 - 0xC3FB_FFFF	112 K	N/A	Reserved
0xC3FC_0000 - 0xC3FC_3FFF	16 K	3 K	Enhanced Time Processing Unit (eTPU) Registers
0xC3FC_4000 - 0xC3FC_7FFF	16 K	N/A	Reserved
0xC3FC_8000 - 0xC3FC_BFFF	16 K	2.5 K	eTPU Parameter RAM
0xC3FC_C000 - 0xC3FC_FFFF	16 K	2.5 K	eTPU Parameter RAM mirror
0xC3FD_0000 - 0xC3FD_3FFF	16 K	12 K	eTPU Code RAM
0xC3FD_4000 - 0xC3FF_FFFF	176 k	N/A	Reserved
0xC400_0000 - 0xDFFF_FFFF	(512 M - 64 M)	N/A	Reserved
Bridge B Peripherals			
0xE000_0000 - 0xFBFF_FFFF	(512 M - 64 M)	N/A	Reserved
0xFC00_0000 - 0xFFEF_FFFF	63 M	N/A	Reserved
0xFFF0_0000 - 0xFFF0_3FFF	16 K	N/A	Bridge B Registers
0xFFF0_4000 - 0xFFF0_7FFF	16 K	N/A	Crossbar (XBAR)
0xFFF0_8000 - 0xFFF0_FFFF	32 K	N/A	Reserved
0xFFF1_0000 - 0xFFF3_FFFF	192 K	N/A	Reserved
0xFFF4_0000 - 0xFFF4_3FFF	16 K	N/A	MCM
0xFFF4_4000 - 0xFFF4_7FFF	16 K	N/A	DMA Controller 2 (eDMA)
0xFFF4_8000 - 0xFFF4_BFFF	16 K	N/A	Interrupt Controller (INTC)
0xFFF4_C000 - 0xFFF4_FFFF	16 K	N/A	Reserved

Table 2. MPC5534 Memory Map

0xFFF5_0000 - 0xFFF7_FFFF	192 K	N/A	Reserved
0xFFF8_0000 - 0xFFF8_3FFF	16 K	164	Enhanced Queued Analog to Digital Converter (eQADC)
0xFFF8_4000 - 0xFFF9_3FFF	64 K	N/A	Reserved
0xFFF9_4000 - 0xFFF9_7FFF	16 K	200	Deserial Serial Peripheral Interface (DSPI_B)
0xFFF9_8000 - 0xFFF9_BFFF	16 K	200	Deserial Serial Peripheral Interface (DSPI_C)
0xFFF9_C000 - 0xFFF9_FFFF	16 K	200	Deserial Serial Peripheral Interface (DSPI_D)
0xFFFA_0000 - 0xFFFA_FFFF	64 K	N/A	Reserved
0xFFFB_0000 - 0xFFFB_3FFF	16 K	44	Serial Communications Interface (SCI_A)
0xFFFB_4000 - 0xFFFB_7FFF	16 K	44	Serial Communications Interface (SCI_B)
0xFFFB_8000 - 0xFFFB_FFFF	32 K	N/A	Reserved
0xFFFC_0000 - 0xFFFC_3FFF	16 K	1152	Controller Area Network (FlexCAN_A)
0xFFFC_4000 - 0xFFFC_7FFF	16 K	1152	Reserved
0xFFFC_8000 - 0xFFFC_BFFF	16 K	1152	Controller Area Network (FlexCAN_C)
0xFFFC_C000 - 0xFFFF_BFFF	192 K	N/A	Reserved
0xFFFF_C000 - 0xFFFF_FFFF	16 K	4 K	Boot Assist Module (BAM)

NOTES:
[1] If allocated size > used size, then the base address for the block is the lowest address of the listed address range, unless noted otherwise.

[2] It is recommneded that the address rage of 0x3000_0000 through 0x3FFF_FFFF be reserved for use by the calibration bus.

Peripheral blocks may be redundantly mapped. The customer must use the MMU to prevent corruption.

4.1   External Master Mode Operation Memory Map

When the MPC5534 MCU acts as a slave from an external master device, the External Bus Interface (EBI) translates the 24-bit external address to a 32-bit internal address. Table 3 lists the translation parameters.

Table 3. External to Internal Memory Map Translation Table for Slave Mode

Ext addr[8:11][1]	Internal addr[0:11]	Size (bytes)	Internal Slave	Internal Address Range
0b0xxx	N/A	8 M	N/A	N/A - Reserved for off-chip access
0b10xx	0b0000_0000_00xx	4 M	Internal Flash	0x0000_0000 - 0x003F_FFFF
0b1100	0b0100_0000_0000	1 M	SRAM	0x4000_0000 - 0x400F_FFFF
0b1101	0b0110_0000_0000	1 M	Reserved[2]	0x6000_0000 - 0x600F_FFFF
0b1110	0b1100_0011_1111	1 M	Bridge A Peripherals	0xC3F0_0000 - 0xC3FF_FFFF
0b1111	0b1111_1111_1111	1 M	Bridge B Peripherals	0xFFF0_0000 - 0xFFFF_FFFF

NOTES:
[1] Only the lower 24 address signals (addr[8:31]) are available off-chip.

[2] Reserved for a future block that requires its own crossbar slave port.

Table 4 shows the memory map for a MPC5534 MCU acting as a slave from the point of view of the external master.

Table 4. MPC5534 Slave Memory Map as seen from an External Master

External Address Range[1]	Size (bytes)	Use
0x00_0000[2] - 0x7F_FFFF	8 M	N/A - Used for off-chip memory accesses
0x80_0000 - 0x8F_FFFF	1 M	Slave Flash[3]
0x90_0000 - 0xBF_FFFF	3 M	Reserved
0xC0_0000 - 0xC0_FFFF	64 K	Slave SRAM
0xC1_0000 - 0xCF_FFFF	(1 M - 64 K)	Reserved
0xD0_0000 - 0xCF_FFFF	1 M	Reserved
0xE0_0000 - 0xEF_FFFF	1 M	Slave Bridge A Peripherals
0xF0_0000 - 0xFF_FFFF	1 M	Slave Bridge B Peripherals

NOTES:
[1] Only the lower 24 address signals (addr[8:31]) are available off-chip.
[2] This address range is not part of the MPC5534 slave memory map, rather it is shown to illustrate the addressing scheme for off-chip accesses when the MPC5534 is operating in slave mode.
[3] The shadow row of the Slave Flash is not accessible by an External Master

5 Detailed Features

The following sections provided detailed information about each of the on-chip modules.

5.1 e200z3 Core Overview

The e200z3 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32x32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or

not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

 Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the PowerPC architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified storage model for single-precision floating-point data types of 32-bits and the normal integer type. Single-cycle floating-point add, subtract, multiply, compare, and conversion operations are provided. Divide instructions are multi-cycle and are not pipelined.

The Signal Processing Extension (SPE) Auxiliary Processing Unit (APU) provides hardware SIMD operations and supports a full compliment of dual integer arithmetic operation including Multiply Accumulate (MAC) and dual integer multiply (MUL) in a pipelined fashion. The general purpose register file is enhanced such that all 32 of the GPRs are extended to 64 bits wide and are used for source and destination operands, thus there is a unified storage model for 32 x 32 MAC operations which generate greater than 32 bit results.

The majority of both scalar and vector operations (including MAC and MUL) are executed in a single clock cycle. Both Scalar and Vector divides take multiple clocks. The SPE APU also provides extended load and store operations to support the transfer of data to and from the extended 64 bit GPRs. This SPE APU is fully binary compatible with the e200z6 SPE APU used in MPC5554 and MPC5553.

The CPU includes support for variable length encoding (VLE) instruction enhancements. This allows the optional execution of an alternate instruction set consisting of a mixture of 16-bit and 32-bit instructions. This results in a significantly smaller code size footprint without affecting performance noticeably. The e200z3 core supports both the PowerPC Book E and VLE instruction sets.

5.2   Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and five slave ports.

- Four master ports:
  — Core CPU - Instruction
  — Core CPU - Data
  — eDMA
  — EBI
- Five slave ports
  — Flash (64-bit data access)
  — EBI (64-bit data access)
  — SRAM (64-bit data access)
  — Peripheral Bridge A (32-bit data access)
  — Peripheral Bridge B (32-bit data access)

The crossbar allows for concurrent transactions to occur from any master port to any slave port. It is possible for all master ports and slave ports to be in use at the same time as a result of independent master requests. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. By default, requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

5.3   Enhanced direct memory access (eDMA) controller

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 32 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

5.4   Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC allows interrupt request servicing from up to 210 interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the

execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

5.5   Frequency Modulated PLL (FMPLL)

The frequency modulated PLL allows the user to generate high speed system clocks from an 8MHz to 20MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio, modulation depth, and modulation rate are all software configurable.

5.6   External Bus Interface (EBI)

The EBI controls data transfer across the crossbar switch to/from memories or peripherals in the external address space. The EBI is only available on the 324 and 416 BGA packages. The EBI includes a memory controller that generates interface signals to support a variety of external memories. The EBI memory controller supports single data rate (SDR) burst mode Flash, SRAM, and asynchronous memories. In addition, the EBI supports up to 4 regions via chip selects (multiplexed with 4 address bits), along with programmed region-specific attributes.

5.7   Calibration Bus (cal_bus)

The Cal Bus controls data transfer across the crossbar switch to/from memories or peripherals connected to the *VertiCal* connector. The cal_bus is only available when the silicon is packaged in the *VertiCal* calibration system. The cal_bus shares the memory controller and most of the control logic with the EBI but the two buses come out on two completely independant sets of pads. The cal_bus memory controller supports single data rate (SDR) non-burst mode Flash, SRAM, and asynchronous memories. In addition, the cal_bus supports up to 3 regions via dedicated calibration chip selects (2 chip selects multiplexed with 2 address bits), along with programmed region-specific attributes.

5.8   System Integration Unit (SIU)

The SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O

pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the RSTOUT pin. The SIU is accessed by the e200z3 core through the crossbar switch.

For more information on configuring the MPC5534 at reset see Section 6, "Chip Configuration," on page 30.

5.9   On-chip Flash

The MPC5534 provides 1 Mbyte of programmable, non-volatile, Flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The Flash module interfaces the system bus to a dedicated Flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to Flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the Flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal Flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and may be restricted to servicing a single bus master. Prefetches may also be restricted to being triggered for instruction or data accesses.

5.10   SRAM

The MPC5534 SRAM module provides a general-purpose 64-Kbyte memory block. The first 32K block of the SRAM is powered by its own power supply pin, called VSTBY. This allows the contents of this memory region to be preserved when the rest of the MCU is powered down.

ECC handling is done on a 32-bit boundary and is completely software compatible with MPC5500 family devices with an e200z6 core and 64-bit wide ECC syndrome. Because the e200z3 core in MPC5534 is a cacheless processor, the platform RAM is organized on a 32-bit boundary versus the 64-bit organization used on other MPC5500 family MCUs based on the e200z6 core.

5.11   BAM

The BAM is a block of read-only memory that is hard-coded by Freescale and is identical for all MPC5500 family MCU's with an e200 core. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports three different modes of booting. They are:

- Booting from internal Flash memory
- Single Master Booting from external memory (for parts in 324 BGA and 416 BGA package that have an external bus)
- Serial boot loading (a program is downloaded into RAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from Flash memory (either internal or external) and configures the MPC5534 hardware accordingly.

For more information on configuring the MPC5534 at reset see Section 6, "Chip Configuration," on page 30.

5.12 eMIOS

The eMIOS module provides the functionality to generate or measure time events. A unified channel (UC) module is employed that provides a superset of the functionality of all the MIOS channels, while providing a consistent user interface. This allows more flexibility as each unified channel can be programmed for different functions in different applications. In order to identify up to two timed events, each UC contains two comparators, a time base selector and registers. This structure is able to produce match events, which can be configured to measure or generate a waveform. Alternatively, input events can be used to capture the time base, allowing measurement of an input signal.

5.13 eTPU

The eTPU is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU.

The eTPU is an enhanced version of the TPU module implemented on the MC68332 and MPC500 products. Enhancements of the eTPU include a more powerful processor which handles high-level C code efficiently and allows for more functionality and increased performace. Although there is no compatibility at microcode level, the eTPU maintains several features of older TPU versions and is conceptually almost identical. The eTPU library is a superset of the standard TPU library functions modified to take advantage of enhancements in the eTPU. These, along with a C compiler, make it relatively easy to port older applications. By providing source code for the Freescale library, it is possible for the eTPU to support the users own function development.

The eTPU includes these distinctive features:

- 32 channels, each channel is associated with one input and one output signal.
  — Enhanced input digital filters on the input pins for improved noise immunity.
  — Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel as a given time, so each signal can have any functionality.
  — Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  — Input and output signal states visible from the host
- Two independent 24-bit time bases for channel synchronization:
  — First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  — Both time bases can be exported to the eMIOS timer module
  — Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time.

- — Both timebases visible from the host
- Event-triggered microengine:
  - — Fixed-length instruction execution in two-system-clock microcycle
  - — 12 Kbytes of code memory (SCM)
  - — 2.5 Kbytes of parameter (data) RAM (SPRAM)
  - — Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - — 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single bit manipulation, shift operations, sign extension and conditional execution
  - — Additional 24 bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - — Hardware scheduler works as a "task management" unit, dispatching event service routines by pre-defined, host-configured priority.
  - — Automatic channel context switch when a "task switch" occurs, i.e., one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - — SPRAM shared between host CPU and eTPU, supporting communication either between channels and host or inter-channel
  - — Hardware implementation of 4 semaphores support coherent parameter sharing between both eTPU engines
  - — Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - — Nexus Class 3 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions (see Section 5.18, "Nexus," for more details on the Nexus module)
  - — Software breakpoints
  - — SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU normal operation

5.14 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADCs), and a single master to single slave serial interface to an off-chip external device. The two on-chip ADCs are designed to allow access to all the analog channels.

The eQADC transfers commands from multiple command FIFOs (CFIFOs) to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into multiple result FIFOs (RFIFOs) in parallel, independently of the CFIFOs. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the CFIFOs to the on-chip ADCs or to the external device. It also monitors the fullness of CFIFOs and RFIFOs, and accordingly generates DMA or interrupt requests to control data movement between the FIFOs and the system memory, which is external to the eQADC.

5.15 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5534 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. There are two identical DSPI blocks on the MPC5534 MCU.

The DSPIs have three configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as a SPI with support for queues
- Deserial serial interface (DSI) configuration where the DSPI serializes eTPU and eMIOS output channels and deserializes the received data by placing it on the eTPU and eMIOS input channels
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

5.16 eSCI

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to local interconnect network (LIN) slave devices.

5.17 FlexCAN

The MPC5534 MCU contains two controller area network (FlexCAN) blocks. Each FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used pimarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers (MB).

5.18 Nexus

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for the MPC5534 MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the MPC5534. The NDI block interfaces to the host processor, eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the core and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- 15 full duplex pin interface for medium visibility throughput
  — reduced port mode (RPM) comprises 4 MDO pins
  — Auxiliary output port
- 1 MCKO (message clock out) pin
- 4 (message data out) pins
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- 1 $\overline{\text{RDY}}$ (ready) pin
- 1 $\overline{\text{EVTO}}$ (event out) pin
  — Auxiliary input port
- 1 $\overline{\text{EVTI}}$ (event in) pin
- 5 pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  — Supports JTAG mode
- Host processor (e200) development support features
  — IEEE-ISTO 5001-2003 standard Class 3 compliant
  — Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads and/or writes to selected internal memory resources.
  — Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  — Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  — Watchpoint messaging (WPM) via the auxiliary port
  — Watchpoint trigger enable of program and/or data trace messaging
  — Data tracing of instruction fetches via private opcodes

— Subset of PowerPC Book E software debug facilities with OnCE block (Nexus Class 1 features implemented by OnCE)

- eTPU development support features

    — IEEE-ISTO 5001-2003 standard Class 3 compliant for the eTPU

    — Data trace via data write messaging and data read messaging. This allows the development tool to trace reads and writes to selected shared parameter RAM (SPRAM) address ranges. Four data trace windows are available.

    — Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which channel is being serviced. An ownership trace message is transmitted to indicate when a new channel service request is scheduled, allowing the development tools to trace task flow. A special OTM is sent when the engine enters in idle state, meaning that all requests were serviced and no new requests are yet scheduled.

    — Program trace via branch trace messaging. BTM displays program flow discontinuities (start, repeat, jump, return, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced. The branch trace messaging method uses the branch/predicate method to reduce the number of generated messages.

    — Watchpoint messaging via the auxiliary port. WPM provides visibility of the occurrence of the eTPUs' watchpoints and breakpoints.

    — Nexus based breakpoint/watchpoint configuration and single step support.

- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.

- All features are independently configurable and controllable via the IEEE 1149.1 I/O port.

- The NDI block reset is controlled with JCOMP, power-on reset, and the TAP state machine. All these sources are independent of system reset.

- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

5.19 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard.

6   Chip Configuration

Various functions of the MPC5534 may be implemented at reset. The following operations may be configured:

- Boot mode

    — Internal memory boot (default)

    — External memory boot (single master)

    — Boot from serial port (FlexCAN or eSCI)

• PLL mode

    — Normal mode with crystal reference (default)

    — Normal mode with external reference

    — Bypass mode

• Watchdog timer enable

7 Documentation

Table 5 lists other documents that provide information related to the MPC5534 and its development support tools. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com.

Table 5. MPC5534 and Related Documentation

Freescale Document Number	Title	Revision
MPC5534RM	MPC5534 Reference Manual	Not Available
AN2127/D	EMC Guidelines for MPC500-Based Automotive Powertrain Systems	check website
AN1259/D	System Design and Layout Techniques for Noise Reduction in MCU-Based Systems	check website
AN2613	MPC5554 Minimum Board Configuration	check website
AN2614	Nexus Interface Options for the MPC5500 Family	check website
AN2706	EMC Guidelines for MPC5500-based Systems	check website

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