Freescale Semiconductor
Product Brief

Document Number: MPC5565PB
Rev. 0, 11/2007

MPC5565 Microcontroller Product Brief

Designed for engine management and high temperature industrial applications, the MPC5565 32-bit embedded controller is a device from Freescale Semiconductor's MPC5500 Family containing the Book E compliant Power Architecture™ technology core with Variable Length Encoding (VLE). This core complies with the Power Architecture embedded category, and is 100 percent user mode compatible with the original Power PC™ user instruction set architecture (UISA). It offers system performance up to five times that of its MPC500 predecessors, while bringing you the reliability and familiarity of the proven Power Architecture technology.

A comprehensive suite of hardware and software development tools are available to help simplify and speed system design. Development support is available from leading tools vendors providing compilers, debuggers and simulation development environments.

This document provides an overview of the MPC5565 microcontroller features, including the major functional components.

Contents

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1 Applications

The MPC5500 is well suited to network-connected automotive and industrial applications that require complex real-time control.

- Multipoint fuel injection control
- Electronically controlled transmissions
- Direct diesel injection (DDI)
- Gasoline direct injection (GDI)
- Avionics
- Robotics
- Motion control
- Turbine control
- Utilities / Power Management
- Alternative energies
- Autonomous vehicles
- Any model based design using RAppID and Matlab/Simulink

2 Features

2.1 MPC5500 Family Comparison

Table 1. MPC5500 Family Members

MPC5500 Device		MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
Power Core		e200z3	e200z3	e200z6	e200z6	e200z6	e200z6	e200z6	e200z6
Variable Length Instruction Support		Yes	Yes	No	No	Yes	Yes	Yes	Yes
Cache		None	None	8 Kbyte Unified[1]	32 Kbyte Unified[2]	32 Kbyte Unified[3]	8 Kbyte Unified[1]	32 Kbyte Unified[3]	8 Kbyte Unified[1]
Memory Management Unit (MMU)		16 entry	16 entry	32 entry	32 entry	32 entry	32 entry	32 entry	32 entry
Crossbar		4x5	4x5	4x5	3x5	4x6	3^4x5	4x5	5x5
Core Nexus		Class 3+ (NZ3C3)	Class 3+ (NZ3C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)
SRAM		48 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	192 Kbyte	80 Kbyte	128 Kbyte	80 Kbyte
Flash	Main Array	768 Kbyte[5]	1 Mbyte[5]	1.5 Mbyte[6]	2 Mbyte[6]	1 Mbyte[6]	2 Mbyte[6]	3 Mbyte[6]	2 Mbyte[6]
	Shadow Block	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte
External Bus (EBI)	Data Bus	16-bit[7]	16 bit[7]	32 bit[7]	32 bit[7]	32-bit[7]	32-bit[7]	32-bit[7]	32-bit[7]
	Address Bus	24	24	24	24	26[8]	26[8]	26[8]	26[8]
Calibration Bus		Yes	Yes	Partial	No	Yes	Yes	Yes	Yes
Direct Memory Access (DMA)		32 channel	32 channel	32 channel	64 channel	32 channel	32 channel	64 channel	32 channel
DMA Nexus		None	None	Class 3	Class 3	Class 3	Class 3	Class 3	Class 3
Serial		1	2	2	2	4	2	2	2
	eSCI_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_B	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_C	No	No	No	No	Yes	No	No	No
	eSCI_D	No	No	No	No	Yes	No	No	No
Controller Area Network (CAN)		2	2	2	3	3^9	3^9	4^9	5^9
	CAN_A	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_B	No	No	No	64 buf	No	64 buf	64 buf	64 buf
	CAN_C	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_D	No	No	No	No	No	No	64 buf	64 buf
	CAN_E	No	No	No	No	No	No	No	64 buf
SPI		2	3	3	4	3	3	4	3
	DSPI_A	No	No	No	Yes	No	No	Yes	No
	DSPI_B	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_D	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
eMIOS		0 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel

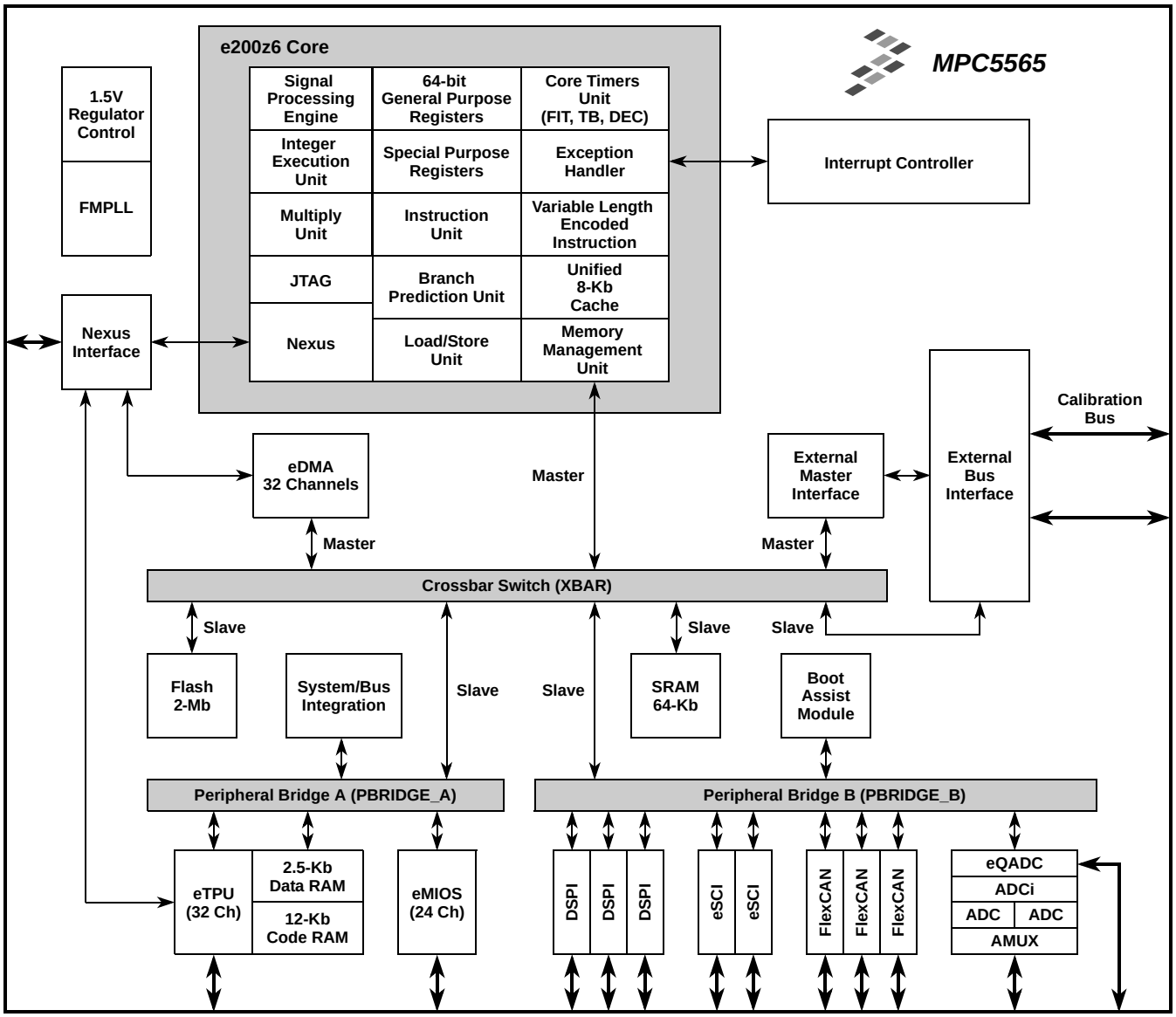
Table 1. MPC5500 Family Members (continued)

MPC5500 Device	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
eTPU	32 channel	32 channel	32 channel	64 channel	0 channel	32 channel	64 channel	32 channel
eTPU_A	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
eTPU_B	No	No	No	Yes	No	No	Yes	No
Code Memory	12 Kbyte	12 Kbyte	12 Kbyte	16 Kbyte	0 Kbyte	12 Kbyte	20 Kbyte	12 Kbyte
Parameter RAM	2.5 Kbyte	2.5 Kbyte	2.5 Kbyte	3 Kbyte	0 Kbyte	2.5 Kbyte	4 Kbyte	2.5 Kbyte
Nexus	Class 3	Class 3	Class 3	Class 3	No	Class 3	Class 3	Class 3
Interrupt Controller	178 channel	210 channel	210 channel	300 channel	231 channel	231 channel	329 channel	281 channel
Analog to Digital Converter (eQADC)	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel
ADC_0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC_1	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast Ethernet Controller (FEC)	No	No	Yes[10]	No	No	No	Yes[10]	Yes[11]
FlexRay	No	No	No	No	Yes	No	No	Yes
FlexRay Nexus	No	No	No	No	Class 3	No	No	Class 3
Phase Lock Loop (PLL)	FM	FM	FM	FM	FM	FM	FM	FM
Maximum System Frequency[12]	80 MHz	80 MHz	132 MHz	132 MHz	132 MHz	132 MHz	144 MHz	132 MHz
Crystal Range	8–20 MHz	8–20 MHz	8–20 MHz	8–20 MHz	8–40 MHz	8–20 MHz	8–20 MHz	8–40 MHz
Voltage Regulator Controller (VRC)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

NOTES:
1 2-way associative
2 8-way associative
3 4-way or 8-way associative
4 The actual crossbar is implemented as a 5x5 crossbar with two unused ports
5 16-byte flash page size for programming
6 32-byte flash page size for programming
7 May not be externally available in some package configurations
8 Either ADDR[8:31] or ADDR[6:29] can be selected.
9 Updated FlexCAN module with optional individual receive filters
10 The FEC signals are shared with data bus pins DATA[16:31]
11 The FEC signals are shared with the calibration bus
12 Initial automotive temperature range qualification

2.2 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5565.



LEGEND

MPC5500 Device Module Acronyms

CAN – Controller area network (FlexCAN)
DSPI – Deserial/serial peripheral interface
eDMA – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued analog/digital converter
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 1. MPC5565 Block Diagram

2.3 Operating Parameters

- Fully static operation, up to 132 MHz
- –40° to 150° C junction temperature
- 1.5 V Core, 3.0–5.25 V I/O, 1.8–3.3 V external bus and Nexus pins

2.4 Packages

- 324-pin plastic ball grid array (TEPBGA)

2.5 Chip Level Features

- Low power design
  - Less than 1.2 W power dissipation
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Separate power supply for stand-by operation for portion of internal SRAM
- Fabricated in 0.13 µm process
- Single issue, 32-bit Book E compliant Power Architecture™ technology e200z6 CPU core
- 32-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 231 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- External bus interface (EBI) with error correction status module (ECSM)
- System integration unit (SIU)
- 2 MB on-chip Flash with Flash bus interface unit (FBIU)
- 80 KB on-chip static RAM
- Boot assist module (BAM)
- Support for dynamic calibration with 3 calibration chip-selects
- 24-channel enhanced modular I/O system (eMIOS)
- One enhanced time processor unit (eTPU) engine. The eTPU engine controls 32 hardware channels.
- Two enhanced queued analog-to-digital converter (eQADC) modules
- Three deserial serial peripheral interface (DSPI) modules
- Two enhanced serial communication interface (eSCI) modules
- Three controller area network (FlexCAN) modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)

2.6 Module Features

The following is a brief summary of the functional blocks in the MPC5565. For more detailed information, refer to the MPC5565 Reference Manual (MPC5565RM).

2.6.1 High Performance e200z6 Core Processor

- 32-bit CPU built on Power Architecture™ technology
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 32-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 8 KB unified cache with line locking
  - 2-way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports assigning cache as instruction or data only on a per way basis
  - Supports tag and data parity
- Vectored interrupt support
- Interrupt latency less than 70 ns @ 132 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (internal SRAM and Flash)
- Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware; double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency in the MPC5565; to reduce latency, long cycle time instructions are aborted upon interrupt requests.
- Extensive system development support through Nexus debug module

2.6.2 System Bus Crossbar Switch (XBAR)

- Three master ports, five slave ports
- 32-bit address bus, 64-bit data bus

- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

2.6.3 Enhanced Direct Memory Access (eDMA) Controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

2.6.4 Interrupt Controller (INTC)

- 231[1] total interrupt vectors
  - 208 peripheral interrupt requests
  - 8 software settable sources
  - 16 reserved
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

2.6.5 Frequency Modulated Phase-locked Loop (FMPLL)

- Input clock frequency
  - 8 to 20 MHz
- Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- Four selectable modes of operation
- Programmable frequency modulation
- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter (reduces number of external components required)
- Engineering clock output configurable to divide-by-2 to divide-by-126 of the system clock frequency

1. Although this device has a maximum of 231 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 232.

2.6.6 External Bus Interface (EBI)

- 1.8–3.3 V nominal I/O voltage
- 324 BGA: 16-bit data bus, 20-bit address bus is default, but configurable to 24-bit address bus. Although this device is designed to support a 32-bit EBI data bus, only 16 data bus pins are available and connected on the 324 BGA package. (The 496-pin VertiCal assembly provides the calibration functionality.)
- Memory controller with support for various memory types
  - Non-burst SDR flash and SRAM
  - Asynchronous/legacy flash and SRAM
  - Most standard memories used with the MPC5xx family
- Configurable bus speed modes
  - 50% of system frequency
  - 25% of system frequency
- Support for external master accesses to internal addresses
- Burst support
- Bus monitor
  - User selectable
  - Programmable timeout period (with eight external bus clock resolution)
- Four chip selects: $\overline{\text{CS}}$[0:3] multiplexed with ADDR[8:11].
- Two write/byte enable ($\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1]) signals in the 324-pin package and the 496-pin assembly.
- Configurable wait states (via chip selects)
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations):
  Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

2.6.7 Calibration Bus Interface

- Calibration bus interface accessible only through 496-pin VertiCal assembly with top connector
- 1.8–3.3 V nominal I/O voltage
- Memory controller shared with EBI
- 16-bit data bus
- 21-bit address bus with no support for the least significant address bit (ADDR31)
- Up to 22-bit address space providing a 4 MB addressing range (the two most significant bits shared with $\overline{\text{CAL\_CS}}$[2:3])
- Chip selects: up to three chip selects ($\overline{\text{CAL\_CS}}$[0] and $\overline{\text{CAL\_CS}}$[2:3] shared with CAL_ADDR[10:11])

2.6.8 System Integration Unit (SIU)

- Centralized GPIO control of bus pins:

  - 324 BGA package: 150 pins
  - 496 CSP BGA package: 225 pins
- Centralized pad control on a per-pin basis
- System reset monitoring and generation
- External interrupt inputs, filtering and control

2.6.9 Error Correction Status Module (ECSM)

- Configurable error-correcting codes (ECC) reporting for internal SRAM and flash memories

2.6.10 On-chip Flash Memory

- 2 MB burst flash memory
- 256 KB × 64-bit configuration
- Censorship protection scheme to prevent flash content visibility
- Hardware read-while-write feature that can erase/program blocks while other blocks are read (used for EEPROM emulation and data calibration)
- 20 blocks with sizes ranging from 16–128 KB to support features such as boot block, operating system block, and EEPROM emulation. Blocks are structured as follows:
  - 2 x 16 KB
  - 2 x 48 KB
  - 2 x 64 KB
  - 14 x 128 KB
- Read while write with multiple partitions
- Parallel programming mode to support rapid end of line programming
- Hardware programming state machine

2.6.11 Configurable Cache Memory, 0–8 KB

- Two-way set-associative unified (instruction and data) cache
- Decouples processor performance from system memory performance

2.6.12 On-chip Internal Static RAM (SRAM)

- 80 KB general-purpose SRAM of which 32 KB are on standby power
- ECC performs single-bit correction, double-bit error detection

2.6.13 Boot Assist Module (BAM)

- Enables and manages the transition of MCU from reset to user code execution in the following configurations:
  - User application can boot from internal or external Flash memory

— Download and execution of code via FlexCAN or eSCI
— User application can boot with either classic Power Architecture code or VLE code

2.6.14 Enhanced Modular I/O System (eMIOS)

- 24 orthogonal channels with double action, PWM, and modulus counter functionality
- Supports all DASM and PWM modes of MIOS14 (MPC5xx)
- Four selectable time bases plus shared time or angle counter bus
- DMA and interrupt request support
- Motor control capability

2.6.15 Enhanced Time Processor Unit (eTPU)

- One engine
- 32-channel engine
- 24-bit timer resolution
- 12 KB shared code memory, 2.5 KB shared data memory
- Event-triggered timer subsystem
- High level assembler/compiler
- Variable number of parameters allocatable per channel
- Double match/capture channels
- Angle clock hardware support
- Shared time or angle counter bus for all eTPU and eMIOS modules
- DMA and interrupt request support
- Nexus Class 3 Debug support (with some Class 4 support)

2.6.16 Enhanced Queued Analog/digital Converter (eQADC)

- Two independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V
- 40 single-ended input channels, expandable to 65 channels with external multiplexers on the 324 BGA package
- Eight channels can be used as four pairs of differential analog input channels
- 10-bit accuracy at 400 ksamples/second; 8-bit accuracy at 800 ksamples/second
- Supports six FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal (eTPU and eMIOS), or external triggers
- DMA and interrupt request support
- Supports all functional modes from QADC (MPC5xx family)

2.6.17 Three Deserial Serial Peripheral Interface Modules (DSPI)

- Serial peripheral interface (SPI)
  - Full duplex communication ports with interrupt and eDMA request support
  - Supports all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Deserial serial interface (DSI)
  - Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels
  - Chaining of DSI submodules
  - Triggered transfer control and change in data transfer control (for reduced EMI)

2.6.18 Two Enhanced Serial Communication Interface (eSCI) Modules

- UART mode provides NRZ format and half or full duplex interface
- eSCI bit rate up to 1 Mb/s
- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8 or 9 bits
- Separately enabled transmitter and receiver
- LIN Support
- DMA support
- Interrupt request support

2.6.19 Three FlexCANs

- 64 message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Based on and including all existing features of the Freescale TouCAN module
- Programmable acceptance filters
- Individual RX filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen only mode capabilities
- Programmable clock source: system clock or oscillator clock
- Reception queue possible by setting more than one RX message buffer with the same ID
- Backwards compatible with previous FlexCAN modules

2.6.20 Nexus Development Interface (NDI)

- Per IEEE®-ISTO 5001-2003
- Real time development support for Power Architecture core and eTPU engines through Nexus class 3 (some class 4 support)
- Data trace of eDMA accesses
- Read and write access
- Configured via the IEEE® 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

2.6.21 IEEE® 1149.1 JTAG Controller (JTAGC)

- IEEE® 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP. Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports IEEE® 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers: a bypass register, a boundary scan register, and a device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

2.6.22 Voltage Regulator Controller

- Provides a low-cost solution to powering the core logic; reduces the number of power supplies required from the customer power supply chip.

2.6.23 POR Block

- Provides initial reset condition up to the voltage at which pins ($\overline{\text{RESET}}$) can be read safely; it does not guarantee the safe operation of the chip at specified minimum operating voltages.

3 Developer Environment

The MPC5500 family of MCUs supports similar tools and third party developers as other Power Architecture products, offering a widespread, established network of tools and software vendors.

The following development support is available.

- Evaluation/development boards and systems
- Emulators, simulators, and probes
- Flash programmers
- IDE/tool chains

- C/C++ compilers
- Hardware and software debuggers
- Initialization/boot code generators
- Software libraries
- Device/module drivers
- C-header and equate files
- JTAG interfaces
- Code examples
- Third party real-time operating systems (RTOS)

4 Document Revision History

Table 2 provides a revision history of this document.

Table 2. Revision History

Revision	Substantive Change(s)
Rev. 0	First public release.

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Document Number: MPC5565PB
Rev. 0
11/2007

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