Freescale Semiconductor
Product Brief

Document Number: MPC5566PB
Rev. 1, 12/2007

MPC5566 Microcontroller Product Brief

Designed for engine management and high-temperature industrial applications, the MPC5566 32-bit embedded controller is part of Freescale Semiconductor's MPC5500 family that uses the Book E compliant Power Architecture™ technology core with variable length encoding (VLE). The core complies with the Power Architecture embedded category, and is 100 percent user-mode compatible with the original PowerPC™ user instruction set architecture (UISA). It offers system performance up to five times that of its MPC500 predecessors, bringing you the reliability and familiarity of the proven Power Architecture technology.

A comprehensive suite of hardware and software development tools are available to help simplify and speed system design. Development support is available from leading tools vendors providing compilers, debuggers and simulation development environments.

This document provides an overview of the MPC5566 microcontroller features, including the major functional components.

Contents

freescale™ semiconductor

1 Applications

The MPC5500 is well suited to network-connected automotive and industrial applications that require complex real-time control.

- Multipoint fuel injection control
- Electronically controlled transmissions
- Direct diesel injection (DDI)
- Gasoline direct injection (GDI)
- Avionics
- Robotics
- Motion control
- Turbine control
- Utilities/Power Management
- Alternative energies
- Autonomous vehicles
- Any model based design using RAppID and Matlab/Simulink

2 Features

This section provides a high-level description of the MPC5566 features.

2.1 MPC5500 Device Comparison

Table 1 compares the microcontroller features of the MPC5566 to the MPC5554.

Table 1. MPC5554 vs. MPC5566 Family Members

Module		MPC5566	MPC5554
PowerPC Core		e200z6	e200z6
Variable length instruction support		Yes	No
Cache		32 Kbyte Unified[1]	32 Kbyte Unified[2]
Memory management unit (MMU)		32 entry	32 entry
Crossbar		4x5	3x5
Core Nexus		Class 3+ (NZ6C3)	Class 3+ (NZ6C3)
SRAM		128 Kbyte	64 Kbyte
Flash	Main array [3]	3 MB	2 MB
	Shadow block	1 Kbyte	1 Kbyte
External bus (EBI)	Data bus	32 bits[4]	32 bits
	Address bus	26 bits[5]	24 bits
Calibration bus		Yes	No
Direct memory access (DMA)		64 channels	64 channels
DMA Nexus		Class 3	Class 3

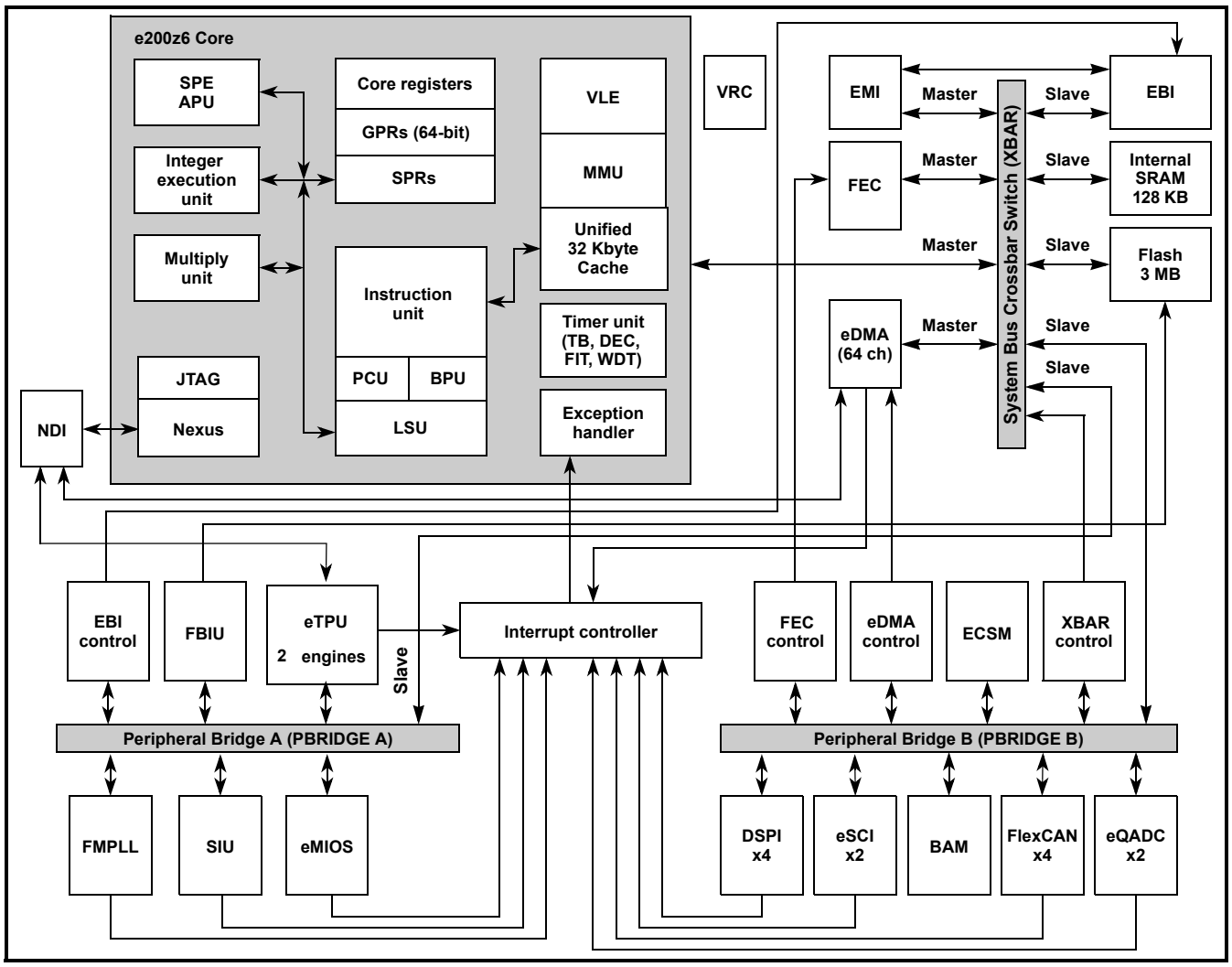
Table 1. MPC5554 vs. MPC5566 Family Members (continued)

Module	MPC5566	MPC5554
Serial	2	2
eSCI A	Yes	Yes
eSCI B	Yes	Yes
Controller area network (CAN)	4[6]	3
CAN A	64 buffers	64 buffers
CAN B	64 buffers	64 buffers
CAN C	64 buffers	64 buffers
CAN D	64 buffers	No
CAN E	No	No
SPI	4	4
DSPI A	Yes	Yes
DSPI B	Yes	Yes
DSPI C	Yes	Yes
DSPI D	Yes	Yes
eMIOS	24 channels	24 channels
eTPU	64 channels	64 channels
eTPU A	Yes	Yes
eTPU B	Yes	Yes
Code memory	20 Kbyte	16 Kbyte
Parameter RAM	4 Kbyte	3 Kbyte
Nexus	Class 3	Class 3
Interrupt controller	332 channels [7]	308 channels
Analog to digital converter (eQADC)	40 channels	40 channels
ADC 0	Yes	Yes
ADC 1	Yes	Yes
Fast Ethernet controller (FEC)	Yes[8]	No
FlexRay	No	No
FlexRay Nexus	No	No
Phase-lock loop (PLL)	Frequency modulated	Frequency modulated
Maximum system frequency[9]	144 MHz	132 MHz
Crystal range	8 – 20 MHz	8 – 20 MHz
Voltage regulator controller (VRC)	Yes	Yes

NOTES:
1 4-way and 8-way associative
2 8-way associative
3 32-byte flash page size for programming
4 Check the package configuration to verify the external data and address bus widths
5 ADDR[8:31] or ADDR[6:29] can be selected
6 Updated FlexCAN module with optional individual receive filters
7 The max number of interrupts is 329, but because it must be a multiple of four, 332 is listed.
8 The FEC signals are shared with data bus pins DATA[16:31]
9 Initial automotive temperature range qualification

2.2 Block Diagram

Figure 1 shows a top-level block diagram of the MPC5566.



Legend

BAM – Boot assist module
CAN – Controller area network (FlexCAN)
DSPI – Deserial/serial peripheral interface
EBI – External bus interface
ECSM – Error correction status module
EMI – External master interface
eDMA – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued analog/digital converter
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing unit
FBIU – Flash bus interface unit
FEC – Fast Ethernet controller
FMPLL – Frequency modulated phase-locked loop
NDI – Nexus developmental interface
SIU – System integration unit
SRAM – Internal static RAM
VRC – Voltage regulator controller
XBAR – System bus crossbar switch

e200z6 core components

APU – Auxiliary processing unit
BIU – Bus interface unit
BPU – Branch processing unit
DEC – Decrementer
FIT – Fixed interval timer
GPR – General-purpose register
JTAG – JTAG controller
LSU – Load/store unit
MMU – Memory management unit
PCU – Program counter unit
SPE – Signal processing engine
SPR – Special purpose register
TB – Time base
VLE – Variable length encoding
WDT – Watchdog timer
↔ – System bus

Figure 1. MPC5566 Block Diagram

2.3 Operating Parameters

- Fully static operation, up to 144 MHz
- –40° to 150° C junction temperature
- 1.5 V core, 3.0 – 5.5 V I/O, 1.6 – 3.6 V external bus, 2.5 – 3.6 V Nexus pins

2.4 Package

A 416-pin ball grid array (BGA)

2.5 Chip-level Features

- Low-power design
  - Less than 1.2 Watts power dissipation
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Separate power supply for stand-by operation for portion of internal SRAM
- Fabricated in 0.13 µm process
- Single-issue, 32-bit Book E compliant Power Architecture technology e200z6 CPU core
- 64-channel enhanced direct memory access controller (eDMA)
- Interrupt controller (INTC) capable of handling 329 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- External bus interface (EBI)
- Error correction status module (ECSM)
- System integration unit (SIU)
- 3 MB on-chip flash with flash bus interface unit (FBIU)
- 128-Kbyte on-chip static RAM
- Boot assist module (BAM)
- Support for dynamic calibration with four calibration chip-selects
- 24-channel enhanced modular I/O system (eMIOS)
- Dual enhanced time processor unit (eTPU) engines; each eTPU engine controls 32 hardware channels, for a total of 64 hardware channels
- Two enhanced queued analog-to-digital converter (eQADC) modules
- Four deserial serial peripheral interface (DSPI) modules
- Two enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE

2.6 Module Features

The following is a brief summary of the functional blocks in the MPC5566. For more detailed information, refer to the *MPC5566 Reference Manual* (MPC5566RM).

2.6.1 High Performance e200z6 Core Processor

- 32-bit PowerPC Book E compliant CPU
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 32-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 32-Kbyte unified cache with line locking
  - Four-way and eight-way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports assigning cache as instruction or data only on a per way basis
  - Supports tag and data parity
- Vectored interrupt support
- Interrupt latency less than 70 ns @ 144 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (internal SRAM and flash)
- Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single-precision hardware, double-precision software library
  - Conversion instructions between single-precision floating point and fixed point
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency in the MPC5566. To reduce latency, long cycle-time instructions are aborted upon interrupt requests.
- Extensive system development support through Nexus debug module

2.6.2 System Bus Crossbar Switch (XBAR)

- Four master ports and five slave ports
- 32-bit address bus and 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

2.6.3 Enhanced Direct Memory Access (eDMA) Controller

- 64 channels support independent 8-, 16- and 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

2.6.4 Interrupt Controller (INTC)

- 332 total interrupt vectors [1]
  - 298 peripheral interrupt requests
  - eight software settable sources
  - 26 reserved
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

2.6.5 Frequency Modulated Phase-locked Loop (FMPLL)

- Input clock frequency 8 to 20 MHz
- Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- Four selectable modes of operation
- Programmable frequency modulation
- Lock-detect circuitry continuously monitors lock status
- Loss-of-clock (LOC) detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter (reduces number of external components required)
- Engineering clock output configurable to divide-by-2 to 126 of the system clock frequency

1. Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332.

2.6.6 External Bus Interface (EBI)

- 1.8 – 3.3 V I/O nominal voltage
- Memory controller with support for various memory types
- MPC5566 specifications:
  - 416 BGA: 32-bit data bus, 26-bit address bus
  - 496 BGA: 32-bit data bus, 26-bit address bus
- 26-bit address bus: the two most significant bits (MSBs), ADDR[6:7], are multiplexed with the two least significant bits (LSBs) ADDR[30:31].
- Selectable drive strength
- Configurable bus speed modes
- Support for external master accesses to internal addresses
- Burst support
- Bus monitor
- Four chip selects: $\overline{\text{CS}}$[0:3] multiplexed with ADDR[8:11].
- Four write/byte enable ($\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1]) signals in the 416-pin package
- Configurable wait states
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus (with some limitations): Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

2.6.7 Calibration Bus Interface

- Calibration bus interface only accessible through 496-pin VertiCal assembly top connector
- 1.8 – 3.3 V nominal I/O voltage
- Memory controller shared with EBI
- 16-bit data bus (CAL_DATA[0:15])
- Four calibration bus chip selects (CAL_$\overline{\text{CS}}$[0:3]); three calibration chip select signals (CAL_$\overline{\text{CS}}$[1:3]) are muxed with three calibration address signals (CAL_ADDR[9:11])
- 19-bit calibration address bus (CAL_ADDR[12:30]); no support for the least significant address bit (CAL_ADDR31)
- Up to 22-bit calibration address bus by using CAL_ADDR[9:11] with one calibration chip select signal (CAL_$\overline{\text{CS}}$[0]) to provide a 4 MB addressing range

2.6.8 System Integration Unit (SIU)

- Centralized GPIO control of bus pins:
  - 416 BGA package: 178 pins
  - 496 CSP BGA package: 225 pins
- Centralized pad control on a per-pin basis
- System reset monitoring and generation
- External interrupt inputs, filtering and control
- Internal multiplexer submodule

2.6.9 Error Correction Status Module (ECSM)

Configurable error-correcting codes (ECC) reporting for internal SRAM and flash memories.

2.6.10 On-chip Flash Memory

- 3 MB burst flash memory
- 384 K × 64-bit configuration
- Censorship protection scheme to prevent flash content visibility
- Hardware read-while-write feature that allows blocks to be erased/programmed while other blocks are being read (used for EEPROM emulation and data calibration)
- 28 blocks with sizes ranging from 16 – 128 Kbyte to support features such as boot block, operating system block, and EEPROM emulation. Blocks are structured as follows:
  - 2 x 16 Kbyte
  - 2 x 48 Kbyte
  - 2 x 64 Kbyte
  - 22 x 128 Kbyte
- Read while write with multiple partitions
- Parallel programming mode to support rapid end-of-line programming
- Hardware programming state machine

2.6.11 Configurable Cache Memory, 0 – 32 Kbytes

- Four-way and eight-way set-associative unified (instruction and data) cache
- Decouples processor performance from system memory performance

2.6.12 On-chip Internal Static RAM (SRAM)

- Total of 128 Kbyte internal general-purpose static RAM (SRAM), of which 32 Kbyte are designated to standby power
- ECC performs single-bit correction and double-bit error detection

2.6.13 Boot Assist Module (BAM)

Enables and manages the transition of the MCU from reset to user-code execution in the following configurations:

- User application can boot from internal or external flash memory
- Download and execute program code via FlexCAN or eSCI
- User application can boot to classic Power PC code or VLE code

2.6.14 Enhanced Modular I/O System (eMIOS)

- 24 orthogonal channels with double action, PWM, and modulus counter functionality
- Supports all DASM and PWM modes of MIOS14 (MPC5xx)
- Four selectable time bases plus shared time or angle counter bus
- DMA and interrupt request support
- Motor control capability

2.6.15 Enhanced Time Processor Unit (eTPU)

- Two 32-channels eTPU engines for a total of 64 channels
- 24-bit timer resolution
- 20-Kbyte shared code memory, 4-Kbyte shared data memory
- Event-triggered timer subsystem
- High level assembler/compiler
- Variable number of parameters allocatable per channel
- Double match/capture channels
- Angle clock hardware support
- Shared time or angle counter bus for all eTPU and eMIOS modules
- DMA and interrupt request support
- Nexus Class 3 Debug support (with some Class 4 support)

2.6.16 Enhanced Queued Analog/Digital Converter (eQADC)

- Two independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0 – 5 V
- 40 single-ended inputs channels, expandable to 65 channels
- 34 single-ended inputs channels, expandable to 57 channels
- Eight channels can be used as four pairs of differential analog input channels
- 10-bit accuracy at 400 ksamples/second, 8-bit accuracy at 800 ksamples/second
- Supports six FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal (eTPU and eMIOS), or external triggers

- DMA and interrupt request support
- Supports all functional modes from MPC5xx family QADC module

2.6.17 Four Deserial Serial Peripheral Interface Modules (DSPI)

- Serial Peripheral Interface (SPI)
  - Full duplex communication ports with interrupt and eDMA request support
  - Supports all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay and clock phase on a per frame basis
  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Deserial serial interface (DSI)
  - Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels
  - Chaining of DSI submodules
  - Triggered transfer control and change in data transfer control (for reduced EMI)

2.6.18 Two Enhanced Serial Communication Interface (eSCI) Modules

- UART mode provides NRZ format and half- or full-duplex interface
- eSCI bit rate up to one Mbps
- Advanced error detection, and optional parity generation and detection
- Word length programmable as eight or nine bits
- Separately enabled transmitter and receiver
- LIN Support
- DMA support
- Interrupt request support

2.6.19 Four FlexCANs

- 64 message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Based on and including all existing features of the Freescale TouCAN module
- Programmable acceptance filters
- Individual receive data filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen only mode capabilities

- Programmable clock source: system clock or oscillator clock
- Reception queue model; set more than one receive message buffer with the same ID
- Backwards compatibility with previous FlexCAN modules

2.6.20 Nexus Development interface (NDI)

- Per IEEE®-ISTO 5001-2003
- Real time development support for PowerPC core and eTPU engines through Nexus Class 3 (some Class 4 support)
- Data trace of eDMA accesses
- Read and write access
- Configured via the IEEE® 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

2.6.21 IEEE® 1149.1 JTAG Controller (JTAGC)

- IEEE® 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP. Selectable modes of operation include JTAGC/debug or normal system operation.
- Five-bit instruction register that supports IEEE® 1149.1-2001 defined instructions
- Five-bit instruction register that supports additional public instructions
- Three test data registers: a bypass register, a boundary scan register, and a device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

2.6.22 Voltage Regulator Controller

Provides a low cost solution to power the core logic. It reduces the number of power supplies required from the customer power supply chip.

2.6.23 Power-on Reset (POR) Block

Provides initial reset condition up to the voltage at which pins ($\overline{\text{RESET}}$) can be read safely. It does not guarantee the safe operation of the chip at specified minimum operating voltages.

2.6.24 Fast Ethernet Controller (FEC)

- IEEE® 802.3 MAC (compliant with IEEE® 802.3 1998 edition)
- Built-in FIFO and DMA controller

- Fully software compatible with the FEC module of Freescale's industry standard PowerQUICC communications controller
- Full compliance with the IEEE 802.3 standard for 10/100 base-T
- Support for different Ethernet physical interfaces:
- IEEE® 802.3 MII
- 10 Mbps seven-wire interface (industry standard)
- MII management interface for control and status
- Large on-chip transmit and receive FIFOs to support a variety of bus latencies
- Retransmission from the transmit FIFO after a collision
- Automatic internal flushing of the receive FIFO for runts and collisions
- External BD tables of user-definable size allow nearly unlimited flexibility in management of transmit and receive buffer memory
- Address recognition for broadcast, single station address, promiscuous mode, and multicast hashing
- Ethernet channel uses DMA burst transactions to transfer data to and from external/system memory

3 Developer Environment

The MPC5500 family of MCUs supports similar tools and third party developers as other Power Architecture products, offering a widespread, established network of tools and software vendors. The following development support is available.

- Evaluation/development boards and systems
- Emulators, simulators, and probes
- Flash programmers
- IDE/tool chains
- C/C++ compilers
- Hardware and software debuggers
- Initialization/boot code generators
- Software libraries
- Device/module drivers
- C-header and equate files
- JTAG interfaces
- Code examples
- Third party real-time operating systems (RTOS)

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MPC5566PB
Rev. 1
12/2007

freescale™
semiconductor