**MOTOROLA**

Semiconductor Products Sector

# *PowerPC*™

# Advance Information
# MPC7400 RISC Microprocessor
# Hardware Specifications

The MPC7400 is an implementation of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the MPC7400. For functional characteristics of the processor, refer to the MPC7400 RISC Microprocessor User's Manual.

This document contains the following topics:

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## 1.1 Overview

The MPC7400 is the first implementation of the fourth generation (G4) of PowerPC microprocessors from Motorola. The MPC7400 implements the full PowerPC 32-bit architecture and is targeted at both portable and computing systems applications. Some comments on the MPC7400 (with respect to MPC750):

- The MPC7400 adds an implementation of the new AltiVec™ technology instruction set
- The MPC7400 includes significant improvements in memory subsystem (MSS) bandwidth and offers an optional, high-bandwidth MPX bus interface
- The MPC7400 adds full hardware-based multiprocessing capability, including a 5-state cache coherency protocol (4 MESI states plus a fifth state for shared intervention)
- The MPC7400 is implemented in a next generation process technology for core frequency improvement
- The MPC7400 floating-point unit has been improved to make latency equal for double-precision and single-precision operations involving multiplication
- The completion queue has been extended to 8 slots
- There are no other significant changes to scalar pipelines, decode/dispatch/completion mechanisms, or the branch unit. The MPC750's 4-stage pipeline model is unchanged (fetch, decode/dispatch, execute, complete/writeback)

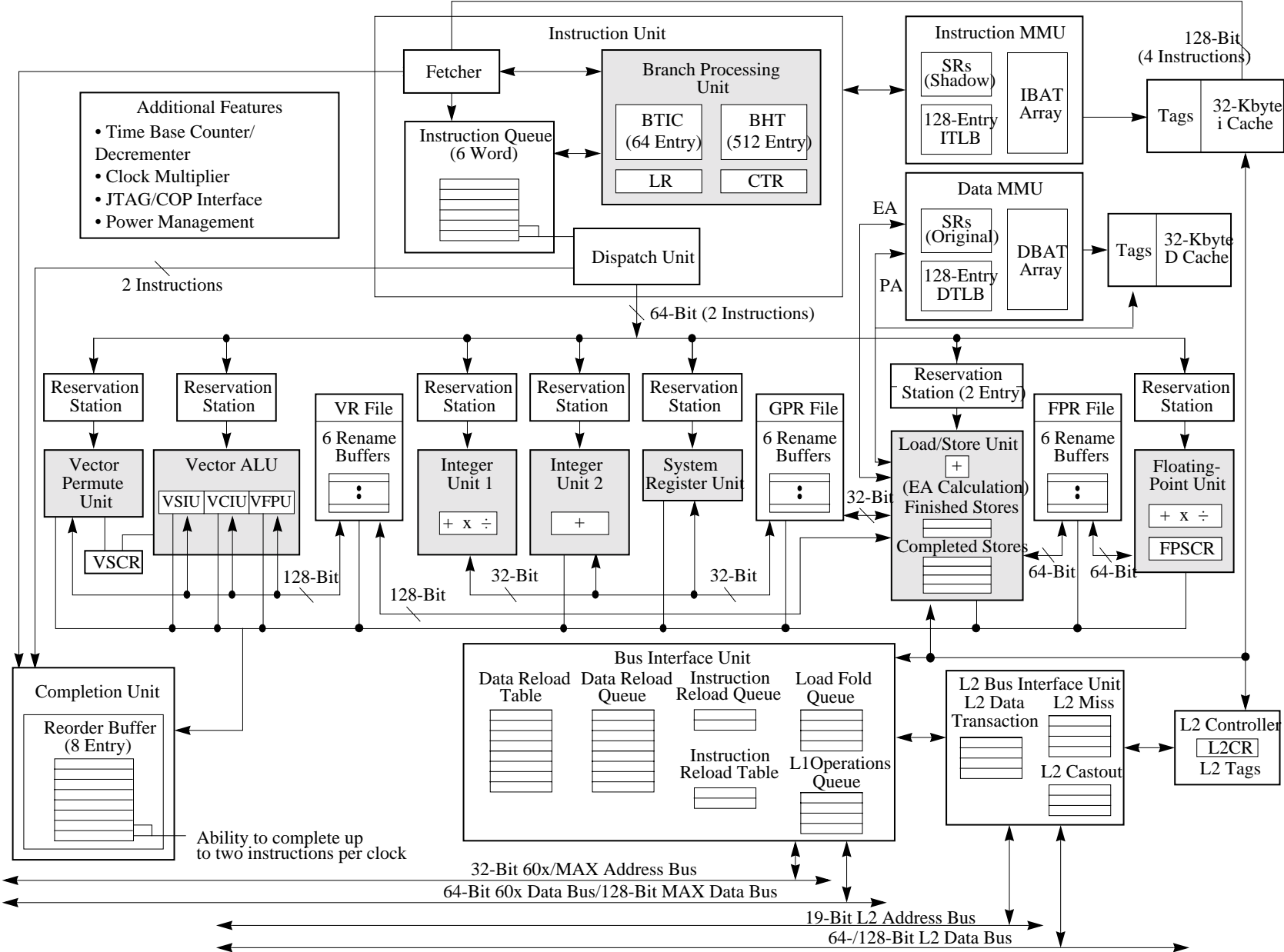Figure 1 shows a block diagram of the MPC7400.

**Figure 1. MPC7400 Block Diagram**

## 1.2  Features

This section summarizes features of the MPC7400's implementation of the PowerPC architecture. Major features of the MPC7400 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 8 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed-point units (FXUs) that share 32 GPRs for integer operands
  - Fixed-point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage floating-point unit and a 32-entry FPR file
  - Support for IEEE-754 standard single and double-precision floating-point arithmetic
  - 3 cycle latency, 1 cycle throughput (single or double precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions

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**Features**

- AltiVec Unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit.
  - Contains its own 32-entry 128-bit vector register file (VRF) with 6 renames
  - The vector ALU unit is further sub-divided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU), and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/store unit
  - One cycle load or store cache access (byte, half word, word, double-word)
  - 2 cycle load latency with 1 cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all 4 architecture AltiVec DST streams
- Level 1 (L1) cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache (iL1)
  - 32K, 32-byte line, 8-way set associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page per page basis)
  - Supports all PowerPC memory coherency modes
  - Non-blocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) cache interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512K, 1M, and 2Mbyte 2-way set associative L2 cache support
  - Copyback or write-through data cache (on a page basis, or for all L2)
  - 32 byte (512K), 64 byte (1M), or 128 byte (2M) sectored line size
  - Supports pipelined (register-register) synchronous burst SRAMs and pipelined (register-register) late-write synchronous burst SRAMs
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64 bit data bus
  - Selectable interface voltages of 1.8, 2.5, and 3.3V.

- Memory management unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - 4 instruction BATs and 4 data BATs
  - Virtual memory support for up to 4 exabytes ($2^{52}$) of virtual memory
  - Real memory support for up to 4 gigabytes ($2^{32}$) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient data flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2, and the bus are 128-bits wide
  - dL1 is fully pipelined to provide 128 bits/cycle to/from the VRF
  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s
  - Up to 8 outstanding, out-of-order, cache misses between dL1 and L2/bus
  - Up to 7 outstanding, out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older, outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (i.e., address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - 2-entry finished store queue and 4-entry completed store queue between load/store unit and dL1
  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, etc.) from dL1 and L2
- Bus interface
  - New MPX bus extension to 60X processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64 bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x supported
  - Selectable interface voltages of 1.8 and 3.3V.
- Power management
  - Low-power design with thermal requirements very similar to MPC740 and MPC750.
  - 1.8 volt processor core
  - Selectable interface voltages below 3.3V can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST)—factory test only.
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and serviceability
  - Parity checking on 60x and L2 cache buses

## 1.3  General Parameters

The following list provides a summary of the general parameters of the MPC7400:

| | |
|---|---|
| Technology | 0.20 µm CMOS, six-layer metal |
| Die size | 7.86 mm x 10.58 mm (83 mm$^2$) |
| Transistor count | 10.5 million |
| Logic design | Fully-static |
| Packages | Surface mount 360 ceramic ball grid array (CBGA) |
| Core power supply: | 1.8V ± 100 mV dc (nominal; see Table 3 for recommended operating conditions) |
| I/O power supply | 1.8V ± 100 mV dc or |
| | 2.5V ± 100 mV dc or |
| | 3.3V ± 5% (input thresholds are configuration pin selectable) |

## 1.4  Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC7400.

### 1.4.1  DC Electrical Characteristics

The tables in this section describe the MPC7400 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Maximum Value | Unit | Note |
|---|---|---|---|---|---|
| Core supply voltage | | Vdd | –0.3 to 2.1 | V | 4 |
| PLL supply voltage | | AVdd | –0.3 to 2.1 | V | 4 |
| L2 DLL supply voltage | | L2AVdd | –0.3 to 2.1 | V | 4 |
| Processor bus supply voltage | | OVdd | –0.3 to 3.465 | V | 3 |
| L2 bus supply voltage | | L2OVdd | –0.3 to 3.465 | V | 3 |
| Input voltage | Processor bus | $V_{in}$ | –0.3 to OVdd + 0.3V | V | 2,5 |
| | L2 Bus | $V_{in}$ | –0.3 to L2OVdd + 0.3V | V | 2,5 |
| | JTAG Signals | $V_{in}$ | –0.3 to 3.6 | V | |
| Storage temperature range | | $T_{stg}$ | –55 to 150 | °C | |

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Caution: $V_{in}$ must not exceed OVdd or L2OVdd by more than 0.3V at any time including during power-on reset.

3. Caution: L2OVdd/OVdd must not exceed Vdd/AVdd/L2AVdd by more than 2.0V at any time including during power-on reset.

4. Caution: Vdd/AVdd/L2AVdd must not exceed L2OVdd/OVdd by more than 0.4V at any time including during power-on reset. In addition, operation at nominal Vdd/AVdd/L2AVdd greater than nominal L2OVdd or OVdd in the 1.8V input threshold select mode can cause erratic operation and AC timing values worse than described in this specification.

5. $V_{in}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

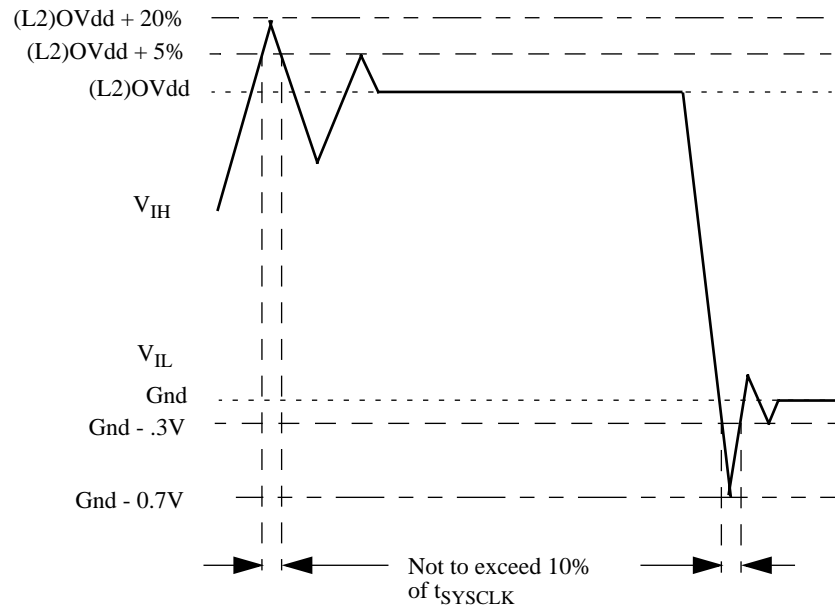Figure 2 shows the undershoot and overshoot voltage on the MPC7400.



**Figure 2. Overshoot/Undershoot Voltage**

The MPC7400 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7400 "core" voltage must always be provided at nominal 1.8V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal HRESET. The output voltage will swing from GND to the maximum voltage applied to the OVdd or L2OVdd power pins.

**Table 2. Input Threshold Voltage Setting**

| BVSEL Signal | Processor Bus Input Threshold is Relative to: | L2VSEL Signal | L2 Bus Input Threshold is Relative to: | Note |
|---|---|---|---|---|
| 0 | 1.8V | 0 | 1.8 | 1 |
| HRESET | 2.5V | HRESET | 2.5 | 1,2 |
| 1 | 3.3V | 1 | 3.3 | 1 |

Notes:

1. Caution: The input threshold selection must agree with the OVdd/L2OVdd voltages supplied.

2. To select the 2.5 volt threshold option, L2VSEL / BVSEL should be tied to HRESET so that the two signals change state together.

**Electrical and Thermal Characteristics**

Table 3 provides the recommended operating conditions for the MPC7400.

**Table 3. Recommended Operating Conditions**

| Characteristic | | Symbol | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| Core supply voltage | | Vdd | 1.8v ± 100mv | V | 1 |
| PLL supply voltage | | AVdd | 1.8v ± 100mv | V | 1 |
| L2 DLL supply voltage | | L2AVdd | 1.8v ± 100mv | V | 1 |
| Processor bus supply voltage | BVSEL = 0 | OVdd | 1.8v ± 100mv | V | 1 |
| | BVSEL = HRESET | OVdd | 2.5v ± 100mv | V | 1 |
| | BVSEL = 1 | OVdd | 3.3v ± 165mv | V | 1 |
| L2 bus supply voltage | L2VSEL = 0 | L2OVdd | 1.8v ± 100mv | V | 1 |
| | L2VSEL = HRESET | L2OVdd | 2.5v ± 100mv | V | 1 |
| | L2VSEL = 1 | L2OVdd | 3.3v ± 165mv | V | 1 |
| Input voltage | Processor bus | $V_{in}$ | GND to OVdd | V | 1 |
| | L2 Bus | $V_{in}$ | GND to L2OVdd | V | 1 |
| | JTAG Signals | $V_{in}$ | GND to OVdd | V | 1 |
| Die-junction temperature | | $T_j$ | 0 to 105 | °C | 2 |

Note:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

2. The extended temperature parts have die-junction temperature of -40 to 105 ˚C.

Table 4 provides the package thermal characteristics for the MPC7400.

**Table 4. Package Thermal Characteristics**

| Characteristic | Symbol | Value | Rating |
|---|---|---|---|
| CBGA package thermal resistance, junction-to-case thermal resistance (typical) | $\theta_{JC}$ | 0.03 | °C/W |
| CBGA package thermal resistance, die junction-to-lead thermal resistance (typical) | $\theta_{JB}$ | 3.8 | °C/W |

Note: Refer to Section 1.8, "System Design Information," for more details about thermal management.

The MPC7400 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the MPC7400 RISC Microprocessor User's Manual for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

**Table 5. Thermal Sensor Specifications**

At recommended operating conditions (See Table 3)

| Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Temperature range | 0 | 127 | °C | 1 |
| Comparator settling time | 20 | — | µs | 2 |

**Table 5. Thermal Sensor Specifications**

At recommended operating conditions (See Table 3)

| Characteristic | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Resolution | 4 | — | °C | 3 |
| Accuracy | -12 | +12 | °C | |

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but it must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Motorola application note, "Programming the Thermal Assist Unit in the MPC750 Microprocessor," (order #: AN1800/D).
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the MPC7400.

**Table 6. DC Electrical Specifications**

At recommended operating conditions (See Table 3)

| Characteristic | Nominal Bus Voltage[1] | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage (all inputs except SYSCLK) | 1.8 | $V_{IH}$ | 0.65 * (L2)OVdd | (L2)OVdd + 0.3 | V | 2,3 |
| | 2.5 | $V_{IH}$ | 1.7 | (L2)OVdd + 0.3 | V | 2,3 |
| | 3.3 | $V_{IH}$ | 2.0 | (L2)OVdd + 0.3 | V | 2,3 |
| Input low voltage (all inputs except SYSCLK) | 1.8 | $V_{IL}$ | -0.3 | 0.35 * OVdd | V | |
| | 2.5 | $V_{IL}$ | -0.3 | 0.2 * (L2)OVdd | V | |
| | 3.3 | $V_{IL}$ | -0.3 | 0.8 | V | |
| SYSCLK input high voltage | 1.8 | $CV_{IH}$ | 1.5 | OVdd + 0.3 | V | 2 |
| | 3.3 | $CV_{IH}$ | 2.4 | OVdd + 0.3 | V | 2 |
| SYSCLK input low voltage | 1.8 | $CV_{IL}$ | -0.3 | 0.2 | V | |
| | 3.3 | $CV_{IL}$ | -0.3 | 0.4 | V | |
| Input leakage current, $V_{in}$ = L2OVdd/OVdd | | $I_{in}$ | — | 10 | µA | 2,3 |
| Hi-Z (off-state) leakage current, $V_{in}$ = L2OVdd/OVdd | | $I_{TSI}$ | — | 10 | µA | 2,3,5 |
| Output high voltage, $I_{OH}$ = -6 mA | 1.8 | $V_{OH}$ | (L2)OVdd–0.45 | — | V | |
| | 2.5 | $V_{OH}$ | 1.7 | — | V | |
| | 3.3 | $V_{OH}$ | 2.4 | — | V | |

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**Electrical and Thermal Characteristics**

### Table 6. DC Electrical Specifications (Continued)

At recommended operating conditions (See Table 3)

| Characteristic | Nominal Bus Voltage[1] | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output low voltage, $I_{OL}$ = 6 mA | 1.8 | $V_{OL}$ | — | 0.45 | V | |
| | 2.5 | $V_{OL}$ | — | 0.4 | V | |
| | 3.3 | $V_{OL}$ | — | 0.4 | V | |
| Capacitance, $V_{in}$ = 0 V, f = 1 MHz | | $C_{in}$ | — | 7.5 | pF | 3,4 |

Notes:

1. Nominal voltages; See Table 3 for recommended operating conditions.

2. For processor bus signals, the reference is OVdd while L2OVdd is the reference for the L2 bus signals.

3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.

4. Capacitance is periodically sampled rather than 100% tested.

5. The leakage is measured for nominal OVdd and Vdd, or both OVdd and Vdd must vary in the same direction (for example, both OVdd and Vdd vary by either +5% or -5%).

Table 7 provides the power consumption for the MPC7400.

**Table 7. Power Consumption for MPC7400**

| | Processor (CPU) Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 350 MHz | 400 MHz | | |
| Full-On Mode | | | | |
| Typical | 4.6 | 5.3 | W | 1, 3 |
| Maximum | 9.9 | 11.3 | W | 1, 2, 4 |
| Doze Mode | | | | |
| Maximum | 4.4 | 5.0 | W | 1, 2 |
| Nap Mode | | | | |
| Maximum | 1.75 | 2.0 | W | 1, 2 |
| Sleep Mode | | | | |
| Maximum | 1.75 | 2.0 | W | 1, 2 |
| Sleep Mode—PLL and DLL Disabled | | | | |
| Typical | 600 | 600 | mW | 1, 3 |
| Maximum | 1.0 | 1.0 | W | 1, 2 |

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.

2. Maximum power is measured at Vdd = 1.9V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.

3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 1.8V, OVdd = L2OVdd = 3.3V in a system while running a codec application that is AltiVec intensive.

4. These values include the use of AltiVec. Without AltiVec operation, estimate a 25% decrease.

## 1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7400. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency; see Section 1.10, "Ordering Information."

## 1.4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

**Table 8. Clock AC Timing Specifications**

At recommended operating conditions (See Table 3)

| Characteristic | Symbol | Maximum Processor Core Frequency | | | | Unit | Notes |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | 350 MHz | | 400 MHz | | | |
| | | Min | Max | Min | Max | | |
| Processor frequency | $f_{core}$ | 300 | 350 | 300 | 400 | MHz | 1 |
| VCO frequency | $f_{VCO}$ | 600 | 700 | 600 | 800 | MHz | 1 |
| SYSCLK frequency | $f_{SYSCLK}$ | 25 | 100 | 25 | 100 | MHz | 1 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 10 | 40 | 7.5 | 40 | ns | |
| SYSCLK rise and fall time | $t_{KR}$ & $t_{KF}$ | — | 1.0 | — | 1.0 | ns | 2 |
| | $t_{KR}$ & $t_{KF}$ | — | 0.5 | — | 0.5 | ns | 3 |
| SYSCLK duty cycle measured at OVdd/2 | $t_{KHKL}/t_{SYSCLK}$ | 40 | 60 | 40 | 60 | % | 4 |
| SYSCLK jitter | | — | ±150 | — | ±150 | ps | 5 |
| Internal PLL relock time | | — | 100 | — | 100 | μs | 6 |

Notes:

1. Caution: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8.1, "PLL Configuration," for valid PLL_CFG[0–3] settings

2. Rise and fall times for the SYSCLK input measured from 0.4V to 2.4V when OVdd = 3.3V nominal.

3. Rise and fall times for the SYSCLK input measured from 0.4V to 1.4V when OVdd = 1.8V nominal.

4. Timing is guaranteed by design and characterization.

5. This represents total input jitter—short term and long term combined—and is guaranteed by design.

6. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

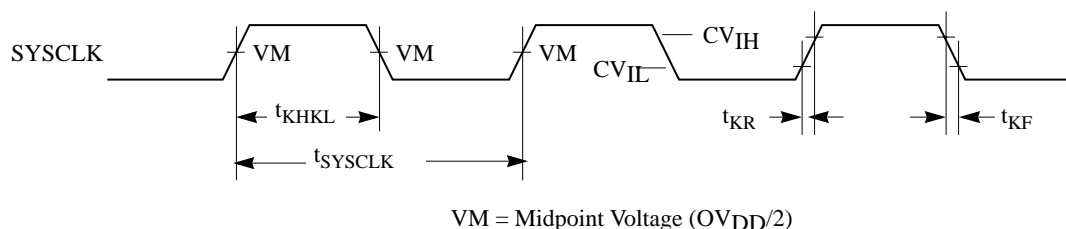Figure 3 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (OV$_{DD}$/2)

**Figure 3. SYSCLK Input Timing Diagram**

## 1.4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7400 as defined in Figure 4 and Figure 5. Timing specifications for the L2 bus are provided in Section 1.4.2.3, "L2 Clock AC Specifications."y

**Table 9. Processor Bus AC Timing Specifications[1]**

At Vdd=AVdd=1.8V±100mV; 0 ≤ Tj ≤ 105°C, OVdd = 3.3V±165mV or OVdd = 2.5V±100mV or OVdd=1.8V±100mV

| Parameter | Symbol[2] | 350, 400 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Mode select input setup to HRESET | $t_{MVRH}$ | 8 | — | $t_{sysclk}$ | 3,4,5,6 |
| HRESET to mode select input hold | $t_{MXRH}$ | 0 | — | ns | 2,3,5 |
| Setup Times: | | | | ns | |
| Address/Transfer Attribute | $t_{AVKH}$ | 1.6 | — | | 7 |
| Transfer Start (TS) | $t_{TSVKH}$ | 1.6 | — | | — |
| Data/Data Parity | $t_{DVKH}$ | 1.6 | — | | 8 |
| ARTRY/SHD0/SHD1 | $t_{ARVKH}$ | 1.6 | — | | — |
| All Other Inputs | $t_{IVKH}$ | 1.6 | — | | 9 |
| Input Hold Times: | | | | ns | |
| Address/Transfer Attribute | $t_{AXKH}$ | 0 | — | | 7 |
| Transfer Start (TS) | $t_{TSXKH}$ | 0 | — | | — |
| Data/Data Parity | $t_{DXKH}$ | 0 | — | | 8 |
| ARTRY/SHD0/SHD1 | $t_{ARXKH}$ | 0 | — | | — |
| All Other Inputs | $t_{IXKH}$ | 0 | — | | 9 |
| Valid Times: | | | | ns | |
| Address/Transfer Attribute | $t_{KHAV}$ | — | 3.2 | | 7 |
| TS, ABB, DBB | $t_{KHTSV}$ | — | 3.4 | | — |
| Data | $t_{KHDV}$ | — | 3.5 | | 8 |
| Data Parity | $t_{KHDPV}$ | — | 3.5 | | 8 |
| ARTRY/SHD0/SHD1 | $t_{KHARV}$ | — | 2.5 | | — |
| All Other Outputs | $t_{KHOV}$ | — | 3.2 | | 10 |

**Table 9. Processor Bus AC Timing Specifications[1] (Continued)**

At Vdd=AVdd=1.8V±100mV; 0 ≤ Tj ≤ 105°C, OVdd = 3.3V±165mV or OVdd = 2.5V±100mV or OVdd=1.8V±100mV

| Parameter | Symbol[2] | 350, 400 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Hold Times: | | | | ns | |
| Address/Transfer Attribute | $t_{KHAX}$ | 0.75 | — | | 7 |
| $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$ | $t_{KHTSX}$ | 0.75 | — | | — |
| Data/Data Parity | $t_{KHDX}$ | 0.6 | — | | 8 |
| $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ | $t_{KHARX}$ | 0.75 | — | | — |
| All Other Outputs | $t_{KHOX}$ | 0.75 | — | | 10 |
| SYSCLK to Output Enable | $t_{KHOE}$ | 0.5 | — | ns | |
| SYSCLK to Output High Impedance (all except $\overline{TS}$, $\overline{ABB}$/AMON(0), $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/DMON(0) ) | $t_{KHOZ}$ | — | 4.0 | ns | |
| SYSCLK to $\overline{TS}$, $\overline{ABB}$/AMON(0), $\overline{DBB}$/DMON(0) High Impedance after precharge | $t_{KHABPZ}$ | — | 1.0 | $t_{sysclk}$ | 5,11,13 |
| Maximum Delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ Precharge | $t_{KHARP}$ | — | 1 | $t_{sysclk}$ | 5,12, 13 |
| SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ High Impedance After Precharge | $t_{KHARPZ}$ | — | 2 | $t_{sysclk}$ | 5,12, 13 |

**Table 9. Processor Bus AC Timing Specifications[1] (Continued)**

At Vdd=AVdd=1.8V±100mV; 0 ≤ Tj ≤ 105°C, OVdd = 3.3V±165mV or OVdd = 2.5V±100mV or OVdd=1.8V±100mV

| Parameter | Symbol[2] | 350, 400 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50 ohm load (See Figure 4). Input and output timings are measured at the pin;time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, $t_{IVKH}$ symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high(H) state or input setup time. And $t_{KHOV}$ symbolizes the time from SYSCLK(K) going high(H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs -and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Motorola PowerPC microprocessors, see the application note "Understanding AC Timing Specifications for PowerPC Microprocessors."

3. The setup and hold time is with respect to the rising edge of HRESET (see Figure 5).

4. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.

5. $t_{sysclk}$ is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

6. Mode select signals are BVSEL, EMODE, L2VSEL, PLL_CFG[0-3]

7. Address/Transfer Attribute signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TBST, TSIZ[0–2], GBL, WT, CI

8. Data signals are composed of the following—DH[0–31], DL[0–31]; Data Parity signals are composed of DP[0–7].

9. All other input signals are composed of the following— AACK, BG, CKSTP_IN, DBG, DBWO/DTI[0], DTI[1-2], HRESET, INT, MCP, QACK, SMI, SRESET, TA, TBEN, TEA, TLBISYNC.

10. All other output signals are composed of the following— BR, CKSTP_OUT, DRDY, HIT, QREQ, RSRV

11. According to the 60x bus protocol, TS, ABB and DBB are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for TS, ABB or DBB is 0.5* $t_{SYSCLK}$, i.e. less than the minimum $t_{SYSCLK}$ period, to ensure that another master asserting TS, ABB, or DBB on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.

12. According to the 60x bus protocol, ARTRY can be driven by multiple bus masters through the clock period immediately following AACK. Bus contention is not an issue since any master asserting ARTRY will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of AACK. The nominal precharge width for ARTRY is 1.0 $t_{sysclk}$; i.e. it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert ARTRY. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.

13. Guaranteed by design and not tested.

**Electrical and Thermal Characteristics**

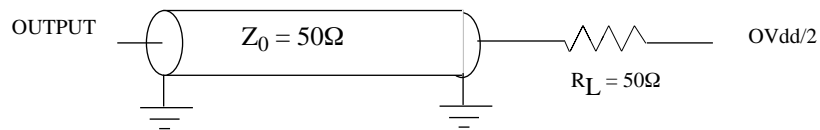Figure 4 provides the AC test load for the MPC7400.



OUTPUT  $Z_0 = 50\Omega$  $R_L = 50\Omega$  OVdd/2

**Figure 4. AC Test Load**

Figure 5 provides the mode select input timing diagram for the MPC7400.



$\overline{\text{HRESET}}$  VM

$t_{MVRH}$  $t_{MXRH}$

MODE SIGNALS

VM = Midpoint Voltage (OV$_{DD}$/2)
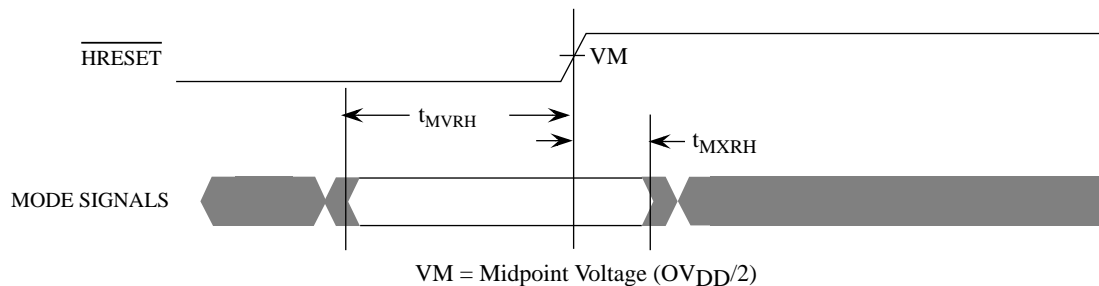
**Figure 5. Mode Input Timing Diagram**

Figure 6 provides the input/output timing diagram for the MPC7400.



$VM = Midpoint Voltage (OV_{DD}/2)$
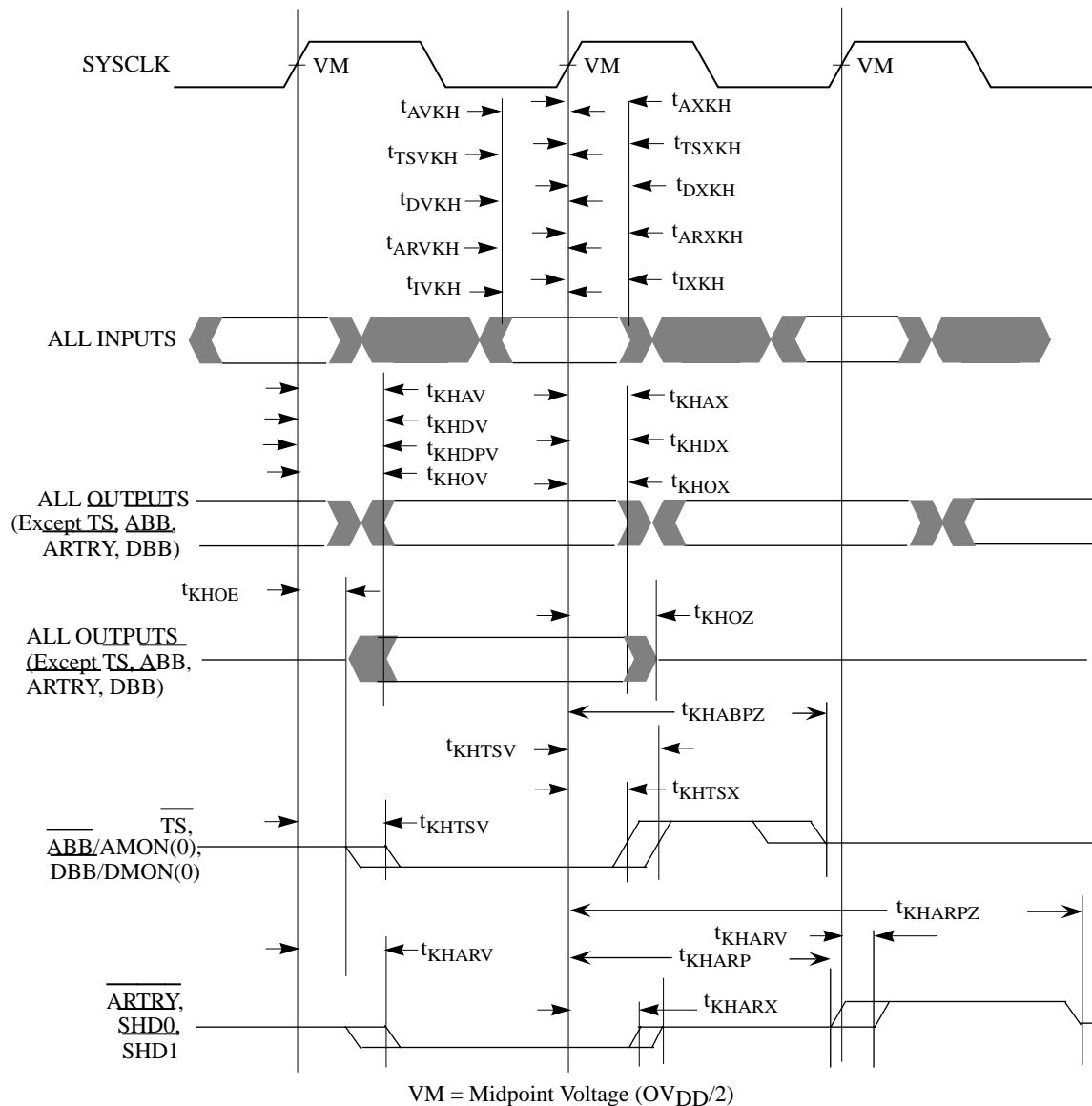
**Figure 6. Input/Output Timing Diagram**

## 1.4.2.3  L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 15 for example core and L2 frequencies at various divisors. Table 10 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC7400 to synchronize L2CLKOUT at the SRAM with the processor's internal clock. L2CLKOUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN179/D "PowerPC™ Backside L2 Timing Analysis for the PCB Design Engineer."

**Electrical and Thermal Characteristics**

The minimum L2CLK frequency of Table 10 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the MPC7400 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 10 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC7400 will be a function of the AC timings of the MPC7400, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 10. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

L2 input and output signals are latched or enabled respectively by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 11 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLKOUTA and L2CLKOUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 11 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

### Table 10. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

| Parameter | Symbol | 350 MHz | | 400 MHz | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| L2CLK frequency | $f_{L2CLK}$ | 100 | 350 | 133 | 400 | MHz | 1,4 |
| L2CLK cycle time | $t_{L2CLK}$ | 2.86 | 10 | 2.5 | 7.5 | ns | |
| L2CLK duty cycle | $t_{CHCL}/t_{L2CLK}$ | 50 | | 50 | | % | 2 |
| Internal DLL-relock time | | 640 | — | 640 | — | L2CLK | 3 |
| DLL capture window | | 0 | 10 | 0 | 10 | ns | 5 |
| L2CLKOUT output-to-output skew | $t_{L2CSKW}$ | | 50 | | 50 | ps | 6 |
| L2CLKOUT output jitter | | | ±150 | | ±150 | ps | 6 |

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent.. L2CLK_OUTA and L2CLK_OUTB must have equal loading.

2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.

3. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.

4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.

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5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.

6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLKOUT and the L2 address/data/control signals equally and therefore is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 7.



VM = Midpoint Voltage (L2OVdd/2)
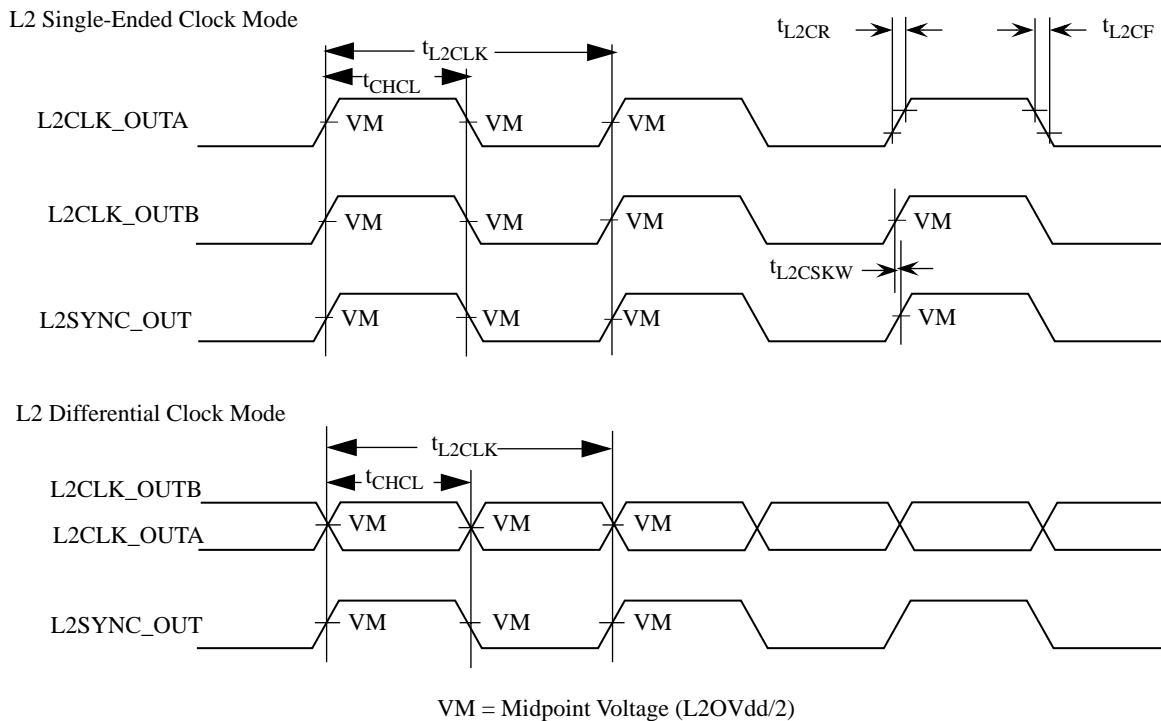
**Figure 7. L2CLK_OUT Output Timing Diagram**

## 1.4.2.4 L2 Bus AC Specifications

Table 11 provides the L2 bus interface AC timing specifications for the MPC7400 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

**Table 11. L2 Bus Interface AC Timing Specifications**

At Vdd=AVdd=L2AVdd=1.8V±100mV; 0 ≤ Tj ≤ 105°C, L2OVdd = 3.3V±165mV or L2OVdd = 2.5V±100mV or L2OVdd=1.8V±100mV

| Parameter | Symbol | 350, 400 MHz | | Unit | Notes |
| --- | --- | --- | --- | --- | --- |
| | | Min | Max | | |
| L2SYNC_IN rise and fall time | $t_{L2CR}$ & $t_{L2CF}$ | — | 1.0 | ns | 1 |
| Setup Times: | | | | ns | 2 |
|         Data and parity | $t_{DVL2CH}$ | 1.5 | — | | |
| Input Hold Times: | | | | ns | 2 |
|         Data and parity | $t_{DXL2CH}$ | 0.0 | — | | |

**Table 11. L2 Bus Interface AC Timing Specifications (Continued)**

At Vdd=AVdd=L2AVdd=1.8V±100mV; 0 ≤ Tj ≤ 105°C, L2OVdd = 3.3V±165mV or L2OVdd = 2.5V±100mV or L2OVdd=1.8V±100mV

| Parameter | Symbol | 350, 400 MHz | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Valid Times:<br><br>All outputs when L2CR[14-15] = 00<br>All outputs when L2CR[14-15] = 01<br>All outputs when L2CR[14-15] = 10<br>All outputs when L2CR[14-15] = 11 | $t_{L2CHOV}$ | -<br>-<br>-<br>- | 2.5<br>3.0<br>3.5<br>4.0 | ns | 3,4 |
| Output Hold Times<br><br>All outputs when L2CR[14-15] = 00<br>All outputs when L2CR[14-15] = 01<br>All outputs when L2CR[14-15] = 10<br>All outputs when L2CR[14-15] = 11 | $t_{L2CHOX}$ | 0.4<br>1.0<br>1.4<br>1.8 | -<br>-<br>-<br>- | ns | 3 |
| L2SYNC_IN to high impedance:<br><br>All outputs when L2CR[14-15] = 00<br>All outputs when L2CR[14-15] = 01<br>All outputs when L2CR[14-15] = 10<br>All outputs when L2CR[14-15] = 11 | $t_{L2CHOZ}$ | -<br>-<br>-<br>- | 2.0<br>2.5<br>3.0<br>3.5 | ns | |

Notes:

1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of L2OVdd.

2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.

3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 ohm load (See Figure 10).

4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous burst RAMs, L2CR[14–15] = 00 is recommended. For pipelined late-write synchronous burst SRAMs, L2CR[14–15] = 10 is recommended.

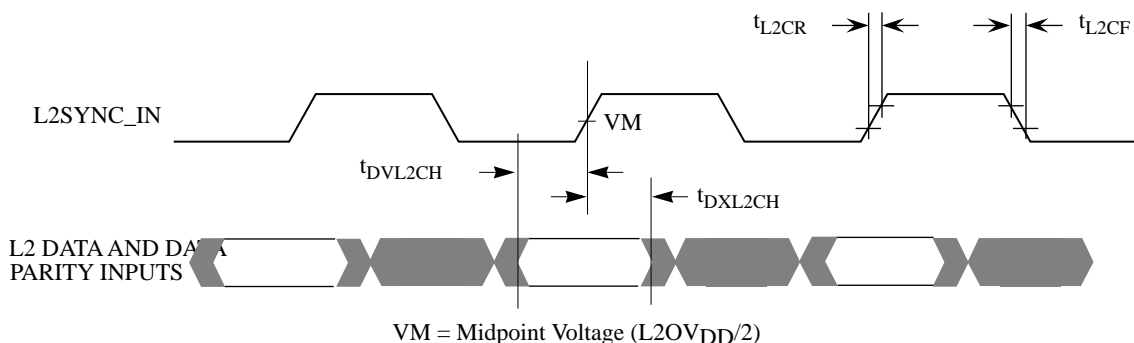Figure 8 shows the L2 bus input timing diagrams for the MPC7400.



VM = Midpoint Voltage (L2OV$_{DD}$/2)

**Figure 8. L2 Bus Input Timing Diagrams**

Figure 9 shows the L2 bus output timing diagrams for the MPC7400.



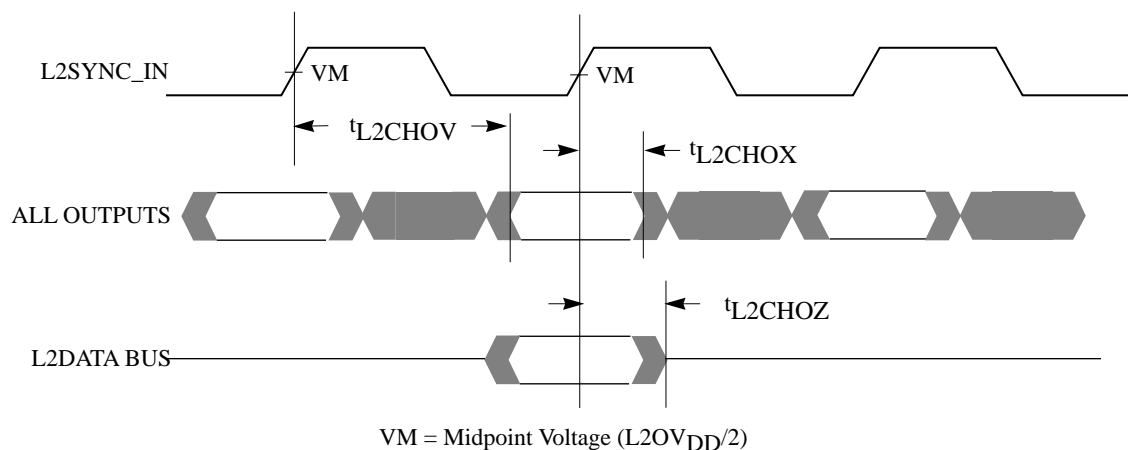VM = Midpoint Voltage (L2OV$_{DD}$/2)

**Figure 9. L2 Bus Output Timing Diagrams**

Figure 10 provides the AC test load for L2 interface of the MPC7400.
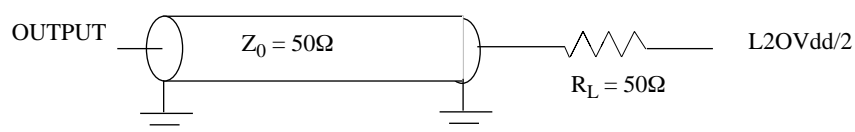


**Figure 10. AC Test Load for the L2 Interface**

## 1.4.2.5  IEEE 1149.1 AC Timing Specifications

Table 12 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12, Figure 13, Figure 14, and Figure 15.

**Table 12. JTAG AC Timing Specifications (Independent of SYSCLK)[1]**

At recommended operating conditions (See Table 3)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| TCK frequency of operation | $f_{TCLK}$ | 0 | 33.3 | MHz | |
| TCK cycle time | $t_{TCLK}$ | 30 | — | ns | |
| TCK clock pulse width measured at 1.4V | $t_{JHJL}$ | 15 | — | ns | |
| TCK rise and fall times | $t_{JR}$ & $t_{JF}$ | 0 | 2 | ns | |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 2 |
| Input Setup Times: | | | | ns | 3 |
| Boundary-scan data | $t_{DVJH}$ | 4 | — | | |
| TMS, TDI | $t_{IVJH}$ | 0 | — | | |
| Input Hold Times: | | | | ns | 3 |
| Boundary-scan data | $t_{DXJH}$ | 20 | — | | |
| TMS, TDI | $t_{IXJH}$ | 25 | — | | |

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**Table 12. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (Continued)**

At recommended operating conditions (See Table 3)

| Parameter | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Valid Times: | | | | | ns | |
| | Boundary-scan data | $t_{JLDV}$ | 4 | 20 | | 4 |
| | TDO | $t_{JLOV}$ | 4 | 25 | | |
| Output Hold Times: | | | | | | |
| | Boundary-scan data | $t_{JLDX}$ | | | | |
| | TDO | $t_{JLOX}$ | | | | |
| TCK to output high impedance: | | | | | ns | |
| | Boundary-scan data | $t_{JLDZ}$ | 3 | 19 | | 4,5 |
| | TDO | $t_{JLOZ}$ | 3 | 9 | | 5 |

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 ohm load (See Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC7400.
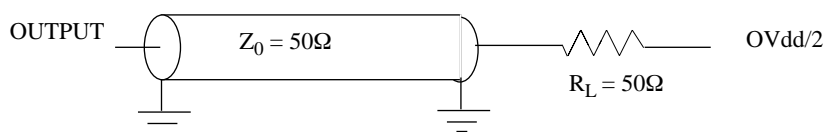


**Figure 11. Alternate AC Test Load for the JTAG Interface**
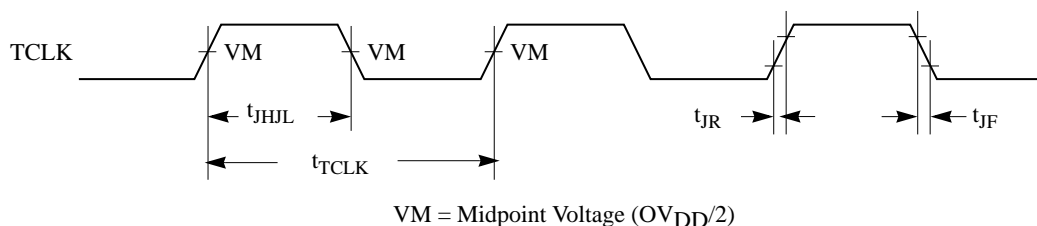
Figure 12 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV$_{DD}$/2)

**Figure 12. JTAG Clock Input Timing Diagram**

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.



VM = Midpoint Voltage (OV$_{DD}$/2)
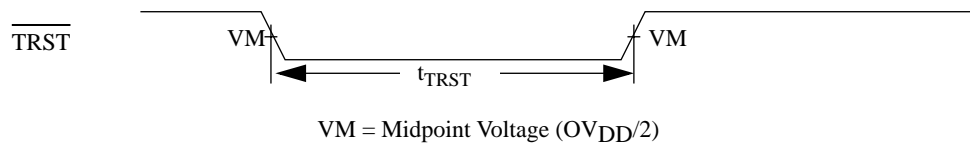
**Figure 13. $\overline{\text{TRST}}$ Timing Diagram**

Figure 14 provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV$_{DD}$/2)
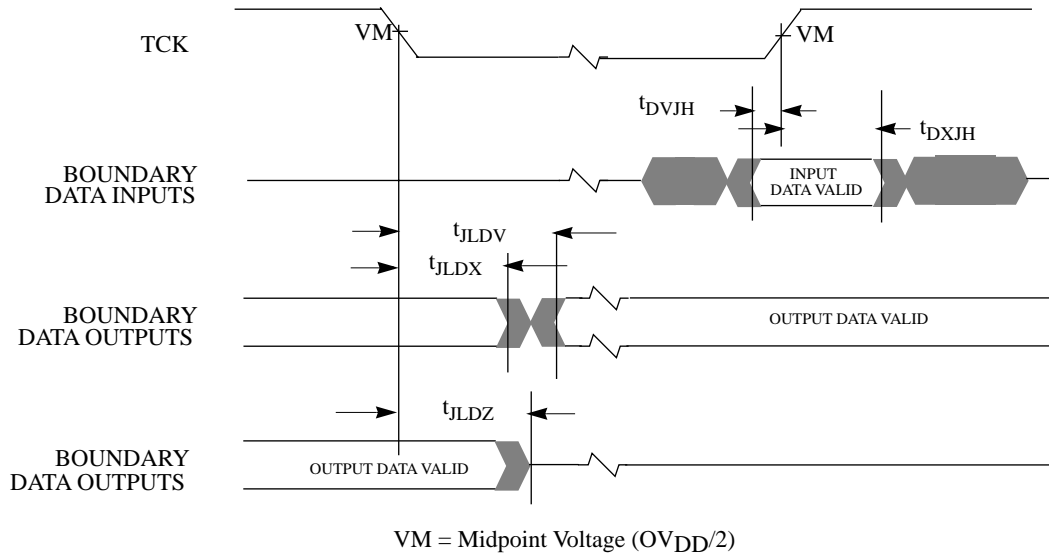
**Figure 14. Boundary-Scan Timing Diagram**

Figure 15 provides the test access port timing diagram.



VM = Midpoint Voltage (OV$_{DD}$/2)
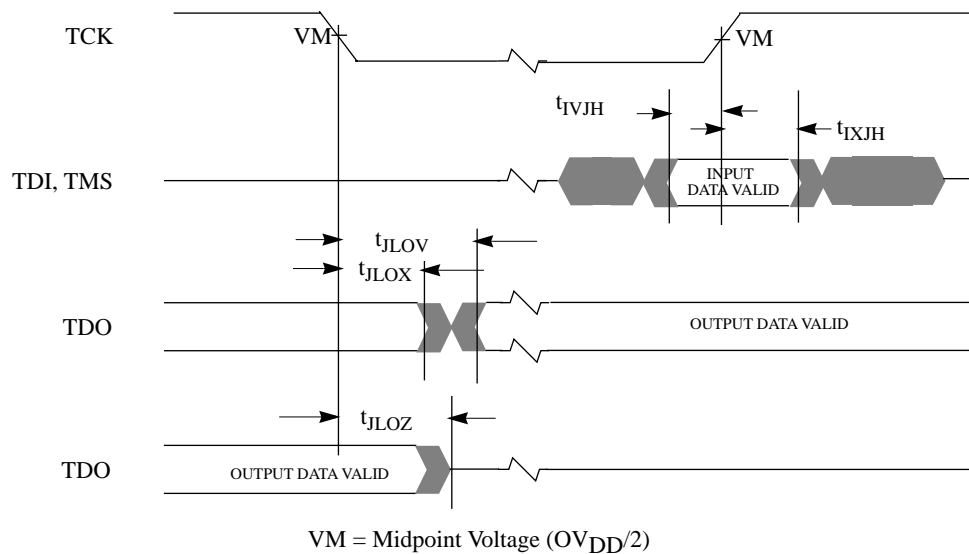
**Figure 15. Test Access Port Timing Diagram**

## 1.5 Pin Assignments

Figure 16 (in part A) shows the pinout of the MPC7400, 360 CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.
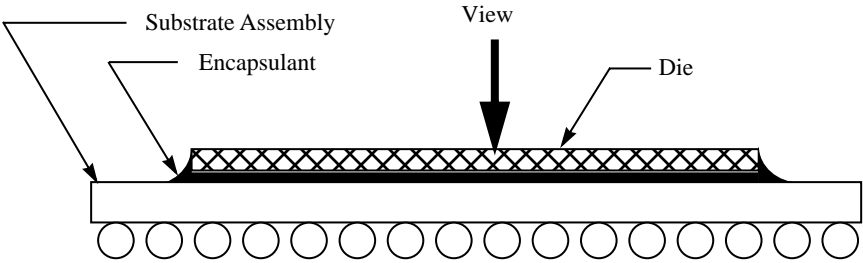
Part A



Not to Scale
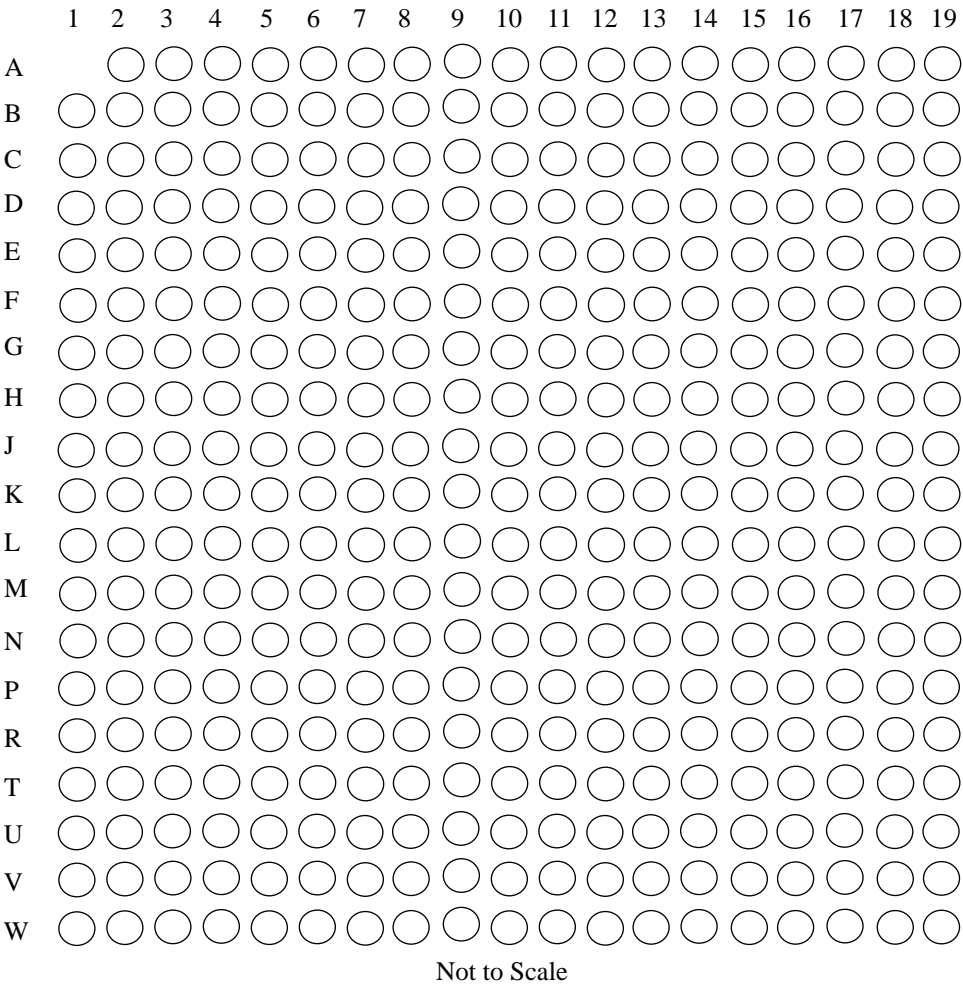
Part B



**Figure 16. Pinout of the MPC7400, 360 CBGA Package as Viewed from the Top Surface**

# 1.6 Pinout Listings

Table 13 provides the pinout listing for the MPC7400, 360 CBGA package.

**Table 13. Pinout Listing for the MPC7400, 360 CBGA Package**

| Signal Name | Pin Number | Active | I/O | I/F Voltages Supported[1] | | | Notes |
|---|---|---|---|---|---|---|---|
| | | | | 1.8v | 2.5v | 3.3v | |
| A[0–31] | A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2 | High | I/O | √ | √ | √ | |
| AACK | N3 | Low | Input | √ | √ | √ | |
| ABB AMON(0) | L7 | Low | Output | √ | √ | √ | 12 |
| AP[0–3] | C4, C5, C6, C7 | High | I/O | √ | √ | √ | |
| ARTRY | L6 | Low | I/O | √ | √ | √ | |
| AVDD | A8 | — | Input | 1.8V | 1.8V | 1.8V | |
| BG | H1 | Low | Input | √ | √ | √ | |
| BR | E7 | Low | Output | √ | √ | √ | |
| BVSEL | W1 | High | Input | GND | HRESET | 3.3V | 3, 8, 9 |
| CHK | K11 | Low | Input | √ | √ | √ | 4, 8, 9 |
| CI | C2 | Low | I/O | √ | √ | √ | |
| CKSTP_IN | B8 | Low | Input | √ | √ | √ | |
| CKSTP_OUT | D7 | Low | Output | √ | √ | √ | |
| CLK_OUT | E3 | High | Output | √ | √ | √ | |
| DBB DMON(0) | K5 | Low | Output | √ | √ | √ | 12 |
| DBG | K1 | Low | Input | √ | √ | √ | |
| DH[0–31] | W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5 | High | I/O | √ | √ | √ | |
| DL[0-31] | M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2 | High | I/O | √ | √ | √ | |
| DP[0–7] | L1, P2, M2, V2, M1, N2, T3, R1 | High | I/O | √ | √ | √ | |
| DRDY | K9 | Low | Output | √ | √ | √ | 6, 8, 13 |
| DBWO DTI[0] | D1 | Low | Input | √ | √ | √ | |
| DTI[1-2] | H6, G1 | High | Input | √ | √ | √ | 10, 13 |
| EMODE | A3 | Low | Input | √ | √ | √ | 7, 10 |

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**Table 13. Pinout Listing for the MPC7400, 360 CBGA Package  (Continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltages Supported[1] | | | Notes |
|---|---|---|---|---|---|---|---|
| | | | | 1.8v | 2.5v | 3.3v | |
| GBL | B1 | Low | I/O | √ | √ | √ | |
| GND | D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16 | — | — | GND | GND | GND | |
| HIT | B5 | Low | Output | √ | √ | √ | 6, 8 |
| HRESET | B6 | Low | Input | √ | √ | √ | |
| INT | C11 | Low | Input | √ | √ | √ | |
| L1_TSTCLK | F8 | High | Input | √ | √ | √ | 2 |
| L2ADDR[0–16] | L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18 | High | Output | √ | √ | √ | |
| L2ADDR[17] | K19 | High | Output | √ | √ | √ | 8 |
| L2ASPARE | W19 | High | Output | √ | √ | √ | 8 |
| L2AVDD | L13 | — | Input | 1.8V | 1.8V | 1.8V | |
| L2CE | P17 | Low | Output | √ | √ | √ | |
| L2CLKOUTA | N15 | High | Output | √ | √ | √ | |
| L2CLKOUTB | L16 | High | Output | √ | √ | √ | |
| L2DATA[0–63] | U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13 | High | I/O | √ | √ | √ | |
| L2DP[0–7] | V14, U16, T19, N18, H14, F17, C19, B15 | High | I/O | √ | √ | √ | |
| L2OVDD | D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15 | — | — | 1.8V | 2.5V | 3.3V | 11 |
| L2SYNC_IN | L14 | High | Input | √ | √ | √ | |
| L2SYNC_OUT | M14 | High | Output | √ | √ | √ | |
| L2_TSTCLK | F7 | High | Input | √ | √ | √ | 2 |
| L2VSEL | A19 | High | Input | GND | HRESET | 3.3V | 1, 3, 8, 9 |
| L2WE | N16 | Low | Output | √ | √ | √ | |
| L2ZZ | G17 | High | Output | √ | √ | √ | |

**Table 13. Pinout Listing for the MPC7400, 360 CBGA Package  (Continued)**

| Signal Name | Pin Number | Active | I/O | I/F Voltages Supported[1] | | | Notes |
|---|---|---|---|---|---|---|---|
| | | | | 1.8v | 2.5v | 3.3v | |
| $\overline{\text{LSSD\_MODE}}$ | F9 | Low | Input | √ | √ | √ | 2 |
| $\overline{\text{MCP}}$ | B11 | Low | Input | √ | √ | √ | |
| OVDD | D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12 | — | — | 1.8V | 2.5V | 3.3V | |
| PLL_CFG[0–3] | A4, A5, A6, A7 | High | Input | √ | √ | √ | |
| $\overline{\text{QACK}}$ | B2 | Low | Input | √ | √ | √ | |
| $\overline{\text{QREQ}}$ | J3 | Low | Output | √ | √ | √ | |
| $\overline{\text{RSRV}}$ | D3 | Low | Output | √ | √ | √ | |
| $\overline{\text{SHD0}}$ | B3 | Low | I/O | √ | √ | √ | 8 |
| $\overline{\text{SHD1}}$ | B4 | Low | I/O | √ | √ | √ | 5, 8 |
| $\overline{\text{SMI}}$ | A12 | Low | Input | √ | √ | √ | |
| $\overline{\text{SRESET}}$ | E10 | Low | Input | √ | √ | √ | |
| SYSCLK | H9 | — | Input | √ | √ | √ | |
| $\overline{\text{TA}}$ | F1 | Low | Input | √ | √ | √ | |
| TBEN | A2 | High | Input | √ | √ | √ | |
| $\overline{\text{TBST}}$ | A11 | Low | Output | √ | √ | √ | |
| TCK | B10 | High | Input | √ | √ | √ | |
| TDI | B7 | High | Input | √ | √ | √ | 9 |
| TDO | D9 | High | Output | √ | √ | √ | |
| $\overline{\text{TEA}}$ | J1 | Low | Input | √ | √ | √ | |
| TMS | C8 | High | Input | √ | √ | √ | 9 |
| $\overline{\text{TRST}}$ | A10 | Low | Input | √ | √ | √ | 9 |
| $\overline{\text{TS}}$ | K7 | Low | I/O | √ | √ | √ | |
| TSIZ[0–2] | A9, B9, C9 | High | Output | √ | √ | √ | |
| TT[0–4] | C10, D11, B12, C12, F11 | High | I/O | √ | √ | √ | |
| $\overline{\text{WT}}$ | C3 | Low | I/O | √ | √ | √ | |
| VDD | G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12 | — | — | 1.8V | 1.8V | 1.8V | |

Notes:

1. OVdd supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{\text{L2CE}}$, $\overline{\text{L2WE}}$, and L2ZZ); L2OVDD supplies power to the L2 cache interface (L2ADDR[0-16], L2ASPARE, L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and Vdd supplies power to the processor core and the PLL and DLL (after filtering to become AVDD and L2AVDD respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of Vin or supply voltages see Table 3.

2. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.

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3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OVDD (selects 3.3v), OGND (selects 1.8v), or to HRESET (selects 2.5v). The Processor bus and L2 bus support all 3 options. (See Table 2. Input Threshold Voltage Setting)

4. Connect to HRESET to trigger post power-on-reset (por) internal memory test.

5. Ignored in 60x bus mode.

6. Unused output in 60x bus mode.

7. Deasserted (pulled high) at HRESET for 60x bus mode.

8. Uses one of 9 existing no-connects in MPC750's 360-BGA package.

9. Internal pull up on die.

10. Reuses MPC750's DRTRY, DBDIS, and TLBISYNC pins (DTI1, DTI2, and EMODE respectively).

11. The VOLTDET pin position on the MPC750 360-CBGA package is now an L2OVDD pin on the MPC7400 360-CBGA package.

12. Output only for MPC7400, was I/O for MPC750.

13. Enhanced mode only.

# 1.7  Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC7400, 360 CBGA packages.

## 1.7.1  Package Parameters for the MPC7400

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead ceramic ball grid array (CBGA).

| | |
|---|---|
| Package outline | 25 x 25 mm |
| Interconnects | 360 (19 x 19 ball array - 1) |
| Pitch | 1.27 mm (50 mil) |
| Minimum module height | 2.65 mm |
| Maximum module height | 3.20 mm |
| Ball diameter | 0.89 mm (35 mil) |

## 1.7.2  Mechanical Dimensions of the MPC7400

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the MPC7400, 360 CBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

| DIM | Millimeters | |
| --- | --- | --- |
| | MIN | MAX |
| A | 2.65 | 3.20 |
| A1 | 0.79 | 0.99 |
| A2 | 1.10 | 1.30 |
| A3 | -- | 0.6 |
| A4 | 0.82 | 0.9 |
| b | 0.82 | 0.93 |
| C1-1 | L2OVDD | |
| C1-2 | GND | |
| C2-1 | L2OVDD | |
| C2-2 | GND | |
| C3-1 | VDD | |
| C3-2 | GND | |
| C4-1 | OVDD | |
| C4-2 | GND | |
| C5-1 | OVDD | |
| C5-2 | GND | |
| C6-1 | VDD | |
| C6-2 | GND | |
| D | 25.00 BSC | |
| D2 | 9.6 typ. | |
| D3 | 7.85 | |
| e | 1.27 BSC | |
| E | 25.00 BSC | |
| E2 | 12.3 typ. | |
| E3 | 10.58 | |
| J1 | 0.89 BSC | |
| J2 | 3.2 BSC | |
| J3 | 0.68 BSC | |
| K1 | 6.56 | |
| K2 | 8.13 | |
| L1 | 9.04 | |
| L2 | 7.47 | |
| M | | 2.00 |

**Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC7400**

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# 1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC7400.

## 1.8.1 PLL Configuration

The MPC7400's PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7400 is shown in Table 14 for example frequencies.

**Table 14. MPC7400 Microprocessor PLL Configuration**

| PLL_CFG [0–3] | Bus-to-Core Multiplier | Core-to VCO Multiplier | Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Bus 25 MHz | Bus 33.3 MHz | Bus 50 MHz | Bus 66.6 MHz | Bus 75 MHz | Bus 100 MHz |
| 0100 | 2x | 2x | | | | | | |
| 0110 | 2.5x | 2x | | | | | | |
| 1000 | 3x | 2x | | | | | | 300 (600) |
| 1110 | 3.5x | 2x | | | | | | 350 (700) |
| 1010 | 4x | 2x | | | | | 300 (600) | 400 (800) |
| 0111 | 4.5x | 2x | | | | 300 (600) | 337 (675) | 450 (900) |
| 1011 | 5x | 2x | | | | 333 (666) | 375 (750) | |
| 1001 | 5.5x | 2x | | | | 366 (733) | 412 (825) | |
| 1101 | 6x | 2x | | | 300 (600) | 400 (800) | 450 (900) | |
| 0101 | 6.5x | 2x | | | 325 (630) | 433 (866) | | |
| 0010 | 7x | 2x | | | 350 (700) | | | |
| 0001 | 7.5x | 2x | | | 375 (750) | | | |
| 1100 | 8x | 2x | | | 400 (800) | | | |
| 0000 | 9x | 2x | | 300 (600) | 450 (900) | | | |
| 0011 | PLL off/bypass | | PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied | | | | | |

**Table 14. MPC7400 Microprocessor PLL Configuration (Continued)**

| PLL_CFG [0–3] | Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Bus-to-Core Multiplier | Core-to-VCO Multiplier | Bus 25 MHz | Bus 33.3 MHz | Bus 50 MHz | Bus 66.6 MHz | Bus 75 MHz | Bus 100 MHz |
| 1111 | PLL off | | PLL off, no core clocking occurs | | | | | |

Notes:

1. PLL_CFG[0–3] settings not listed are reserved.

2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC7400; see Section 1.4.2.1, "Clock AC Specifications," for valid SYSCLK, core, and VCO frequencies.

3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.

4. In PLL-off mode, no clocking occurs inside the MPC7400 regardless of the SYSCLK input.

The MPC7400 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC7400. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC7400 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC7400 core, and the phase adjustment range that the L2 DLL supports. Table 15 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 100MHz.

**Table 15. Sample Core-to-L2 Frequencies**

| Core Frequency in MHz | ÷1 | ÷1.5 | ÷2 | ÷2.5 | ÷3 | ÷3.5 | ÷4 |
|---|---|---|---|---|---|---|---|
| 300 | 300 | 200 | 150 | 120 | 100 | — | — |
| 333 | 333 | 222 | 166 | 133 | 111 | — | — |
| 350 | — | — | 175 | 140 | 117 | 100 | — |
| 366 | — | — | 183 | 147 | 122 | 105 | — |
| 400 | — | — | 200 | 160 | 133 | 114 | 100 |

Note:

1. The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC7400; see Section 1.4.2.3, "L2 Clock AC Specifications," for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

# 1.8.2  PLL Power Supply Filtering

The AVdd and L2AVdd power signals are provided on the MPC7400 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered of any noise in the 500kHz to 10MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 18 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended.

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The circuit should be placed as close as possible to the AVdd pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the L2AVdd pin. It is often possible to route directly from the capacitors to the AVdd pin, which is on the periphery of the 360 CBGA footprint, without the inductance of vias. The L2AVdd pin may be more difficult to route but is proportionately less critical.
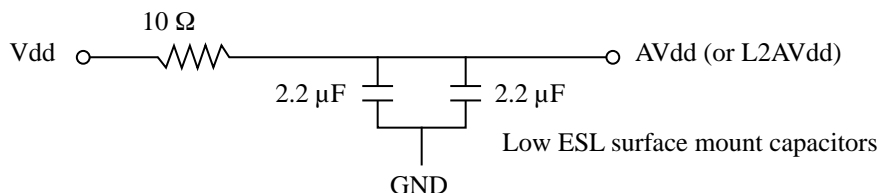


**Figure 18. PLL Power Supply Filter Circuit**

## 1.8.3 Power Supply Voltage Sequencing

The notes in Table 1 contain cautions about the sequencing of the external bus voltages and core voltage of the MPC7400 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, one or both of the circuits of Figure 19 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 19 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.
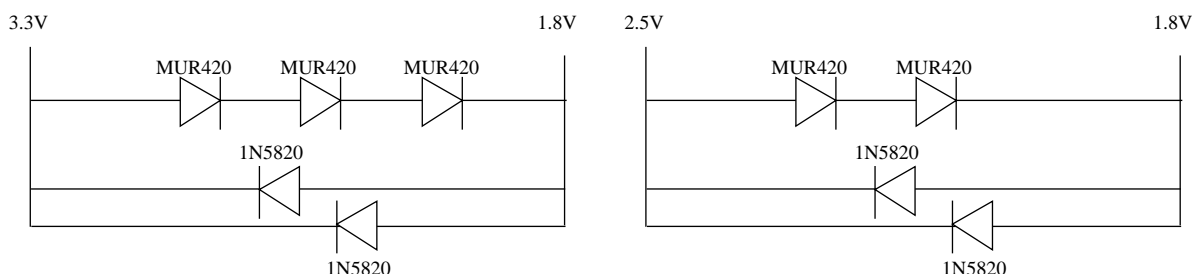


**Figure 19. Example Voltage Sequencing Circuits**

## 1.8.4 Decoupling Recommendations

Due to the MPC7400's dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7400 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7400 system, and the MPC7400 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd, OVdd, and L2OVdd pin of the MPC7400. It is also recommended that these decoupling capacitors receive their power from separate Vdd, (L2)OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard

Johnson in <u>High Speed Digital Design: A Handbook of Black Magic</u> (Prentice Hall, 1993) and contrary to previous recommendations for decoupling PowerPC microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd, L2OVdd, and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100-330 µF (AVX TPS tantalum or Sanyo OSCON).

## 1.8.5  Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OVdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, L2OVdd, and GND pins of the MPC7400.

See Section 1.4.2.3, "L2 Clock AC Specifications" for a discussion of the L2SYNC_OUT and L2SYNC_IN signals.

## 1.8.6  Output Buffer DC Impedance

The MPC7400 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure $Z_0$, an external resistor is connected from the chip pad to OVdd or GND. Then, the value of each resistor is varied until the pad voltage is OVdd/2 (see Figure 20).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and $R_N$ is trimmed until the voltage at the pad equals OVdd/2. $R_N$ then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and $R_P$ is trimmed until the voltage at the pad equals OVdd/2. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.
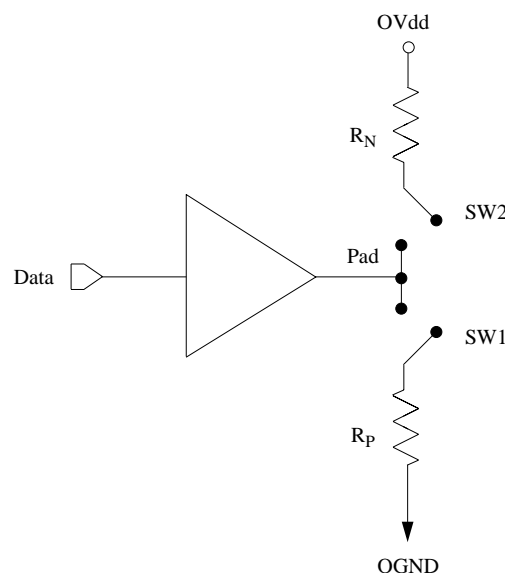


**Figure 20. Driver Impedance Measurement**

Table 16 summarizes the signal impedance results. The driver impedance values were characterized at 0°C, 65 °C, and 105 °C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

**Table 16. Impedance Characteristics**

Vdd = 1.8V, OVdd = 3.3V, Tj = 0 - 105 °C

| Impedance | Processor bus | L2 bus | Symbol | Unit |
|---|---|---|---|---|
| $R_N$ | 32-43 | 39-48 | $Z_0$ | Ohms |
| $R_P$ | 36-48 | 41-50 | $Z_0$ | Ohms |

## 1.8.7  Pull-up Resistor Requirements

The MPC7400 requires high-resistive (weak: 10 KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7400 or other bus masters. These pins are TS, ARTRY, SHDO, and SHD1.

In addition, the MPC7400 has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 KΩ–10 KΩ) if it is used by the system. This pin is CKSTP_OUT.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may therefore float in the high-impedance state for relatively long periods of time. Since the MPC7400 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the MPC7400 or by other receivers in the system. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors by the system, or that they may be otherwise driven by the system during inactive periods of the bus. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], and GBL.

The data bus input receivers are normally turned off when no read operation is in progress and therefore do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pullups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: D[0:63], DP[0:7]

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not normally require pull-up resistors.

## 1.8.8  JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. (BSDL descriptions of the MPC7400 are available on the internet at www.mot.com/PowerPC/teksupport.) The TRST signal is optional in the IEEE 1149.1 specification but is provided on all PowerPC implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors, simply tying TRST to HRESET isn't practical.

The common on-chip processor (COP) function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert

$\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 21 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while insuring that the target can drive HRESET as well. The pull-down resistor on TRST ensures that the JTAG scan chain is initialized during power-on if a JTAG interface cable is not attached; if it is, it is responsible for driving TRST when needed.
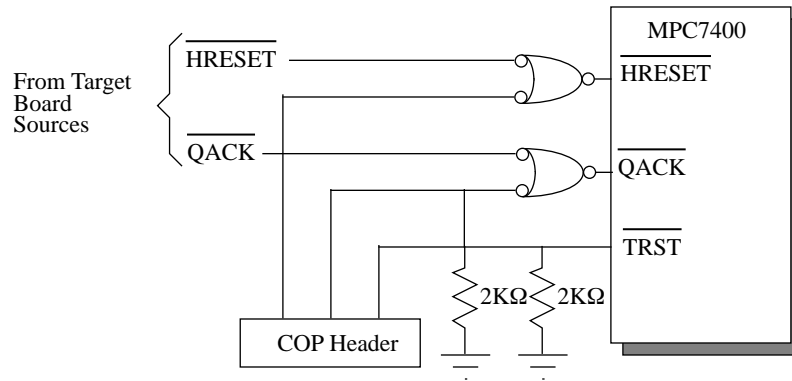


**Figure 21. Suggested TRST connection**

The COP header shown in Figure 21 adds many benefits—breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a "Berg" header). The connector typically has pin 14 removed as a connector key, as shown in Figure 22.
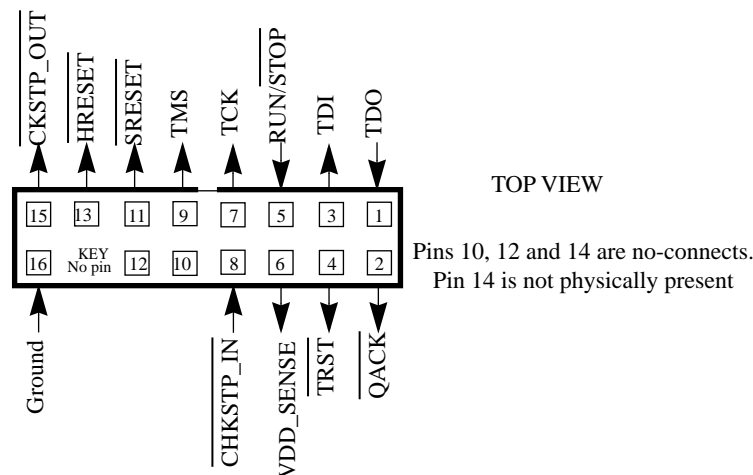


**Figure 22. COP Connector Diagram**

There is no standardized way to number the COP header shown in Figure 22; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin one (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 22 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Table 17 is usually hooked up to the PCI bridge chip in a system and is an input to the MPC7400 informing it that it can go into the quiescent state. Under normal operation this occurs during a low power mode selection. In order for COP to work the MPC7400 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. To preserve correct power down operation, QACK should be merged so that it also can be driven by the PCI bridge.

Table 17 shows the pin definitions.

**Table 17. COP Pin Definitions**

| Pins | Signal | Connection | Special Notes |
|------|--------|------------|---------------|
| 1 | TDO | TDO | |
| 2 | $\overline{\text{QACK}}$ | $\overline{\text{QACK}}$ | Add 2K pulldown to ground. Must be merged with on-board $\overline{\text{QACK}}$, if any. |
| 3 | TDI | TDI | |
| 4 | $\overline{\text{TRST}}$ | $\overline{\text{TRST}}$ | Add 2K pulldown to ground. Must be merged with on-board $\overline{\text{TRST}}$, if any. See Figure 21 |
| 5 | $\overline{\text{RUN}}$/STOP | No Connect | Used on 604e; leave no-connect for all other processors. |
| 6 | VDD_SENSE | VDD | Add 2K pullup to OVDD (for short circuit limiting protection only). |
| 7 | TCK | TCK | |
| 8 | CKSTP_IN | CKSTP_IN | Optional. Add 10K pullup to OVDD. Used on several emulator products. Useful for checkstopping the processor from a logic analyzer of other external trigger. |
| 9 | TMS | TMS | |
| 10 | N/A | | |
| 11 | $\overline{\text{SRESET}}$ | $\overline{\text{SRESET}}$ | Merge with on-board $\overline{\text{SRESET}}$, if any. |
| 12 | N/A | | |
| 13 | $\overline{\text{HRESET}}$ | $\overline{\text{HRESET}}$ | Merge with on-board $\overline{\text{HRESET}}$. |
| 14 | N/A | | Key location; pin should be removed. |
| 15 | CKSTP_OUT | CKSTP_OUT | Add 10K pullup to OVDD. |
| 16 | Ground | Digital Ground | |

# 1.8.9 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 23. This spring force should not exceed 5.5 pounds of force.
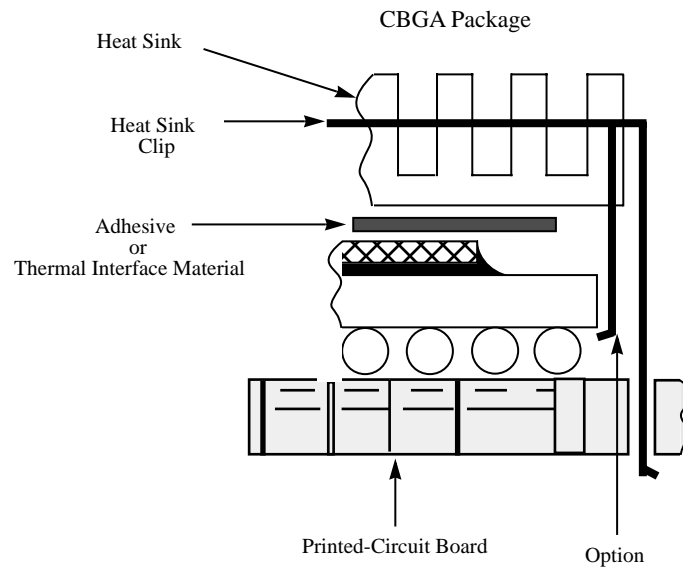
**Figure 23. Package Exploded Cross-Sectional View with Several Heat Sink Options**

The board designer can choose between several types of heat sinks to place on the MPC7400. There are several commercially-available heat sinks for the MPC7400 provided by the following vendors:

Chip Coolers Inc.                                              800-227-0254 (USA/Canada)
333 Strawberry Field Rd.                                      401-739-7600
Warwick, RI 02887-6979

International Electronic Research Corporation (IERC)818-842-7277
135 W. Magnolia Blvd.
Burbank, CA 91502

Thermalloy                                                    214-243-4321
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75731

Wakefield Engineering                                         617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Aavid Engineering                                             603-528-3400
One Kool Path
Laconia, NH 03247-0440

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

## 1.8.9.1  Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 3, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 24 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)
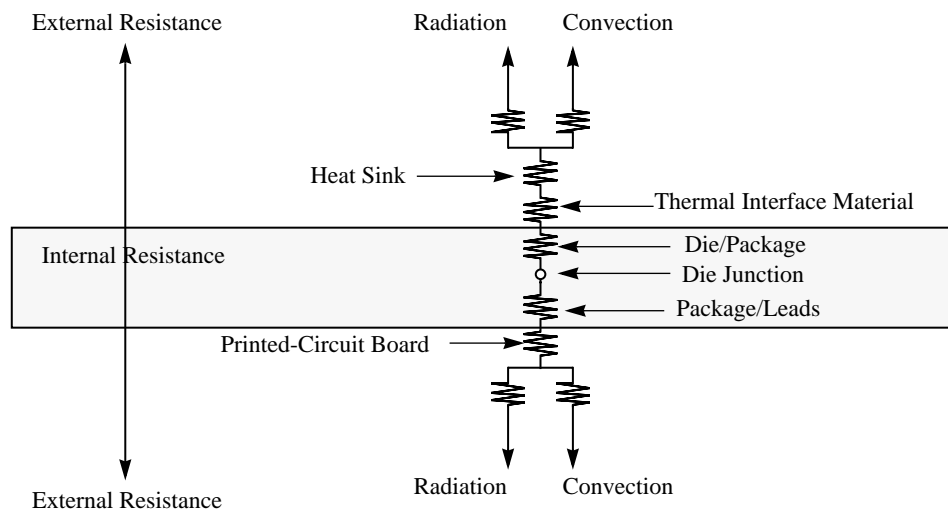
**Figure 24. C4 Package with Heat Sink Mounted to a Printed-Circuit Board**

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

## 1.8.9.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 25 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 24). This spring force should not exceed 10 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.
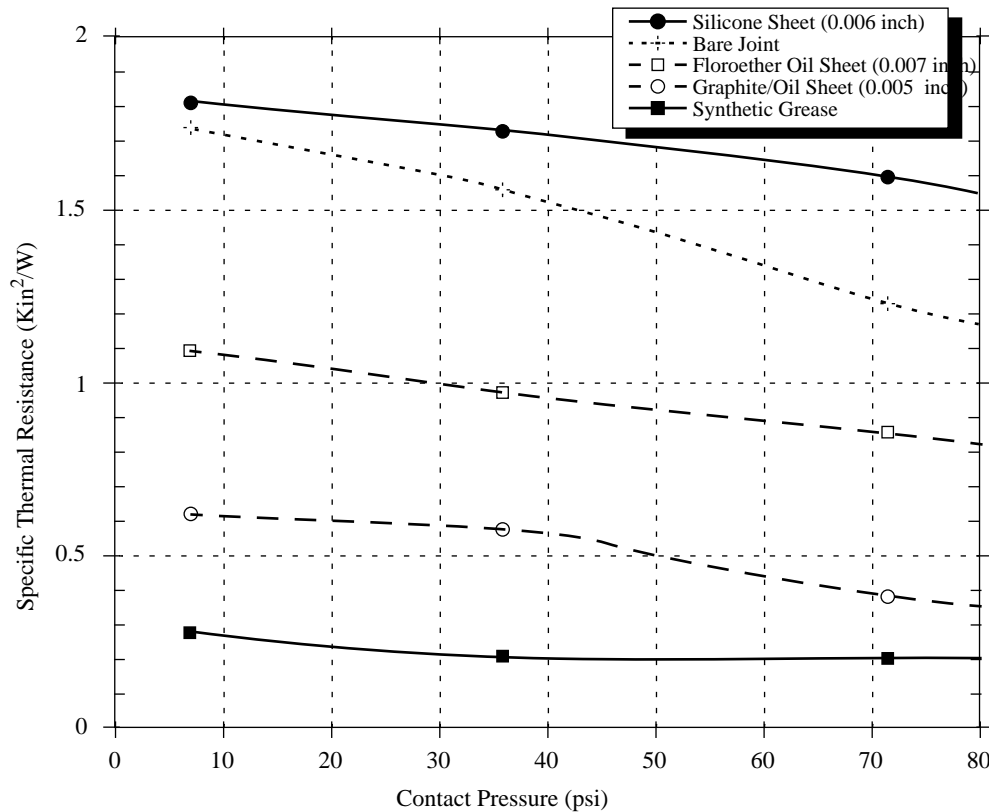
**Figure 25. Thermal Performance of Select Thermal Interface Material**

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation                            517-496-4000
Dow-Corning Electronic Materials
PO Box 0997
Midland, MI 48686-0997

Chomerics, Inc.                                    617-935-4850
77 Dragon Court
Woburn, MA 01888-4850

Thermagon Inc.                                     216-741-7659
3256 West 25th Street
Cleveland, OH 44109-1668

Loctite Corporation                                860-571-5100
1001 Trout Brook Crossing
Rocky Hill, CT 06067

AI Technology (e.g. EG7655)                        609-882-2332
1425 Lower Ferry Rd.
Trent, NJ 08618

## 1.8.9.3 Heat Sink Selection Example

The following section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

$T_j$ is the die-junction temperature

$T_a$ is the inlet cabinet ambient temperature

$T_r$ is the air temperature rise within the computer cabinet

$\theta_{jc}$ is the junction-to-case thermal resistance

$\theta_{int}$ is the adhesive or interface material thermal resistance

$\theta_{sa}$ is the heat sink base-to-ambient thermal resistance

$P_d$ is the power dissipated by the device

During operation the die-junction temperatures ($T_j$) should be maintained less than the value specified in Table 3. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature ($T_a$) may range from 30 to 40 °C. The air temperature rise within a cabinet ($T_r$) may be in the range of 5 to 10 °C. The thermal resistance of the thermal interface material ($\theta_{int}$) is typically about 1 °C/W. Assuming a $T_a$ of 30 °C, a $T_r$ of 5 °C, a CBGA package $\theta_{jc} = 0.03$, and a power consumption ($P_d$) of 5.0 watts, the following expression for $T_j$ is obtained:

Die-junction temperature: $T_j = 30$ °C $+ 5$ °C $+ (0.03$ °C/W $+ 1.0$ °C/W $+ \theta_{sa}) * 5.0$ W

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance ($\theta_{sa}$) versus airflow velocity is shown in Figure 26.
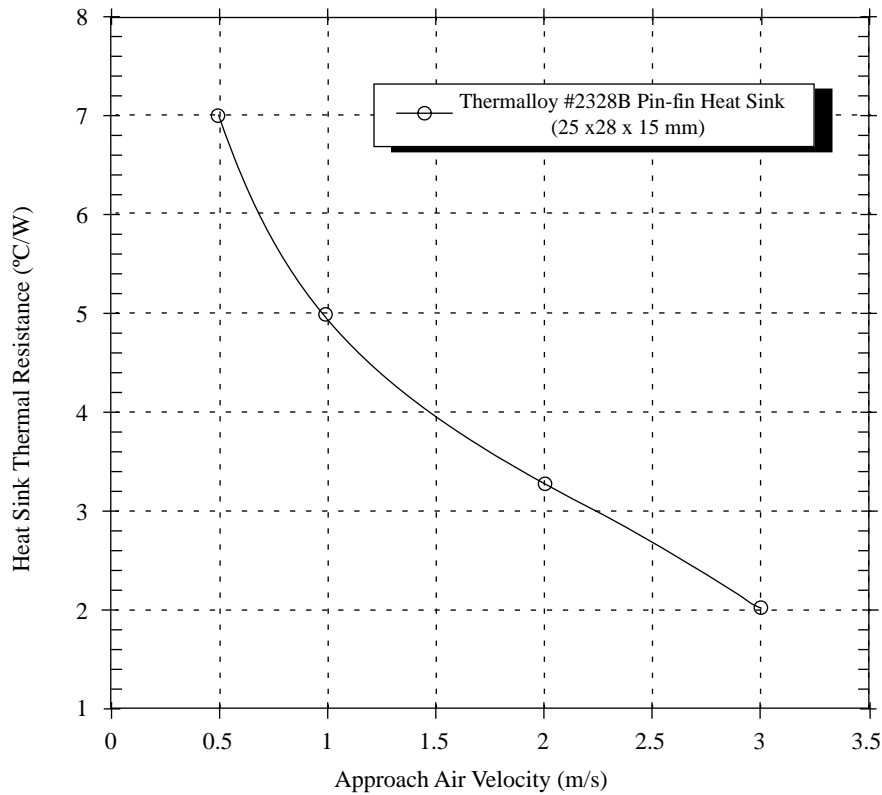
**Figure 26. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity**

Assuming an air velocity of 0.5 m/s, we have an effective $R_{sa}$ of 7 °C/W, thus

$$T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + 7\ °C/W) * 5.0\ W,$$

resulting in a die-junction temperature of approximately 75 °C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

# 1.9  Document Revision History

Table 18 provides a revision history for this hardware specification.

**Table 18. Document Revision History**

| Document Revision | Substantive Change(s) |
|---|---|
| Rev 0 | Initial release |
| Rev 1 | Added 2.5 V support for Processor Bus<br><br>Raised Min Core Frequency and lowered Max Sysclk Frequency in Table 8.<br><br>Reduced L2 Output Hold Time for L2CR[14-15] = 00 from 0.6ns to 0.4ns in Table 11.<br><br>Reduced 400 MHz SYSCLK from 133 MHz to 100MHz in Table 8. |
| Rev 1.1 | Table 3 adds notes on extended temperature parts.<br><br>Figure 27 adds Application Modifier for extended temperature.<br><br>Figure 17 adds capacitor pad dimensions.<br><br>Fixed Table 13 to reflect 2.5 V Processor Bus support added in previous rev of document. |

# 1.10  Ordering Information

Figure 27 provides the Motorola part numbering nomenclature for the MPC7400. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancement(s) in the part from the original production design. The bus divider may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

MPC 7400 RX XXX X X

Product Code

Part Identifier

Revision Level
(Contact Local Motorola Sales Office)

Application Modifier
(L = Full Spec, 1.8V±100mV, 0-105°C $T_j$)
(T = Ext. Temp Spec, 1.8V±100mV, -40-105°C $T_j$)

Processor Frequency

Package
(RX = BGA)
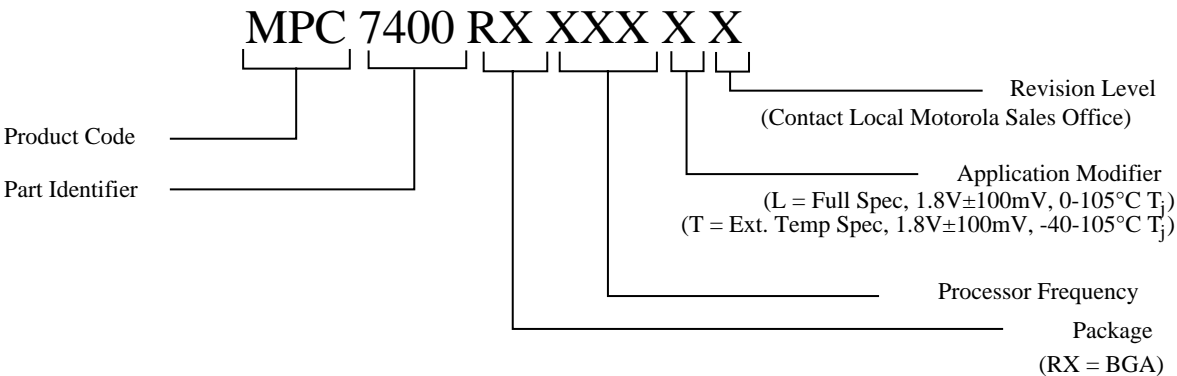
**Figure 27. Motorola Part Number Key**

**MOTOROLA**