17 August 2004

MPC8560ADS Rev.A

Quick Reference Guide

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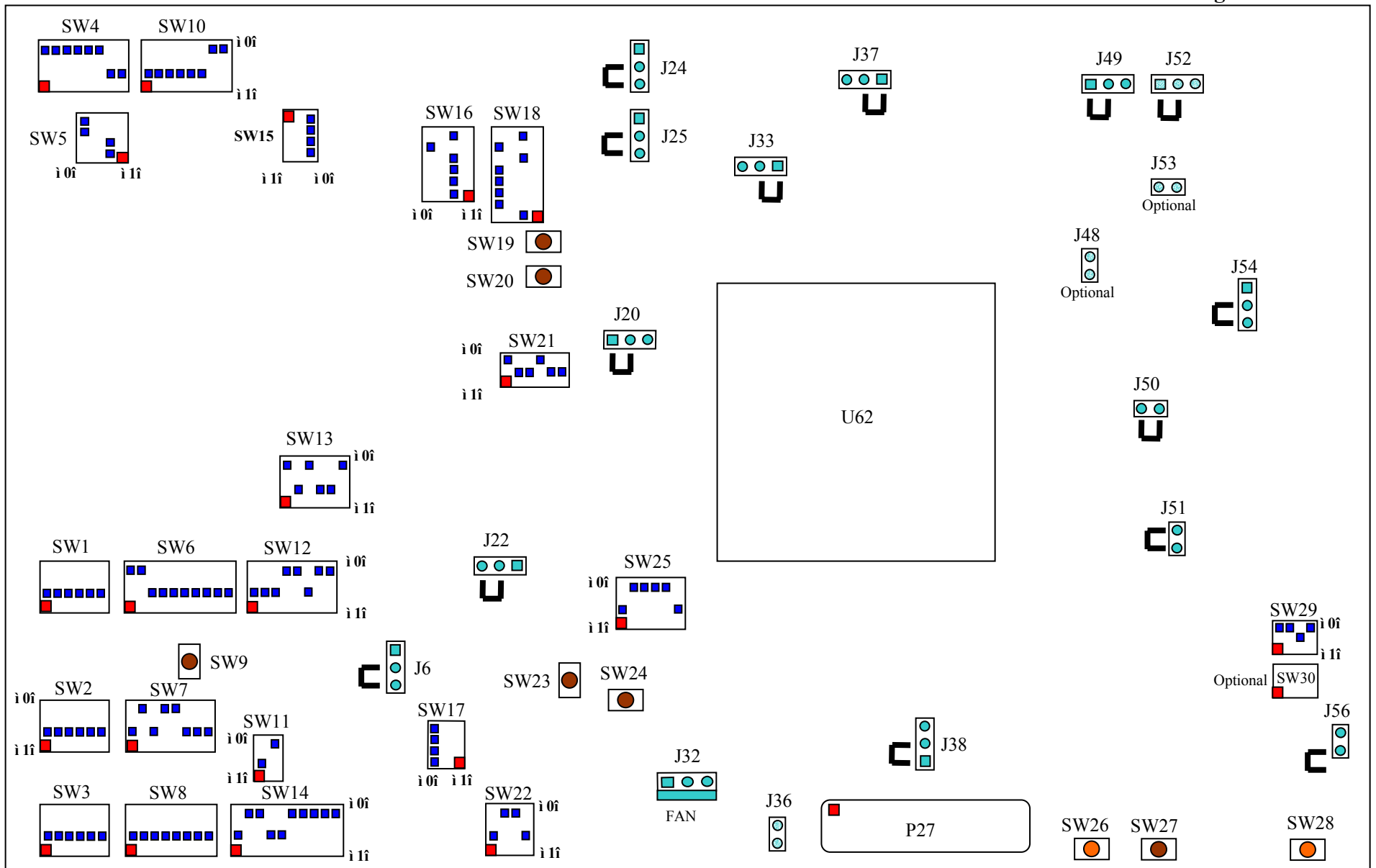Switches and jumpers arrangement on the MPC8560ADS Rev.A represented in the Figure 1.

1. Switchís SETUP

Default status of the board switches represented in the Table 1.

Figure 1

SW4 SW10

ì 0î

ì 1î

SW5

SW15

ì 0î ì 1î

ì 1î ì 0î

SW16 SW18

ì 0î ì 1î

J24

J25

J37

J33

J49 J52

J53
Optional

J48
Optional

J54

SW19

SW20

SW21

ì 0î

ì 1î

J20

U62

J50

SW13

ì 0î

ì 1î

SW1 SW6 SW12

ì 0î

ì 1î

J22

SW25

ì 0î

ì 1î

J51

SW9

SW2 SW7

ì 0î

ì 1î

J6

SW23 SW24

SW29
ì 0î

ì 1î

Optional SW30

SW11

ì 0î

ì 1î

SW17

ì 0î ì 1î

J56

SW3 SW8 SW14

ì 0î

ì 1î

SW22

ì 0î

ì 1î

J32

FAN

J36

J38

P27

SW26 SW27

SW28

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Table 1

#	Ref.	Block Name	Name	Pos.	Note	
1	**SW1**					
	1	**PCI**	I/O IMPED	1	42Ohm PCI impedance; (0=20Ohm PCI impedance)	
	2		ARBITER	1	On-Chip PCI/PCIX Arbiter (0= External Arbiter is required)	
	3		DEBUG	1	Normal mode (0=Debug EN)	***1**
	4		CONFIG	1	PCI mode (0=PCIX mode)	
	5		WIGTH	1	32bit interface (0=64bit interface)	
	6		SPARE	1	Not used **(CORE PLL1 for PQ37L)**	
2	**SW2**					
	1	**PCI & LB**	PCI HOLD_EN 0	1	**LB_HOLD EN0 for PQ37L**	***2**
	2		PCI HOLD_EN 1	1	**LB_HOLD EN1 for PQ37L**	
	3		HOST/AGT 0	1	RIO & PCI Host	***3**
	4		HOST/AGT 1	1	**CORE PLL2 for PQ37L**	
	5		LB_HOLD EN 0	1	1ns hold time	***4**
	6		LB_HOLD EN 1	1		
3	**SW3**					
	1	**ROM & BOOT**	ROM LOC.0	1	FLASH (Local Bus GPCM-32bit)	***5**
	2		ROM LOC.1	1		
	3		ROM LOC.2	1		
	4		CPU_BOOT	1	e500 allowed to boot without waiting	***6**
	5		BOOTSEQ 0	1	Boot sequencer is disabled.	***7**
	6		BOOTSEQ 1	1	I^{2}C ROM not asserted	
4	**SW4**					
	1	**ATM**	ATM2_16	0	FCC1 ATM16 Disabled (1=Enable)	
	2		ATM2_8	0	FCC1 ATM8 Disabled (1=Enable)	
	3		ATM1	0	FCC2 ATM Disabled (1=Enable)	
	4		UTP1_UTP2	0	FCC1 Single PHY (1=Multi-PHY)	
	5		FE2	0	FCC2 FETH2 Disabled (1=Enable)	
	6		FE3	0	FCC3 FETH3 Disabled (1=Enable)	
	7		RS232_2	1	RS232_2 Enabled (0=Disable)	
	8		RS232_1	1	RS232_1 Enabled (0=Disable)	
5	**SW5**					
	1	**CPM CNTR3**	MANUAL	1	Manual (0=Default)	
	2		USB	1	Disabled (0=Enabled)	
	3		RSRV.	0	Not used	
	4		RSRV.	0		
6	**SW6**					
	1	**TSEC & GLOBAL**	TSEC1_CFG	0	GMII/RGMII (1=TBI/RTBI)	***8**
	2		TSEC2_CFG	0	GMII/RGMII (1=TBI/RTBI)	***9**
	3		TSEC_WIGTH	1	ETH 8bit TBI/GMII (0=4bit RTBI/RGMII)	***10**
	4		CPM TEST	1	Connected to TSEC1_TxD[3]	Chip test only
	5		CFG. 60X	1	Connected to TSEC1_TxD[2]	
	6		GL. SFTO	1	Connected to TSEC1_TxD[1]	
	7		GL. WAITR	1	Connected to TSEC1_TxD[0]	
	8		POR ABIST	1	Connected to TRIG_OUT	***11**
	9		MEM. DEBUG	1	DDR debug info on MSRCID & MDVAL	***12**
	10		DDR. DEBUG	1	DDR ECC normal mode	***13**

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Continue Table 1

#	Ref.	Block Name	Name	Pos.	Note		
7	**SW7**						
	1		SYS PLL O	1	10:1 CCB/SYSCLK		***14**
	2		SYS PLL 1	0			
	3		SYS PLL 2	1			
	4	**PLL & RIO**	SYS PLL 3	0			
	5		CORE PLL 0	0	5:2 e500/CCB		***15**
	6		CORE PLL 1	1			
	7		RIO CLK 0	1	CCB = TX Clock	**ROM LOC0 for PQ37L**	***16**
	8		RIO CLK 1	1		**ROM LOC1 for PQ37L**	
8	**SW8**						
	1		DEVICE ID 0	1	Default 0xFF		
	2		DEVICE ID 1	1			
	3		DEVICE ID 2	1			
	4	**RIO ID**	DEVICE ID 3	1			
	5		DEVICE ID 4	1			
	6		DEVICE ID 5	1		Device ID used for Rapid IO hosts	
	7		DEVICE ID 6	1			
	8		DEVICE ID 7	1			
9	**SW9**		**RIO_CLK**		Setting RIO-CLK On-Board Synthesizer clock-out		
10	**SW10**						
	1		NU	1	Host (0=Slave)	**USB for PQ37L**	
	2		SELRSTXD1	1	RS232_1-TXD =PD30 (0=PB28)		
	3		SELRSCTS1	1	RS232_1-CTS =PC15 (0=PC29)		
	4		SELRSTXD2	1	RS232_2-TXD =PD27 (0=PB12)		
	5	**CPM**	SELRSCTS2	1	RS232_2-CTS =PC13 (0=PC28)		
	6		SELRSRXD2	1	RS232_2-RXD =PD28 (0=PB15)		
	7		PC21_CKEN	0	EXP_PC21= Exp. Clock Source Driver Disabled (1=En.)		
	8		PC20_EXP	0	EXP_PC20= Exp. Clock Source Driver and PC20 signal in/out Disabled (1=En.)		
11	**SW11**						
	1	**RIO_CLK**	SEL	1	16MHz On-Board XTAL ref input (0=EXT REF CLK)		
	2		PWD	0	Out Divider ˜ 1; (1= Out Divider ˜ 16)		
12	**SW12**						
	1		LSSD	1	Default	Chip test only	
	2		PERSONALITY	1	Dracom (0=Draco)		
	3		POR LBIST	1	Connected to ASLEEP	Chip test only	
	4	**MODE**	RSRV.	0	Not used		
	5		RSRV	0			
	6		HRST REQ.	1	Disable (0=Enable)		
	7		DRACOM REV.	0	PQ3_Rev2 (1=PQ3_Rev1)		
	8		CONFIG	0	Manual configuration value (1= Default configuration)		

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Continue Table 1

#	Ref.	Block Name	Name	Pos.	Note	
13	**SW13**					
	1		0	0		
	2		1	1		
	3	**DDR GVDD**	2	0	GVDD=2.5V	***17**
	4		3	1		
	5		4	1		
	6		RSRV.	0		
14	**SW14**					
	1		MO	1		
	2		M1	0		
	3		M2	0		
	4		M3	1		
	5	**RIO CLK**	M4	1	VCO=800MHz, Fout=200MHz	***18**
	6		M5	0		
	7		M6	0		
	8		N0	0		
	9		N1	0		
	10		EN	0	Disabled (1=Enable)	
15	**SW15**					
	1		NO	0	Slot #0 (Slot select)	***19**
	2	**PCI-JTAG**	N1	0		
	3		EN	0	PCI Slots aux JTAG disabled (1=Enable)	
	4		RSRV.	0	Not used	
16	**SW16**					
	1		N0	1	N=1	***18**
	2		N1	1		
	3	**CLOCK2**	SYNT_EN	1	Enable (0=Stopped Log.î0î)	
	4		CLK_STOP	1	Clock Buffer	Buffer Out Active (0=Stopped Log.î0î)
	5		CLK_SEL	0		PECL input selected (1=Ext Clock source)
	6		CLK_EN	1		Buffer Out Enable (0=3-State)
17	**SW17**					
	1		WRITE_PRT	0	Write/Read Enable (1=Disable)	
	2	**I²C_EEPROM**	A0	0	I²C bus address ì0î	
	3		A1	0		
	4		A2	0		
18	**SW18**					
	1		MO	1		
	2		M1	0		
	3		M2	0		
	4	**CLOCK1**	M3	0	VCO=1056MHz; (M=33) **Fout=16*33/16=33MHz**	***18**
	5		M4	0		
	6		M5	1		
	7		M6	0		
	8		PWD.	1	Output Power Down Divider = :16 (0=:1)	

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Continue Table 1

#	Ref.	Block Name	Name	Pos	Note	
19	**SW19**	**CLOCK**	**SET**		Manual Sys Clock setting	
20	**SW20**		**MODE**		Sys Clock Control select (Manual/Remote)	
21	**SW21**					
	1	**HOST_CLK**	FRANGE 0	0	Fref=50-100MHz	Optional PCI Buffer for PQ3L device
	2		FRANGE 1	1		
	3		STOP	1	Out stopped at Log.ì0î (0= Enable)	
	4		BSEL	0	Fref=50-100MHz (1=25-50MHz)	
	5		OE	1	Out. Disabled 3-State (0= Active)	
	6		PLL_EN	1	Device Reset (0=PLL Enable)	
22	**SW22**	**HOST_MODE**				
	1		0	1	JTAG ñ SERIAL mode selected when connected to PP PC	***20**
	2		1	0		
	3		2	0		
	4		BOOTWIZ	1	Disabled (ì 0î -Enabled) ñ Optional components	
23	**SW23**	**DDR**	**MODE**		GVDD Control select (Manual/Default)	
24	**SW24**	**CORE**	**MODE**		VDD, AVDD Control select	
25	**SW25**					
	1	**VDD/AVDD**	0	1	VDD, AVDD=1.2V	***21**
	2		1	0		
	3		2	0		
	4		3	0		
	5		4	0		
	6		RSRV.	1	Not used	
26	**SW26**		**HRST**		System HARD RESET	
27	**SW27**		**SRST**		System SOFT RESET	
28	**SW28**		**PWR_ON/OFF**		ADS Power ON/OFF	
29	**SW29**	**DIMM0_ADR**				
	1		SA2	0	DIMM0 SPD EEPROM I^{2}C bus address ì 1î	
	2		SA1	0		
	3		SA0	1		
	4		RSRV.	0	Not used	
30	**SW30**	**DIMM1_ADR**				
	1		SA2	0	DIMM1 SPD EEPROM I^{2}C bus address ì 2î	Not assembled
	2		SA1	1		
	3		SA0	0		
	4		RSRV.	0	Not used	

Notes:

*1

PCI Debug configuration	
1	PCI operates in normal mode
0	PCI debug is enabled. Source ID information is driven onto the highest order address bits PCI_AD(63˜ 59) during the bus command phase (PCI) or attribute phase (PCIX)

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*2

PCI Output Hold configuration			
PCI Mode (SW1/4 =1)		**PCIX Mode (SW1/4 =0)**	
11	2 added buffer delays ñ meets 2ns hold time requirement (default)	**11**	0 added buffer delays ñ meets 0.7ns hold time requirement (default)
10	3 added buffer delays (default ˜ 1)	**10**	1 added buffer delays (default ˜ 1)
01	0 added buffer delays (default˜ 2 mod4)	**01**	2 added buffer delays (default˜ 2)
00	1added buffer delays (default˜ 3mod4)	**00**	3 added buffer delays (default ˜ 3)

*3

PCI & RIO Host/Agent configuration	
11	MPC8560 acts as the host processor (default)
10	MPC8560 acts as an agent of a PCI/PCIX host
01	MPC8560 acts as an agent of a RapidIO host
00	MPC8560 acts as an agent of both a PCI/PCIX and a RapidIO device

*4

Local Bus Output Hold configuration	
11	1 added buffer delay (0 added buffer delays for LALE) -default
10	2 added buffer delays (default ˜ 1) (1 added buffer delay for LALE)
01	3 added buffer delays (default ˜ 2) (1 added buffer delay for LALE)
00	Reserved

*5

Boot ROM Location	
000	PCI/PCIX
001	DDR SDRAM
010	Reserved
011	Rapid IO
100	Reserved
101	Local Bus GPCM ñ 8bit ROM
110	Local Bus GPCM ñ 16bit ROM
111	Local Bus GPCM ñ 32bit ROM (default)

*6

CPU Boot configuration	
1	The e500 core is allowed to boot without waiting for configuration by an external master (default)
0	CPU boot hold-off mode. The e500 core is prevented from booting until configured by an external master

*7

	Boot Sequencer configuration
11	Boot sequencer is disabled. No I^{2}C ROM is asserted (default)
10	Extended I^{2}C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I^{2}C interface. A valid ROM must be presented
01	Normal I^{2}C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I^{2}C interface. A valid ROM must be presented
00	Reserved

*8

	TSEC1 Protocol configuration
0	The TSEC1 controller operates using GMII protocol (TSEC Wight =1) or RGMII if configured in reduced mode (TSEC Wight=0) - default
1	The TSEC1 controller operates using TBI protocol (TSEC Wight =1) or RTBI if configured in reduced mode (TSEC Wight=0)

*9

	TSEC2 Protocol configuration
0	The TSEC1 controller operates using GMII protocol (TSEC Wight =1) or RGMII if configured in reduced mode (TSEC Wight=0) - default
1	The TSEC1 controller operates using TBI protocol (TSEC Wight =1) or RTBI if configured in reduced mode (TSEC Wight=0)

*10

	TSEC Wight configuration
1	Ethernet interfaces operate on their standard TBI or GMII modes using 8 transmit data signals and 8 receive data signals (default)
0	Ethernet interfaces operate in reduced mode, either RTBI or RGMII, using only 4 transmit data signals and 4 receive data signals

*11

SW6/8 should be set to "0" when debugging with CodeWarrior + PowerTap pro.

*12

	DDR Debug configuration
1	Debug information is not driven on ECC pins. ECC pins function in their normal mode (default)
0	Debug information is driven on ECC pins instead of normal ECC I/O. ADS disconnect ECC signals from memory (DDR DIMM)

*13

Memory Debug configuration	
1	Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL pins and may be observed at J21 logic analyzer connector (default)
0	Debug information from the Local Bus controller is driven on the MSRCID and MDVAL pins and may be observed at J21 logic analyzer connector

*14

CCB (System) Clock PLL Ratio	
0000	16:1
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1
1010	10:1
1011	Reserved
1100	12:1
1101	Reserved
1110	Reserved
1111	Reserved

*15

e500 Core PLL Ratio	
00	2:1
01	5:2 (2.5)
10	3:1
11	7:2 (3.5)

*16

Rapid IO Transmit Clock Source	
00	Reserved
01	The Rapid IO receive clock is the source of the transmit clock
10	The Rapid IO transmit clock inputs (RIO_TX_CLK_IN and RIO_TX_CLK_IN-) are the source of the transmit clock
11	The CCB clock is the source of the transmit clock (default)

*17

SW13/4	SW13/3	SW13/2	SW13/1	SW13/0	GVDD (Volt)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	1.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	**1**	**0**	**1**	**0**	**2.5 (default)**
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

*18

The following table shows the synthesizerís available output frequencies with usable 16MHz input oscillator. Considering that crystal 16MHz is used the output frequency of the synthesizer can be represented by this formula:

$$\text{Fout (MHz)} = 16*M \div N$$

M	M (6:0)	Internal VCO Freq., MHz	N=1 (PWD=0) N=16(PWD=1)		N=2 (PWD=0) N=32(PWD=1)		N=4 (PWD=0) N=64(PWD=1)		N=8 (PWD=0) N=128(PWD=1)		Note
			N1	N0	N1	N0	N1	N0	N1	N0	
			1	1	0	0	0	1	1	0	
			Fout (MHz)		Fout (MHz)		Fout (MHz)		Fout (MHz)		
25	0011001	800	400		200		100		50		
26	0011010	832	416		208		104		52		
27	0011011	864	432		216		108		54		
28	0011100	896	448		224		112		56		
29	0011101	928	464		232		116		58		
30	0011110	960	480		240		120		60		
31	0011111	992	496		248		124		62		
32	0100000	1024	512		256		128		64		
33	0100001	1056	528		264		132		66		
34	0100010	1088	544		272		136		68		
35	0100011	1120	560		280		140		70		
36	0100100	1152	576		288		144		72		
37	0100101	1184	592		296		148		74		
38	0100110	1216	608		304		152		76		
39	0100111	1248	624		312		156		78		
40	0101000	1280	640		320		160		80		
41	0101001	1312	656		328		164		82		
42	0101010	1344	672		336		168		84		
43	0101011	1376	688		344		172		86		
44	0101100	1408	704		352		176		88		
45	0101101	1440	720		360		180		90		
46	0101110	1472	736		368		184		92		
47	0101111	1504	752		376		188		94		
48	0110000	1536	768		384		192		96		
49	0110001	1568	784		392		196		98		
50	0110010	1600	800		400		200		100		
51	0110011	1632	816		408		204		102		
52	0110100	1664	832		416		208		104		
53	0110101	1696	848		424		212		106		
54	0110110	1728	864		432		216		108		
55	0110111	1760	880		440		220		110		
56	0111000	1792	896		448		224		112		

*19

Optional PCI-JTAG slot signals connection to the P21 header	
00	Slot #0
01	Slot #1
10	Slot #2
11	Slot #3

*20

SW22			MODE	
0	**1**	**2**		
0	0	0	**I^{2}C Boot ROM-PP (Auxiliary mode)** Use to program/verify on-board I^{2}C Boot ROM by Host PC only	Connect P26 to Host-PC PP
1	0	0	**JTAG-SPP (Cost saving mode)** Use to provide JTAG signal emulation by Host PC Standard Parallel Port	
0	1	0	**JTAG-EXT. CONVERTER (Common Mode)** Use to provide JTAG signal emulation by external converter	Connect external JTAG Converter to P28
1	1	0	**JTAGñEPP (Fast download mode)** Use to provide JTAG signal emulation by on-board JTAG-Master controller connected to the Host PC Parallel Port in EPP mode	Connect P26 to Host-PC PP
0	0	1	**SHMOO (Extensive test mode)** Use to provide VDD/Sys CLK remote control through Host PC Parallel Port in EPP mode while CPU JTAG signal emulation by external converter	Connect: P26 to Host-PC PP, external JTAG Converter to P28
0	1	1	Reserved	
1	0	1		
1	1	1		

*21

SW25/4	SW25/3	SW25/2	SW25/1	SW25/0	VDD/AVDD (Volt)
0	0	1	0	0	1.050
1	0	1	0	0	1.075
0	0	0	1	1	1.100
1	0	0	1	1	1.125
0	0	0	1	0	1.150
1	0	0	1	0	1.175
0	**0**	**0**	**0**	**1**	**1.200 (default)**
1	0	0	0	1	1.225
0	0	0	0	0	1.250
1	0	0	0	0	1.275
0	1	1	1	1	1.300
1	1	1	1	1	1.325
0	1	1	1	0	1.350
1	1	1	1	0	1.375
0	1	1	0	1	1.400
1	1	1	0	1	1.425
0	1	1	0	0	1.450
1	1	1	0	0	1.475
0	1	0	1	1	1.500
1	1	0	1	1	1.525
0	1	0	1	0	1.550
1	1	0	1	0	1.575
0	1	0	0	1	1.600
1	1	0	0	1	1.625
0	1	0	0	0	1.650
1	1	0	0	0	1.675
0	0	1	1	1	1.700
1	0	1	1	1	1.725
0	0	1	1	0	1.750
1	0	1	1	0	1.775
0	0	1	0	1	1.800
1	0	1	0	1	1.825

2. Jumperís SETUP

Default status of the board jumpers represented in the Table 2.

<div align="right">Table2</div>

#	Ref.	Name	Pos.	Note
1	J1-J4, J7-J10	PCI Logic Analyzer	-	Provide LA connection
2	J6	FLASH PROG	2-3 closed	Flash programming enable (1-2 disabled)
3	J5, J11-J14, J16	RIO Logic Analyzer	-	Provide LA connection
4	J15, J17-J19, J21, J23, J26, J27, J31	LB Logic Analyzer	-	Provide LA connection
5	J20	VDD	1-2 closed	Core voltage Enable (2-3 disabled)
6	J22	ZBT ZZ	2-3 closed	ZBT SRAM Snooze enabled (1-2 disabled)
7	J24	FETH 2 MII	2-3 closed	Standard Mode (1-2 legacy mode)
8	J25	FETH 3 MII	2-3 closed	Standard Mode (1-2 legacy mode)
9	J28	ECC-Debug Logic Analyzer	-	Provide LA Connection
10	J29, J30, J34, J35, J39, J40, J43, J44	CPM Logic Analyzer	-	Provide LA connection
11	J32	Heat sink FAN	1(-) 2(+)	Provide 12VDC FAN voltage supply
12	J33	FETH2	1-2 closed	MII mode (2-3 RMII mode)
13	J36	ADS-PP	Open	Service ì PC connect recognitionî (Close to provide virtual PC PP recognition)
14	J37	FETH3	1-2 closed	MII mode (2-3 RMII mode)
15	J38	GVDD	1-2 closed	DDR voltage Enable (2-3 disabled)
16	J41, J42, J45, J46	TSEC Logic Analyzer	-	Provide LA connection
17	J47	TSEC2 Configuration	-	Configuration female plug should be inserted
18	J48	2V5 TSEC Current	Open	Not assembled; {I(A)=U(V)/0.1(Ohm)}
19	J49	ATM1 ADD-CNTR	1-2 closed	ON (2-3 Off)
20	J50	TSEC1 G1CRS	Closed	GMII Mode (Open ñ TBI Mode)
21	J51	TSEC2 G1CRS	Closed	GMII Mode (Open ñ TBI Mode)
22	J52	ATM2 ADD-CNTR	1-2 closed	ON (2-3 Off)
23	J53	1V5 TSEC Current	Open	Not assembled; {I(A)=U(V)/0.1(Ohm)}
24	J54	TSEC VOLT-SEL	2-3 closed	TSEC voltage & LVDD=3.3V (1-2 = 2.5volt)
25	J55	TSEC1 Configuration	-	Configuration female plug should be inserted
26	J56	TEST	Open	PS Normal operation (Close - Test mode)

3. PQ37L (MPC8541/8555) device usage

To utilize PQ37L CPU device in the ADS make sure that the following changes done:

1. Optional components C6, C7, C8, C677, C704, C9, C33, C153, C140, C754, C703, C734, D1, F1, LD7, L1, L17, L55, P5, P7, R5, R6, R97, R10, R7, R8, R11, R26, R27, R28, R29, R50, R49, R135, R165, R259, R265, R267, R268, R272, R376, R378, R381, R394, R426, R429, R431, R439, R495, R496, R509, R511, R527, R528, R529, R530, R543, R544, R556, R558, R578, R579, R591, R593, R595, R605, R615, R616, R618, R619, R583, R155, R162, R571, R718, R719, R725, R726, R786, U2, U4, U5, U19, U31, Y5 were assembled

2. Basic components R26, R27, R28, R29, R30, R136, R167, R260, R264, R266, R269, R271, R375, R377, R379, R380, R427, R428, R430, R438, R592, R594, R606, R607, R617 were removed/not assembled