Hardware Specification

MPC862EC/D
Rev. 1.1, 5/2003

MPC862/857T/857DSL
Hardware Specifications

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This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC862/857T/857DSL family (refer to Table 1-1 for a list of devices). The MPC862P, which contains a PowerPC™ core processor, is the superset device of the MPC862/857T/857DSL family. This document contains the following topics:

Part I Overview

The MPC862/857T/857DSL is a derivative of Motorola's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC862/857T/857DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

Table 1-1 shows the functionality supported by the members of the MPC862/857T/857DSL family.

Table 1-1. MPC862 Family Functionality

Part	Cache		Ethernet		SCC	SMC
	Instruction Cache	Data Cache	10T	10/100		
MPC862P	16 Kbyte	8 Kbyte	Up to 4	1	4	2
MPC862T	4 Kbyte	4 Kbyte	Up to 4	1	4	2
MPC857T	4 Kbyte	4 Kbyte	1	1	1	2
MPC857DSL	4 Kbyte	4 Kbyte	1	1	1 [1]	1 [2]

[1] On the MPC857DSL, the SCC (SCC1) is for ethernet only. Also, the MPC857DSL does not support the Time Slot Assigner (TSA)

[2] On the MPC857DSL, the SMC (SMC1) is for UART only

Part II Features

The following list summarizes the key MPC862/857T/857DSL features:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1-1).
    - 16-Kbyte instruction cache (MPC862P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - 8-Kbyte data cache (MPC862P) is two-way, set-associative with 256 sets; 4-Kbyte data cache (MPC862T, MPC857T, and MPC857DSL) is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip-emulation debug mode

- The MPC862/857T/857DSL provides enhanced ATM functionality over that of the MPC860SAR. The MPC862/857T/857DSL adds major new features available in "enhanced SAR" (ESAR) mode, including the following:
  - Improved operation, administration and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements
  - ATM port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
    - Multi-PHY support on the MPC857T
    - Four PHY support on the MPC857DSL
  - Parameter RAM for both SPI and I^2C can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a "split" bus
  - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{RAS}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to Page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{CAS}$ lines, four $\overline{WE}$ lines, one $\overline{OE}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers

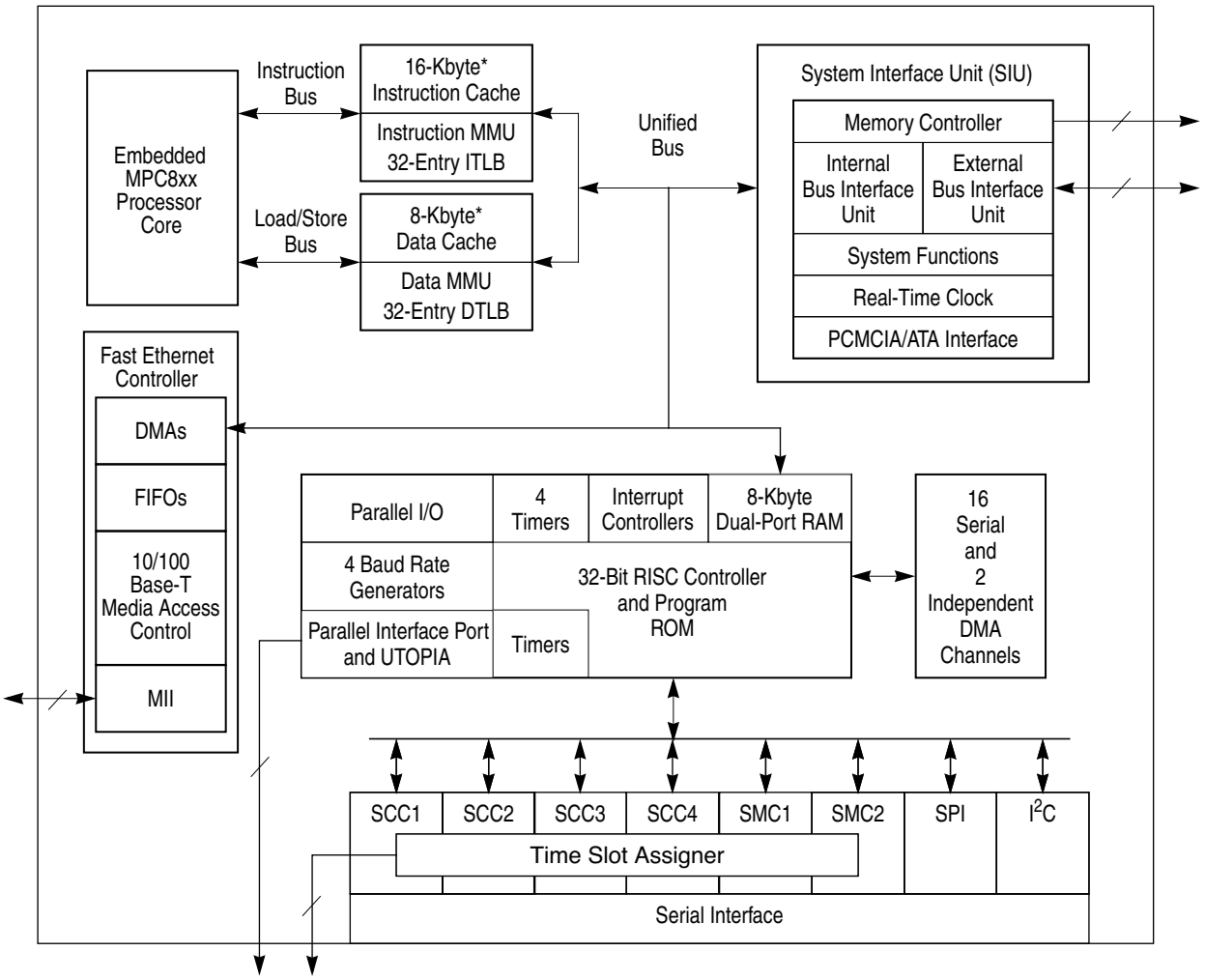
  - Four 16-bit timers cascadable to be two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
  - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus.
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 12 port pins with interrupt capability
  - The MPC862P and MPC862T have 23 internal interrupt sources; the MPC857T and MPC857DSL have 20 internal interrupt sources
  - Programmable priority between SCCs (MPC862P and MPC862T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - The MPC862P and MPC862T have 16 serial DMA (SDMA) channels; the MPC857T and MPC857DSL have 10 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation

  - Autobaud support option
- The MPC862P and MPC862T have four SCCs (serial communication controller) The MPC857T and MPC857DSL have one SCC, SCC1; the MPC857DSL supports ethernet only
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Two SMCs (serial management channels) (The MPC857DSL has one SMC, SMC1 for UART)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit (I^2C) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time-slot assigner (TSA) (The MPC857DSL does not have the TSA)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution

  - Allows independent transmit and receive routing, frame synchronization, clocking
  - Allows dynamic changes
  - On the MPC862P and MPC862T, can be internally connected to six serial channels (four SCCs and two SMCs); on the MPC857T, can be connected to three serial channels (one SCC and two SMCs)
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC862/857T/857DSL or MC68360
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one or two PCMCIA sockets dependant upon whether ESAR functionality is enabled
  - 8 memory or I/O windows supported
- Low power support
  - Full on—All units fully powered
  - Doze—Core functional units disabled except time base decrementer, PLL, memory controller, RTC, and CPM in low-power standby
  - Sleep—All units disabled except RTC, PIT, time base, and decrementer with PLL active for fast wake up
  - Deep sleep—All units disabled including PLL except RTC, PIT, time base, and decrementer.
  - Power down mode— All units powered down except PLL, RTC, PIT, time base and decrementer
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- 3.3 V operation with 5-V TTL compatibility except EXTAL and EXTCLK
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 100MHz

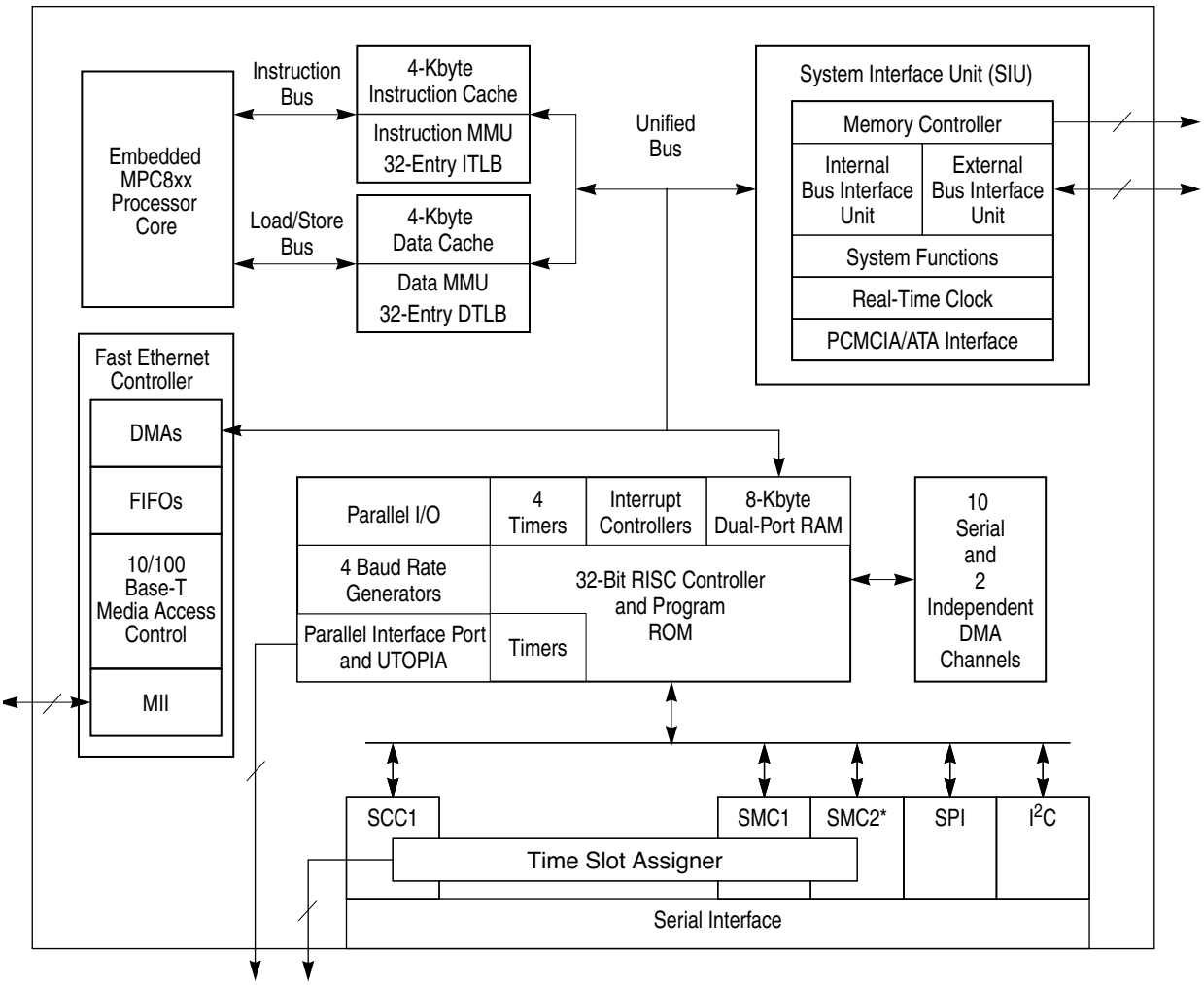
The MPC862/857T/857DSL is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor

module (CPM). The MPC862P/862T block diagram is shown in Figure 2-1. The MPC857T/857DSL block diagram is shown in Figure 2-2.



*The MPC862T contains 4-Kbyte Instruction Cache and 4-Kbyte Data cache.

Figure 2-1. MPC862P/862T Block Diagram



*** The MPC857DSL does not contain SMC2 nor the Time Slot Assigner, and provides eight SDMA controllers.**

Figure 2-2. MPC857T/MPC857DSL Block Diagram

Part III Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC862/857T/857DSL. Table 3-1 provides the maximum ratings.

Table 3-1. Maximum Tolerated Ratings

(GND = 0V)

Rating	Symbol	Value	Unit	Max Freq (MHz)
Supply voltage [1]	VDDH	-0.3 to 4.0	V	-
	VDDL	-0.3 to 4.0	V	-
	KAPWR	-0.3 to 4.0	V	-
	VDDSYN	-0.3 to 4.0	V	-
Input voltage [2]	V_{in}	GND-0.3 to VDDH	V	-
Temperature [3] (standard) [4]	$T_{A(min)}$	0	˚C	100
	$T_{j(max)}$	105	˚C	100
Temperature [3] (extended)	$T_{A(min)}$	-40	˚C	80
	$T_{j(max)}$	115	˚C	80
Storage temperature range	T_{stg}	-55 to +150	˚C	-

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6-1. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC862/857T/857DSL is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

3 Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

4 JTAG is tested only at ambient, not at standard maximum or extended maximum.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Part IV Thermal Characteristics

Table 4-1 shows the thermal characteristics for the MPC862/857T/857DSL.

Table 4-1. MPC862/857T/857DSL Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction to ambient [1]	Natural Convection	Single layer board (1s)	$R_{\theta JA}$ [2]	37	°C/W
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	23	
	Air flow (200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$ [3]	30	
		Four layer board (2s2p)	$R_{\theta JMA}$ [3]	19	
Junction to board [4]			$R_{\theta JB}$	13	
Junction to case [5]			$R_{\theta JC}$	6	
Junction to package top [6]	Natural Convection		Ψ_{JT}	2	
	Air flow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Part V Power Dissipation

Table 5-1 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 5-1. Power Dissipation (P_D)

Die Revision	Frequency	Typical [1]	Maximum [2]	Unit
0 (1:1 Mode)	50 MHz	656	735	mW
	66 MHz	TBD	TBD	mW
A.1, B.0 (1:1 Mode)	50 MHz	630	760	mW
	66 MHz	890	1000	mW
A.1, B.0 (2:1 Mode)	66 MHz	910	1060	mW
	80 MHz	1.06	1.20	W
B.0 (2:1 Mode)	100 MHz	1.35	1.54	W

1 Typical power dissipation is measured at 3.3V.

[2] Maximum power dissipation is measured at 3.5V.

NOTE

Values in Table 5-1 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

Part VI DC Characteristics

Table 6-1 provides the DC electrical characteristics for the MPC862/857T/857DSL.

Table 6-1. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH - 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{in}	—	100	μA
Input Leakage Current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	μA
Input Leakage Current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{In}	—	10	μA
Input Capacitance [1]	C_{in}	—	20	pF
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0V Except XTAL, XFC, and Open drain pins	VOH	2.4	—	V
Output Low Voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA [2] IOL = 5.3 mA [3] IOL = 7.0 mA (TXD1/PA14, TXD2/PA12) IOL = 8.9 mA ($\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)	VOL	—	0.5	V

[1] Input capacitance is periodically sampled.

[2] A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, CTS3/SDACK2/L1TSYNCB/PC7, CD3/L1RSYNCB/PC6, CTS4/SDACK1/L1TSYNCA/PC5, CD4/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/REJECT2, PD6/RTS4, PD7/RTS3, PD4/REJECT3, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, MII_TXD[0:3].

[3] BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30)

Part VII Thermal Calculation and Measurement

For the following discussions, P_D= (VDD x IDD) + PI/O, where PI/O is the power dissipation of the I/O drivers.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature °C

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value which provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity T_J-T_A) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 7-1.

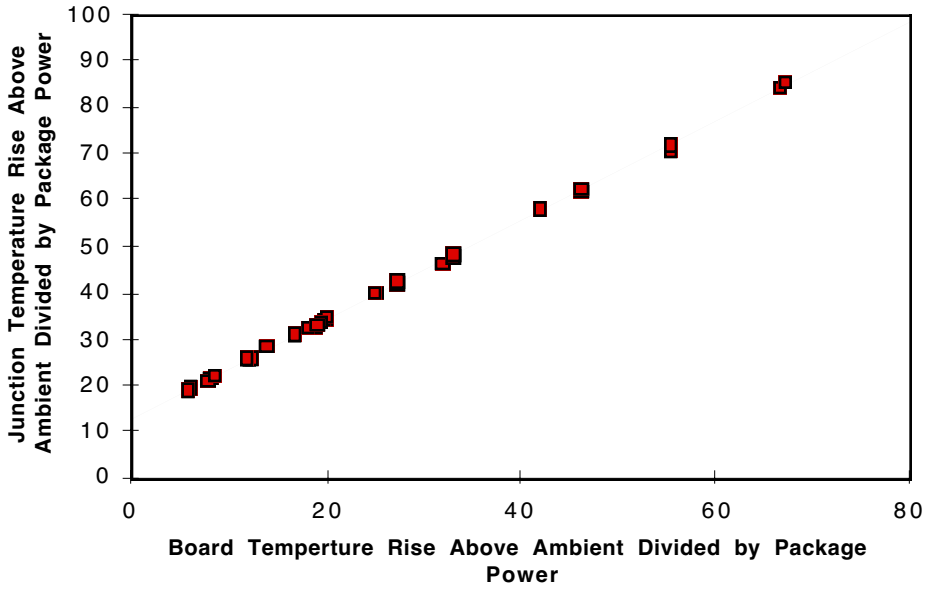


Figure 7-1. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$T_J = T_B + (R_{\theta JB} \times P_D)$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature °C

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International (415) 964-5111
805 East Middlefield Rd
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications 800-854-7179 or
(Available from Global Engineering Documents) 303-397-7956

JEDEC Specifications
http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

Part VIII Layout Practices

Each V_{CC} pin on the MPC862/857T/857DSL should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC862/857T/857DSL have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Part IX Bus Signal Timing

The maximum bus speed supported by the MPC862/857T/857DSL is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC862/857T/857DSL used at 80MHz must be configured for a 40 MHz bus). Table 9-1 shows the period ranges for standard part frequencies.

Table 9-1. Period Range for Standard Part Frequencies

Freq	50MHz		66MHz		80MHz		100MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Period	20.00	30.30	15.15	30.30	25.00	30.30	20.00	30.30

Table 9-2 provides the bus operation timing for the MPC862/857T/857DSL at 33 MHz, 40 Mhz, 50 MHz and 66 Mhz.

The timing for the MPC862/857T/857DSL bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays.

Table 9-2. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	CLKOUT period	30.30	30.30	25.00	30.30	20.00	30.30	15.15	30.30	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	-0.90	0.90	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	-2.30	2.30	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [1]	-0.60	0.60	-0.60	0.60	-0.60	0.60	-0.60	0.60	ns
B1d	CLKOUT phase jitter[1]	-2.00	2.00	-2.00	2.00	-2.00	2.00	-2.00	2.00	ns
B1e	CLKOUT frequency jitter (MF < 10) [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1f	CLKOUT frequency jitter (10 < MF < 500) [1]	—	2.00	—	2.00	—	2.00	—	2.00	%
B1g	CLKOUT frequency jitter (MF > 500) [1]	—	3.00	—	3.00	—	3.00	—	3.00	%
B1h	Frequency jitter on EXTCLK [2]	—	0.50	—	0.50	—	0.50	—	0.50	%
B2	CLKOUT pulse width low (MIN = .040 x B1)	12.10	—	10.00	—	8.00	—	6.10	—	ns
B3	CLKOUT width high (MIN = .040 x B1)	12.10	—	10.00	—	8.00	—	6.10	—	ns
B4	CLKOUT rise time [3] (MAX = 0.00 x B1 + 4.00)	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5[33]	CLKOUT fall time[3] (MAX = 0.00 x B1 + 4.00)	—	4.00	—	4.00	—	4.00	—	4.00	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) invalid (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR invalid (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ invalid [4] (MIN = 0.25 x B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3) $\overline{BDIP}$, PTR valid (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ Valid [4] (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 x B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	11.30	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [5])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 x B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 x B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion(MAX = 0.00 x B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 x B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [6] (4MIN = 0.00 x B1 + .00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 x B1 + 1.00 [7])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [8] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [8] (MIN = 0.00 x B1 + 1.00 [9])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [10](MIN = 0.00 x B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [10] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 - 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM write access [11] (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3) negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 - 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30c	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 - 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid- as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60)	9.40	18.00	7.60	16.00	13.30	14.10	11.30	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid - as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ Valid - as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - As Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 - 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9-2. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B37	UPWAIT valid to CLKOUT falling edge [12] (MIN = 0.00 x B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [12] (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [13] (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.

2 If the rate of change of the frequency of EXTAL is slow (I.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (I.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

3 The timings specified in B4 and B5 are based on full strength clock.

4 The timing for $\overline{BR}$ output is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter.

5 For part speeds above 50MHz, use 9.80ns for B11a.

6 The timing required for $\overline{BR}$ input is relevant when the MPC862/857T/857DSL is selected to work with internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC862/857T/857DSL is selected to work with external bus arbiter.

7 For part speeds above 50MHz, use 2ns for B17.

8 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

9 For part speeds above 50MHz, use 2ns for B19.

10 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

11 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

12 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 9-16.

13 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 9-19.

Figure 9-1 is the control timing diagram.

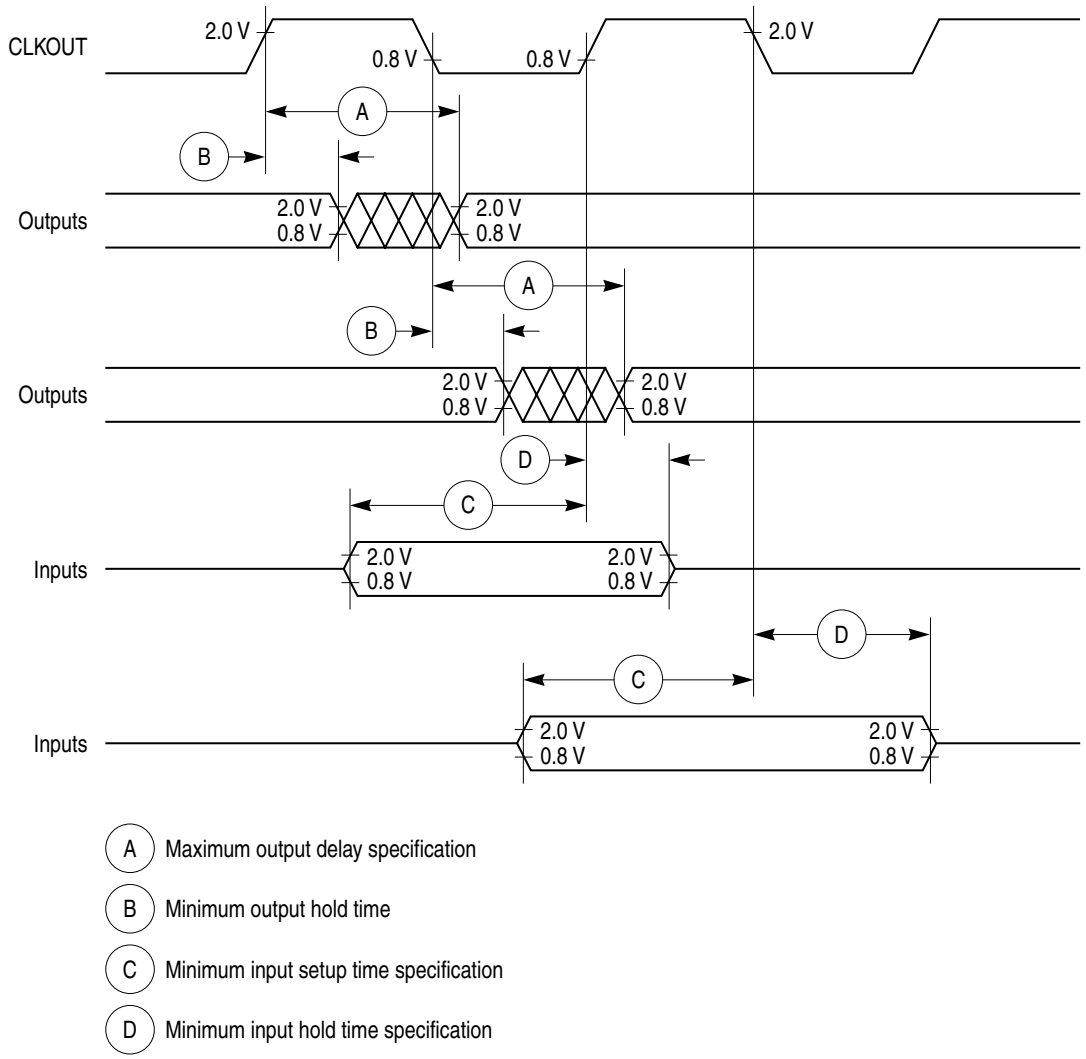


Figure 9-1. Control Timing

Figure 9-2 provides the timing for the external clock.

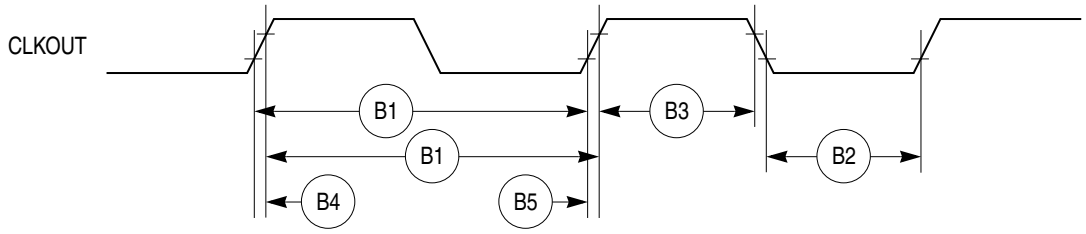


Figure 9-2. External Clock Timing

Figure 9-3 provides the timing for the synchronous output signals.

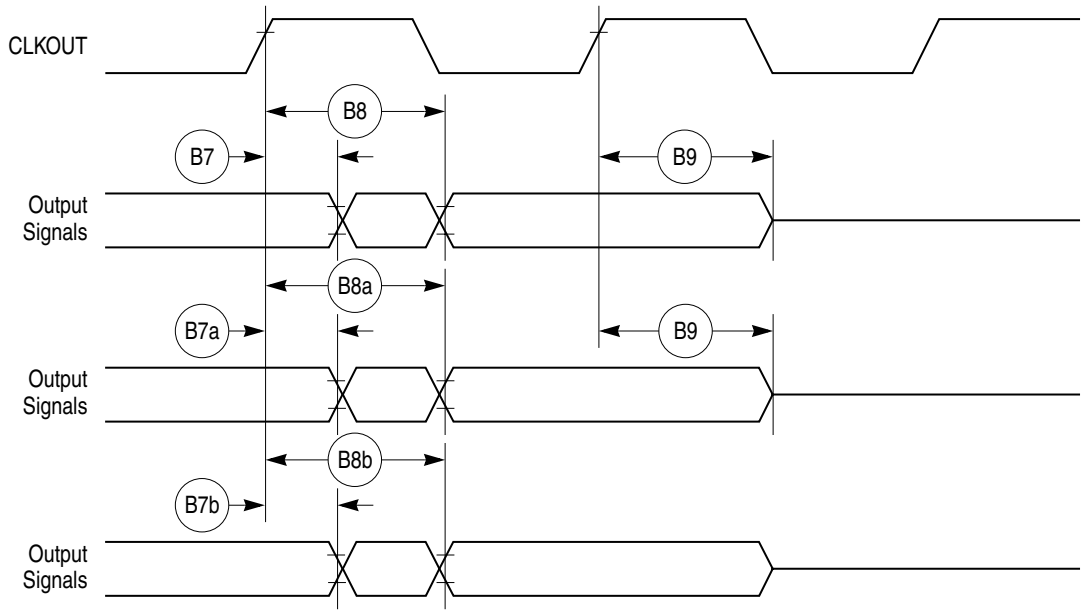


Figure 9-3. Synchronous Output Signals Timing

Figure 9-4 provides the timing for the synchronous active pull-up and open-drain output signals.

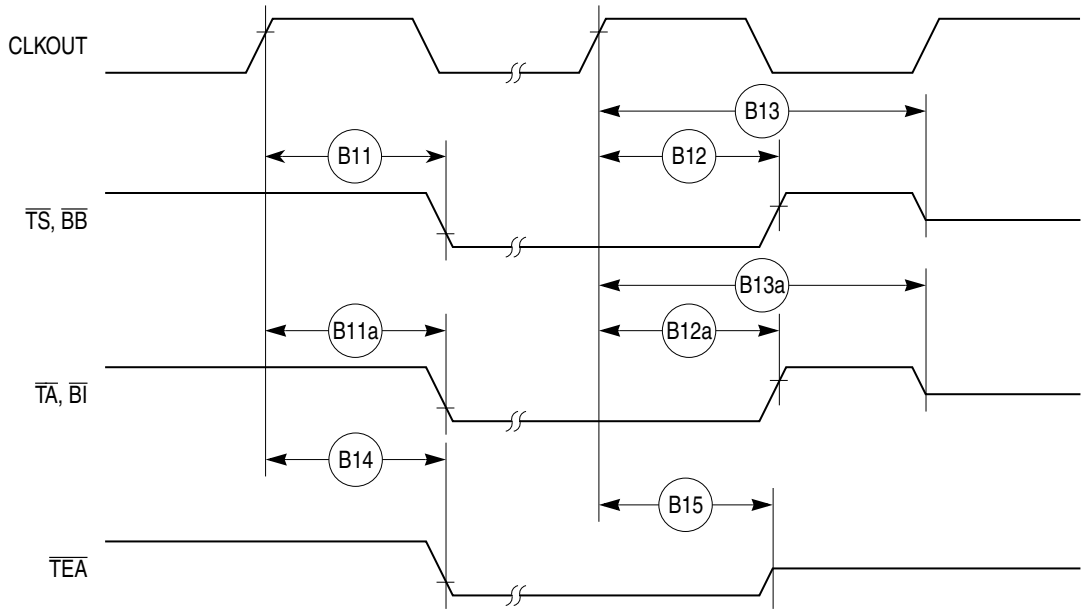


Figure 9-4. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 9-5 provides the timing for the synchronous input signals.

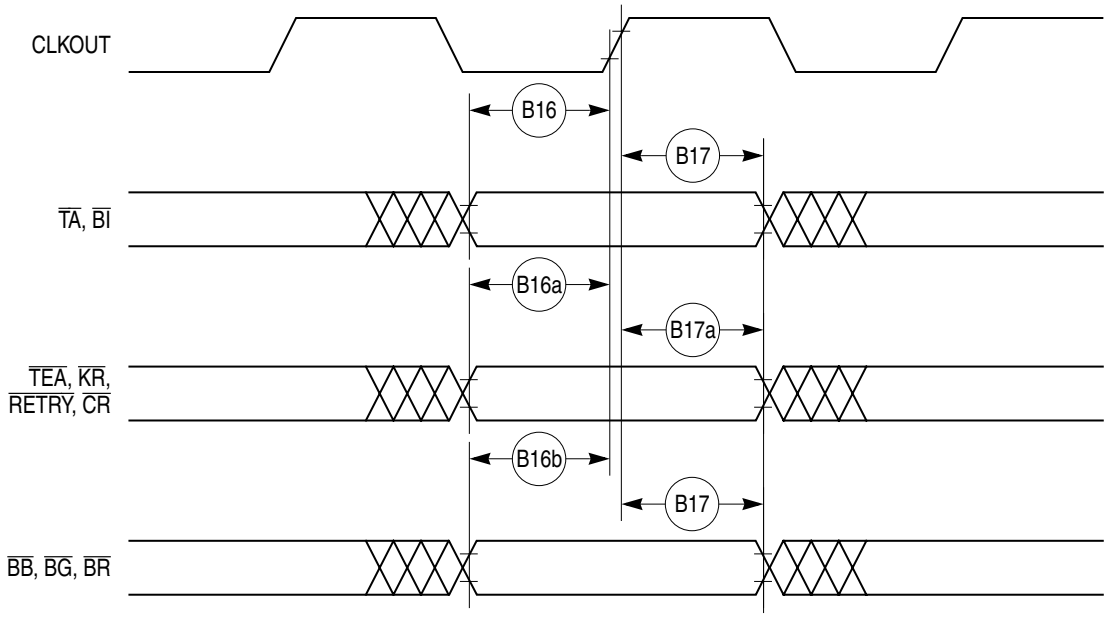


Figure 9-5. Synchronous Input Signals Timing

Figure 9-6 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

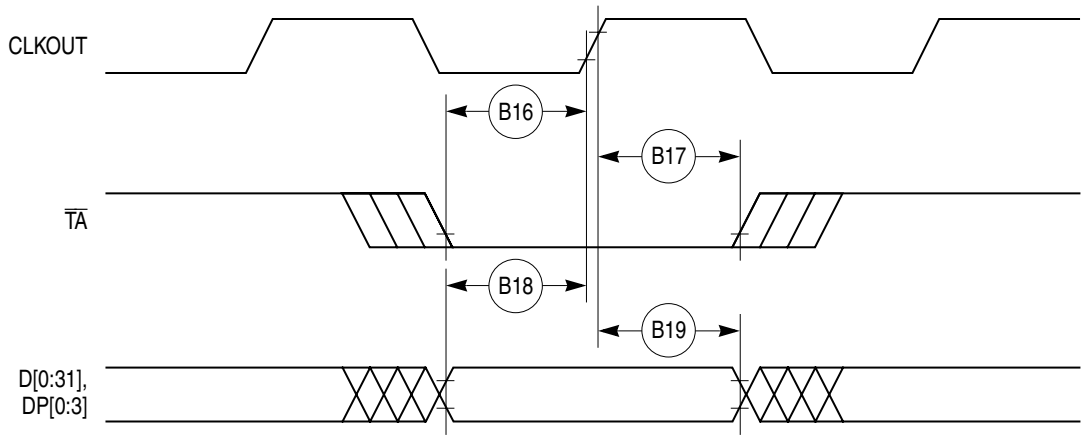


Figure 9-6. Input Data Timing in Normal Case

Figure 9-7 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

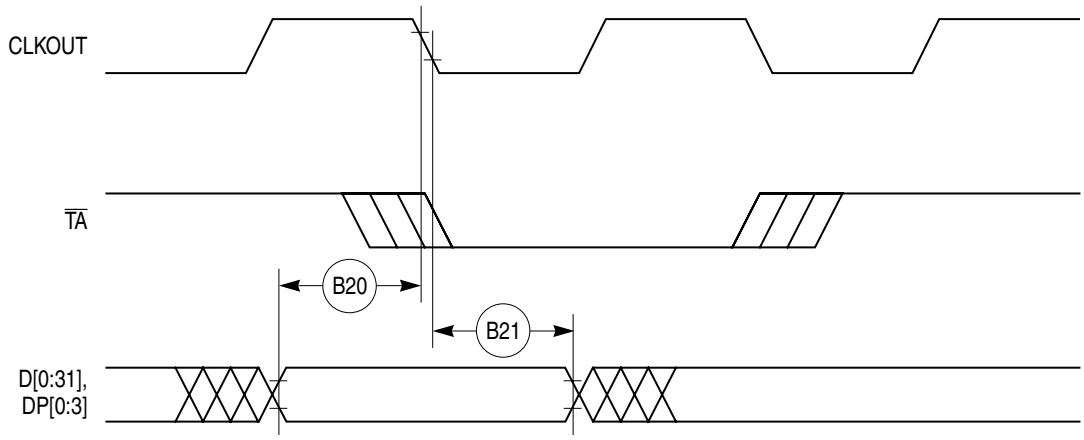


Figure 9-7. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1

Figure 9-8 through Figure 9-11 provide the timing for the external bus read controlled by various GPCM factors.

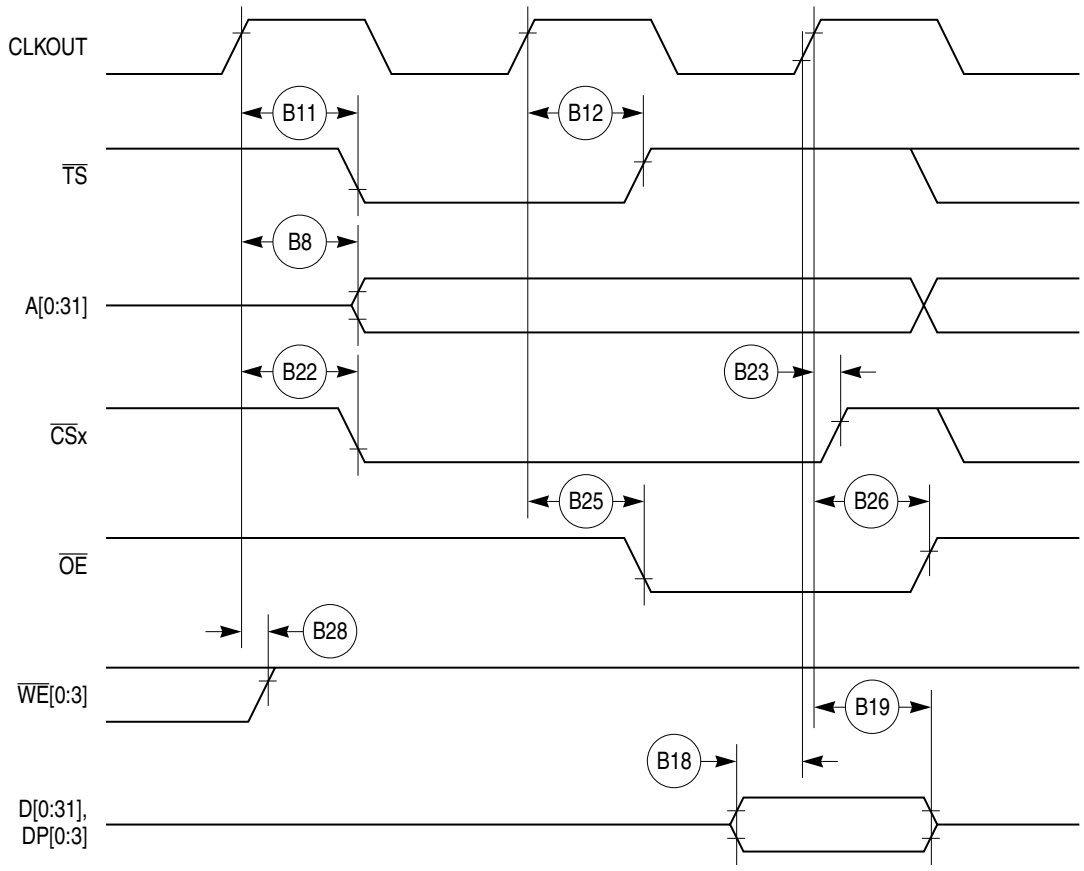


Figure 9-8. External Bus Read Timing (GPCM Controlled—ACS = 00)

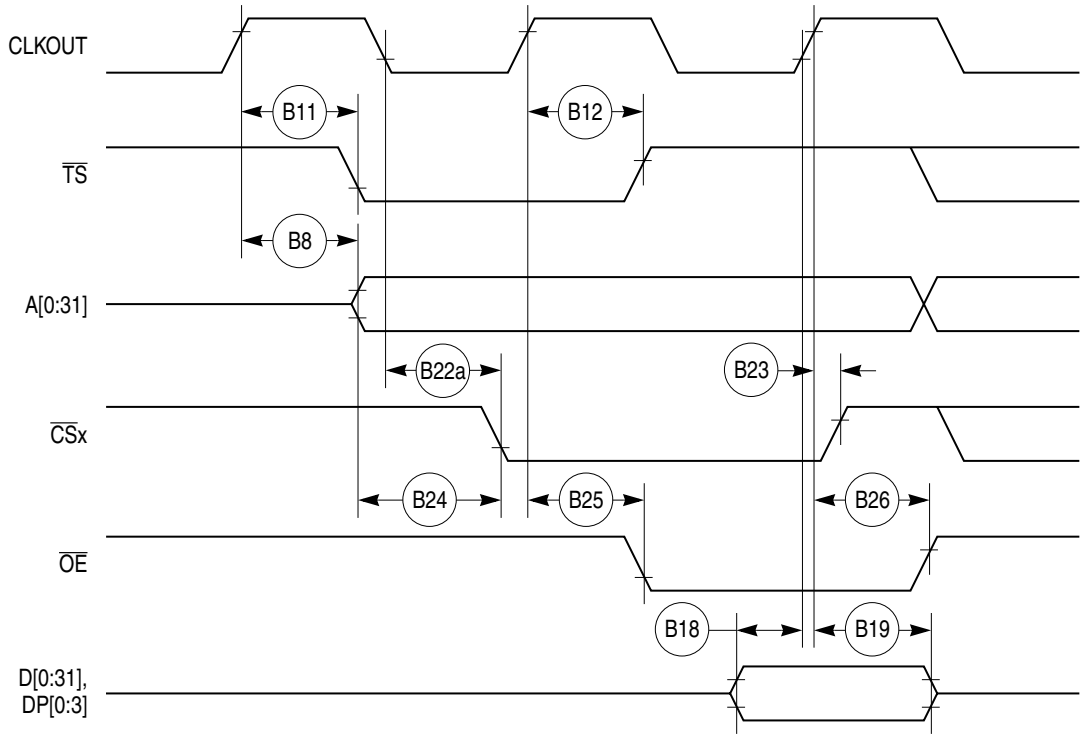


Figure 9-9. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

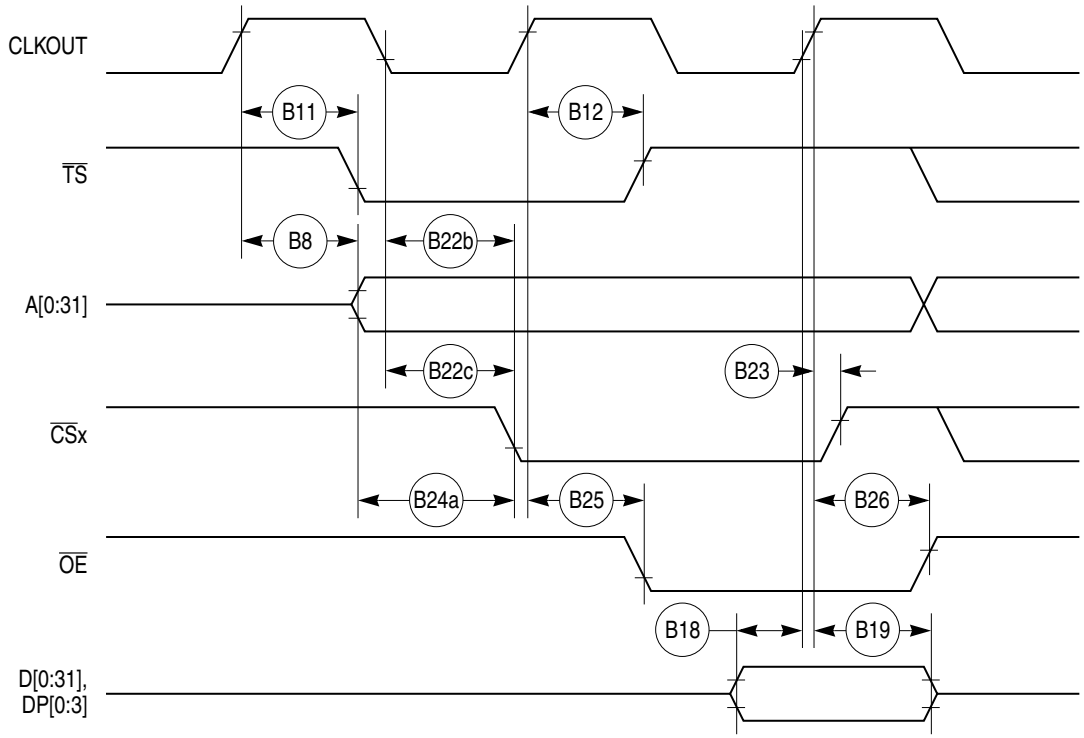


Figure 9-10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

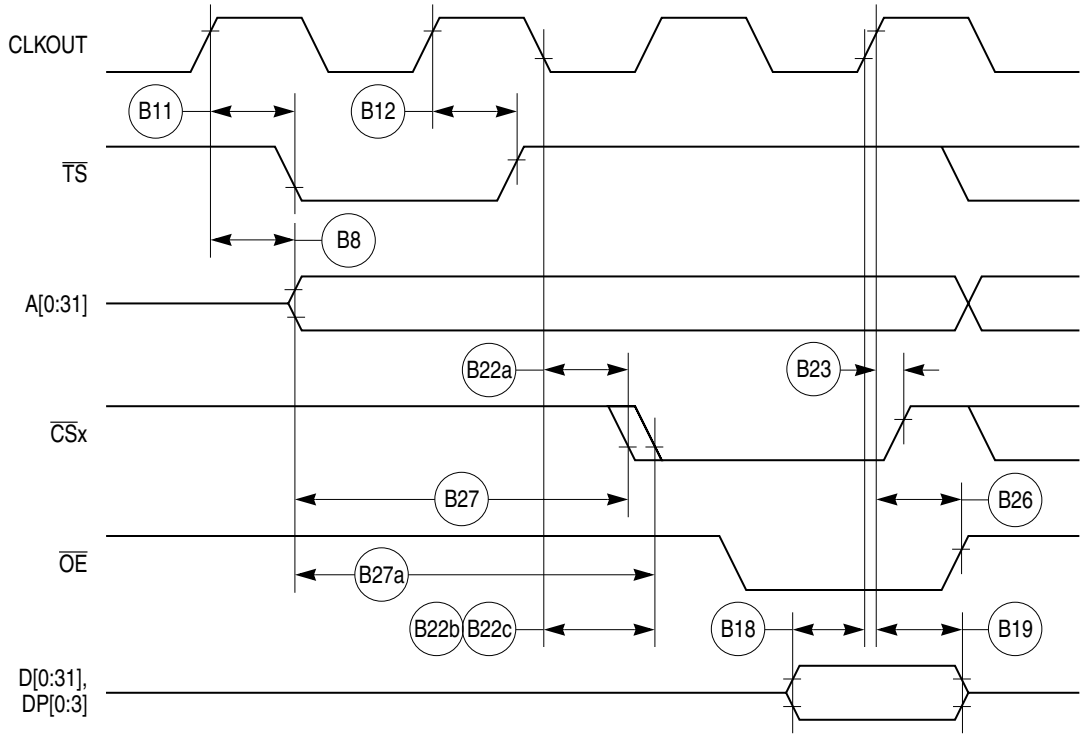


Figure 9-11. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 9-12 through Figure 9-14 provide the timing for the external bus write controlled by various GPCM factors.

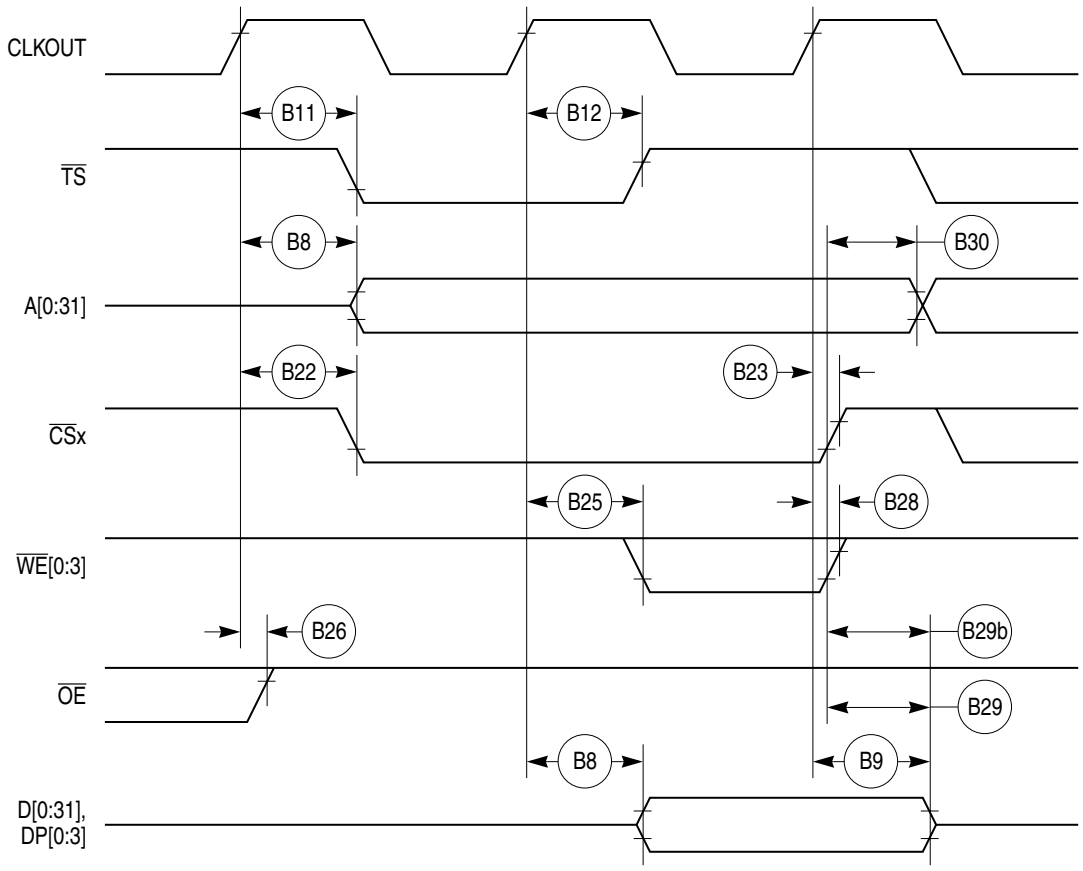


Figure 9-12. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

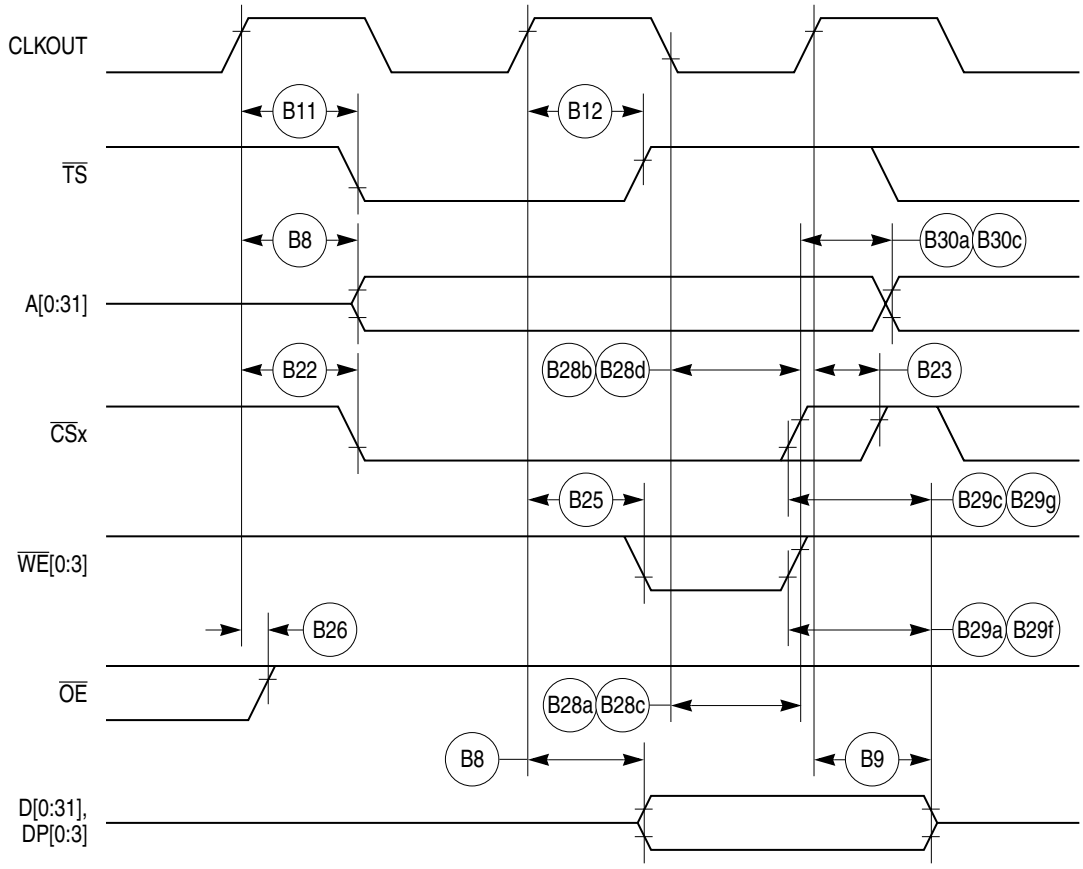


Figure 9-13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

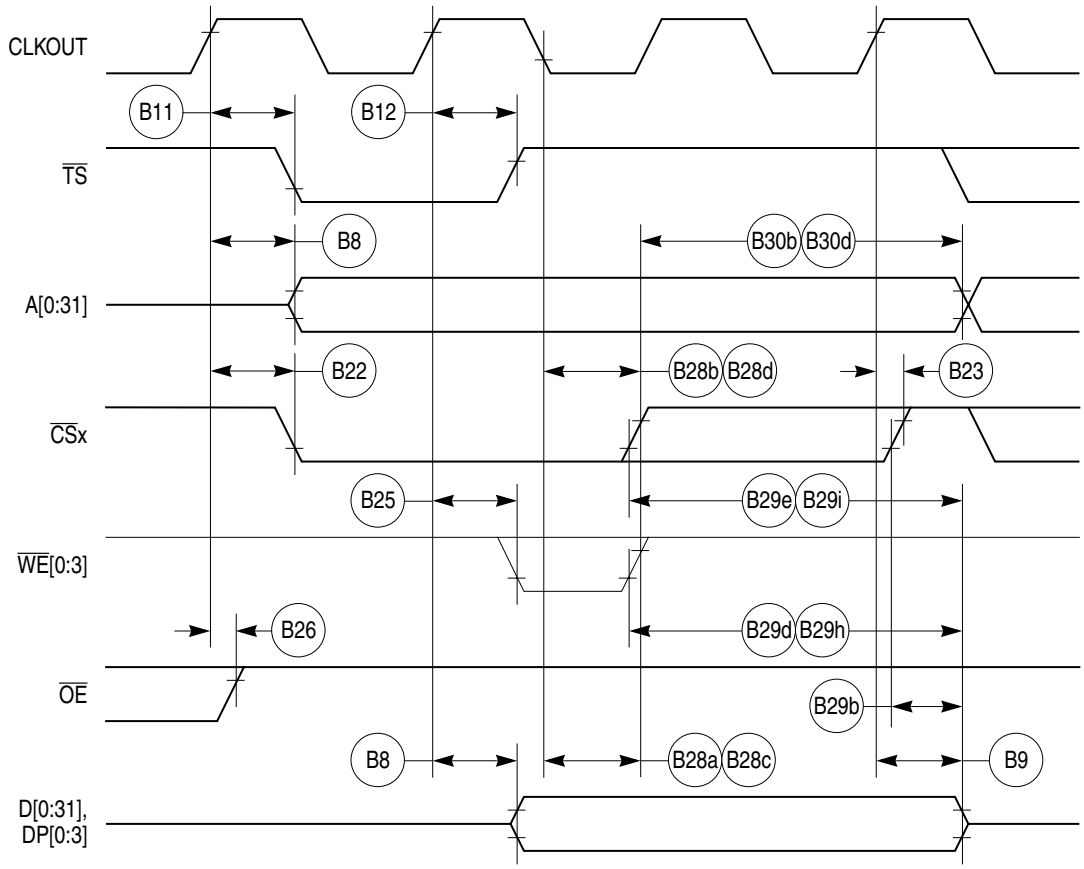


Figure 9-14. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 9-15 provides the timing for the external bus controlled by the UPM.

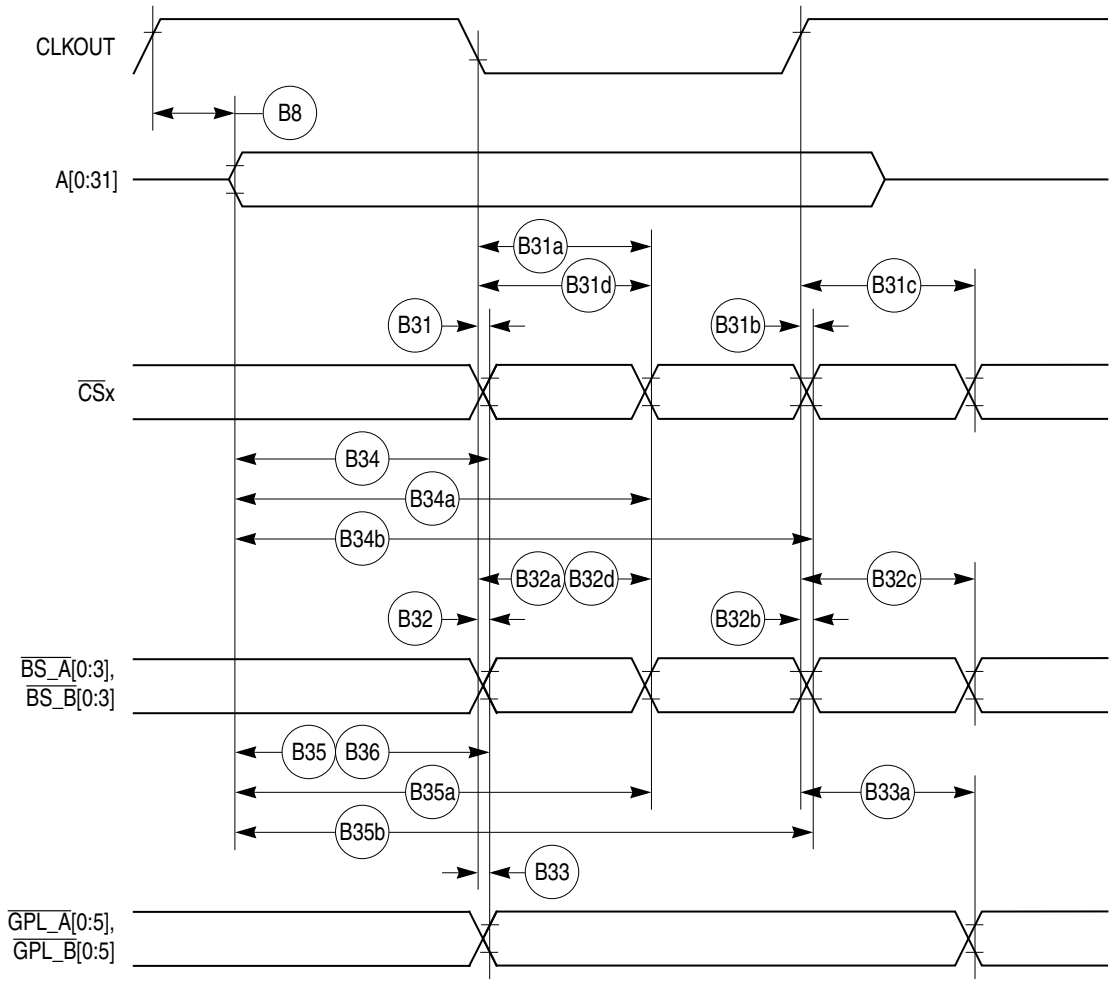


Figure 9-15. External Bus Timing (UPM Controlled Signals)

Figure 9-16 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

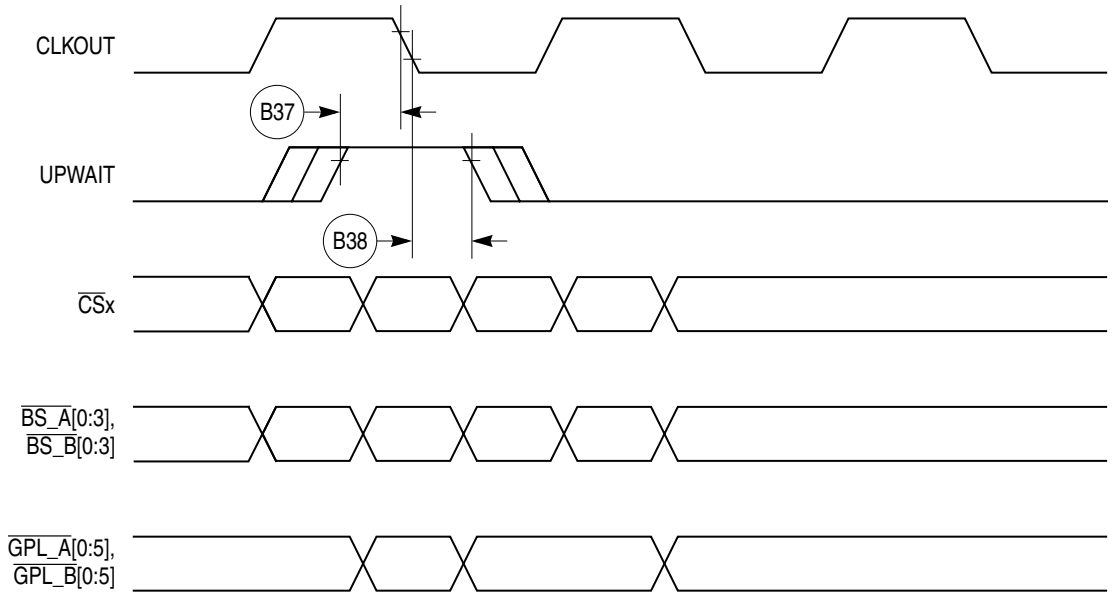


Figure 9-16. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 9-17 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

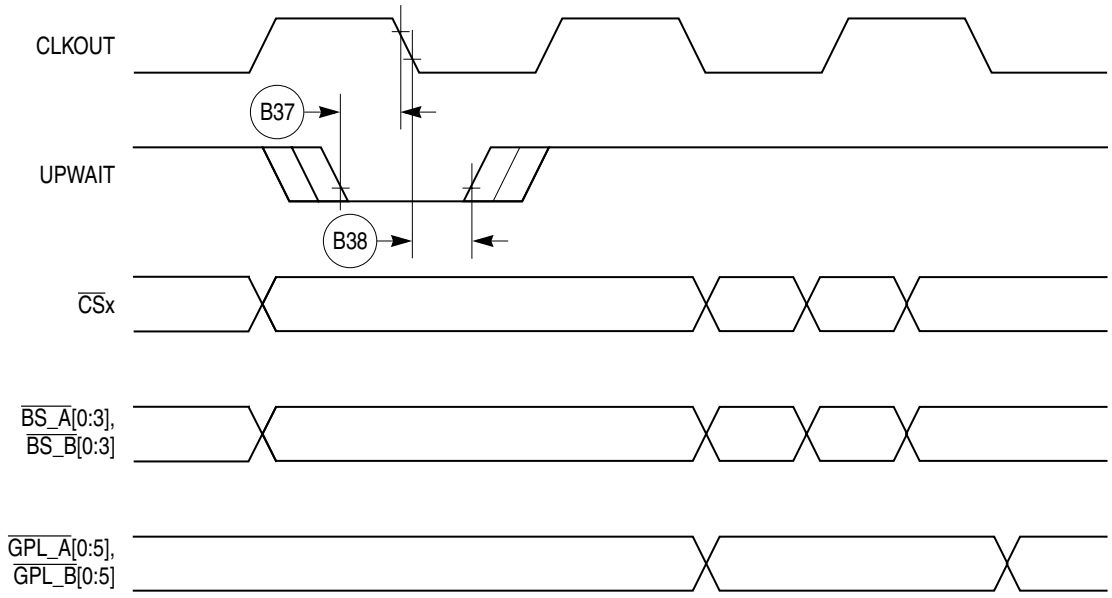


Figure 9-17. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 9-18 provides the timing for the synchronous external master access controlled by the GPCM.

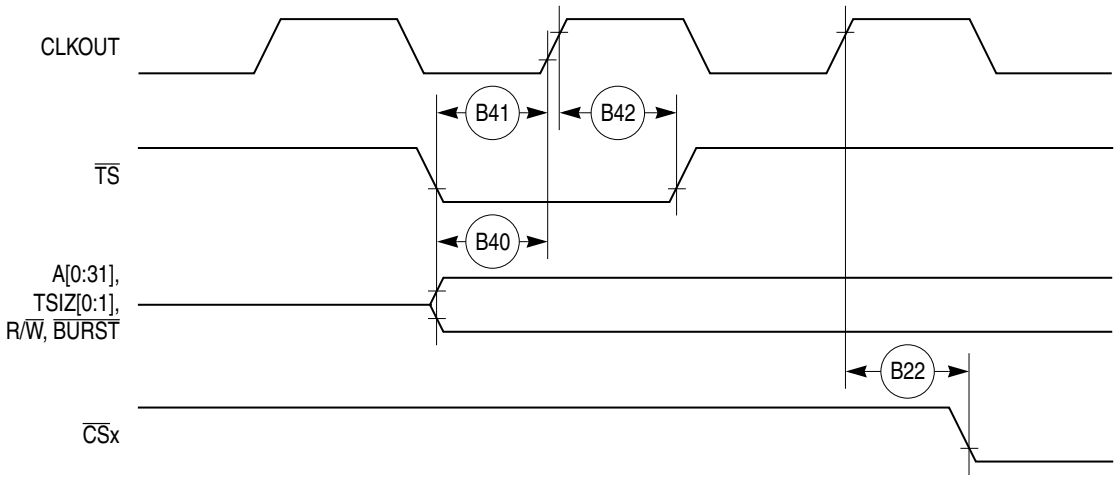


Figure 9-18. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 9-19 provides the timing for the asynchronous external master memory access controlled by the GPCM.

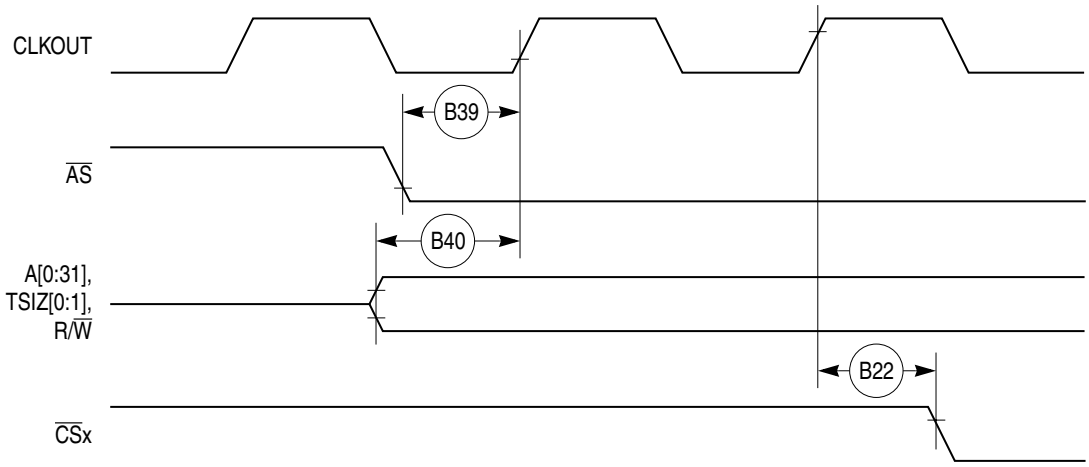


Figure 9-19. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 9-20 provides the timing for the asynchronous external master control signals negation.

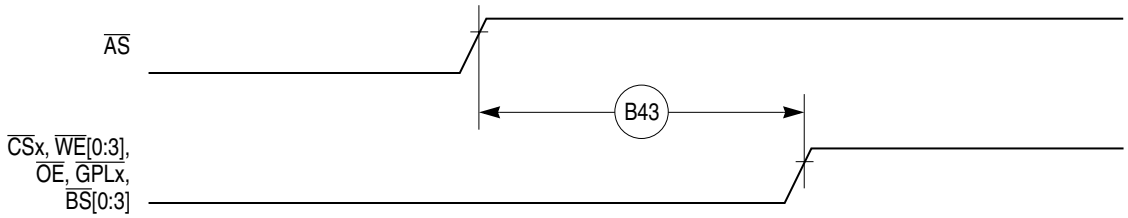


Figure 9-20. Asynchronous External Master—Control Signals Negation Timing

Table 9-3 provides interrupt timing for the MPC862/857T/857DSL.

Table 9-3. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	IRQx valid to CLKOUT rising edge (set up time)	6.00		ns
I40	IRQx hold time after CLKOUT	2.00		ns
I41	IRQx pulse width low	3.00		ns
I42	IRQx pulse width high	3.00		ns
I43	IRQx edge-to-edge time	$4xT_{CLOCKOUT}$		—

[1] The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC862/857T/857DSL is able to support.

Figure 9-21 provides the interrupt detection timing for the external level-sensitive lines.

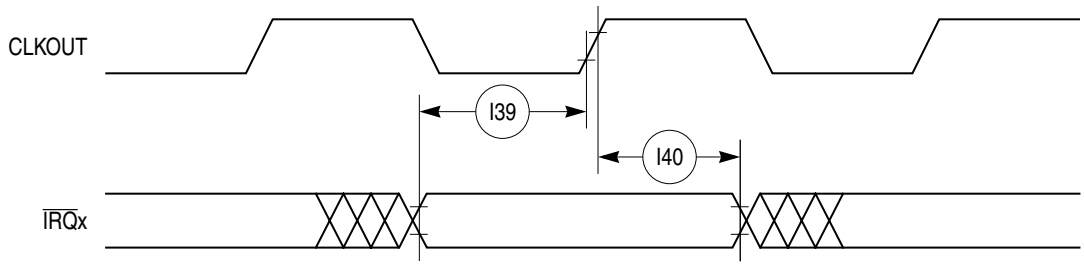


Figure 9-21. Interrupt Detection Timing for External Level Sensitive Lines

Figure 9-22 provides the interrupt detection timing for the external edge-sensitive lines.

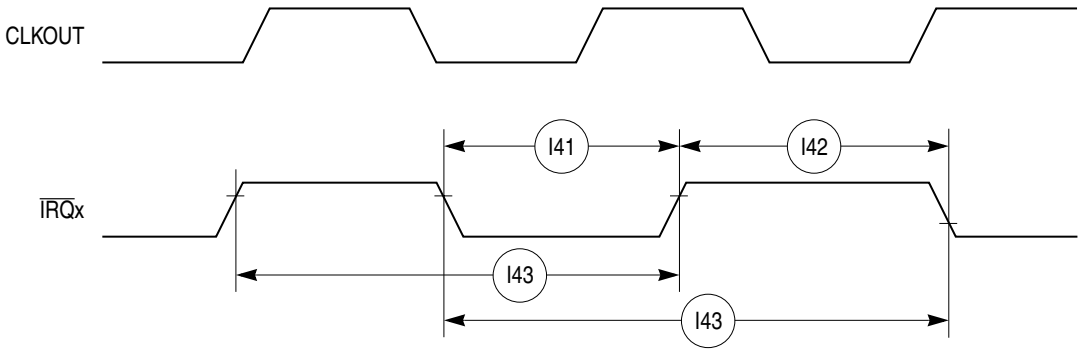


Figure 9-22. Interrupt Detection Timing for External Edge Sensitive Lines

Table 9-4 shows the PCMCIA timing for the MPC862/857T/857DSL.

Table 9-4. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P44	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA Strobe asserted. [1] (MIN = 0.75 x B1 - 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
P45	A(0:31), $\overline{\text{REG}}$ valid to ALE negation.[1] (MIN = 1.00 x B1 - 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid. (MIN = 0.25 x B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated. (MAX = 0.25 x B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time. (MAX = 0.00 x B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time. (MAX = 0.00 x B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
P52	CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
P53	CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid.[1] (MIN = 0.25 x B1 - 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9-4. PCMCIA Timing (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P55	$\overline{WAITA}$ and $\overline{WAITB}$ valid to CLKOUT rising edge.[1] (MIN = 0.00 x B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
P56	CLKOUT rising edge to $\overline{WAITA}$ and $\overline{WAITB}$ invalid.[1] (MIN = 0.00 x B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{WAITx}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{WAITx}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC862 PowerQUICC User s Manual.

Figure 9-23 provides the PCMCIA access cycle timing for the external bus read.

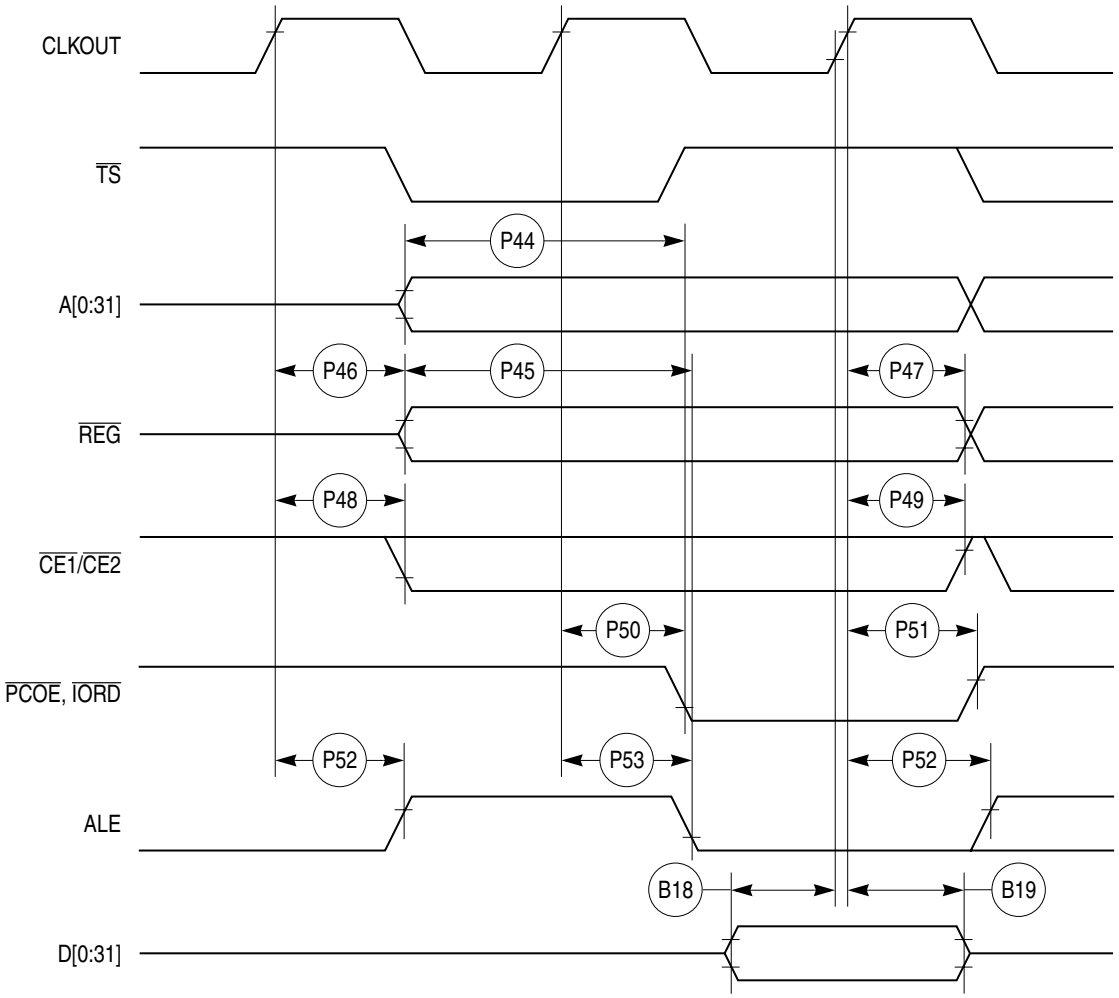


Figure 9-23. PCMCIA Access Cycles Timing External Bus Read

Figure 9-24 provides the PCMCIA access cycle timing for the external bus write.

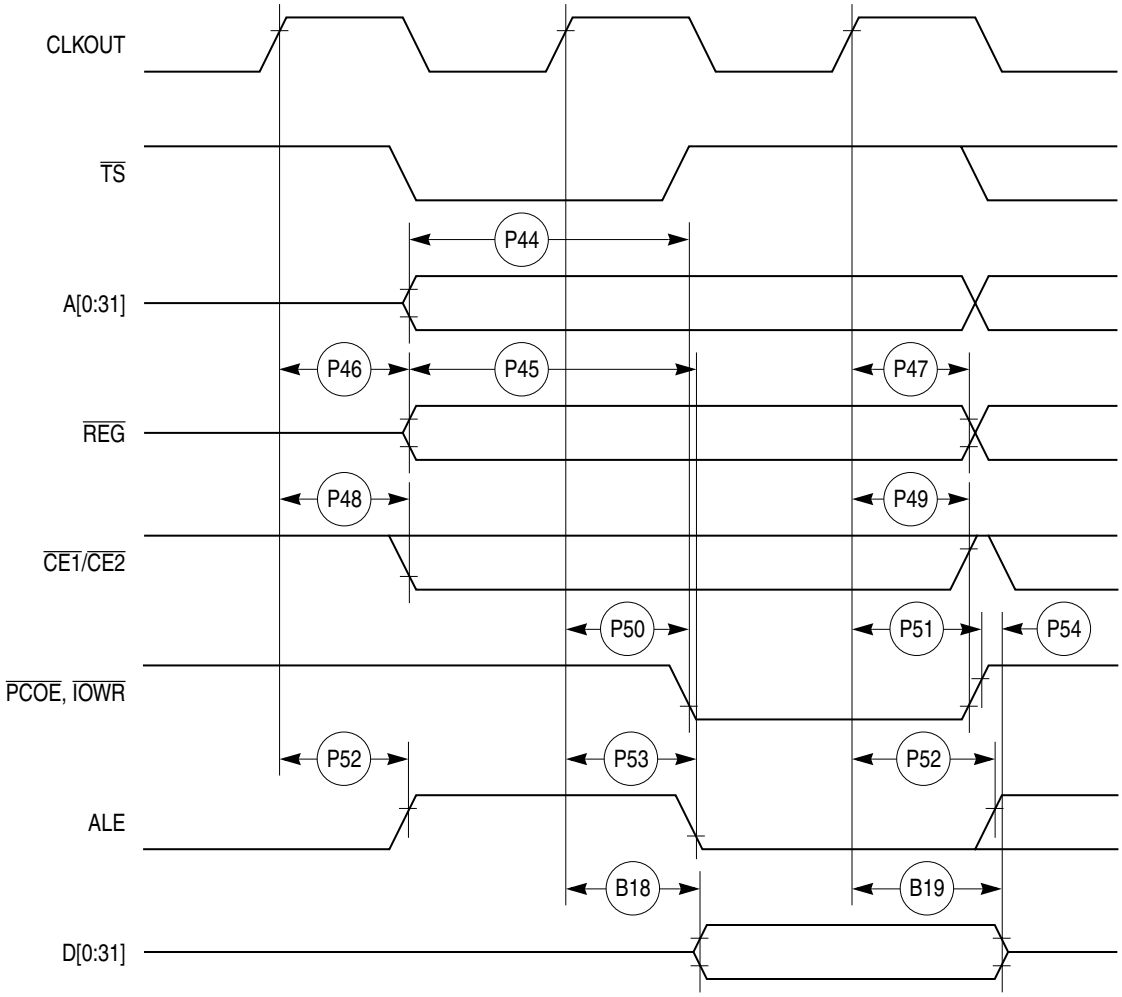


Figure 9-24. PCMCIA Access Cycles Timing External Bus Write

Figure 9-25 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

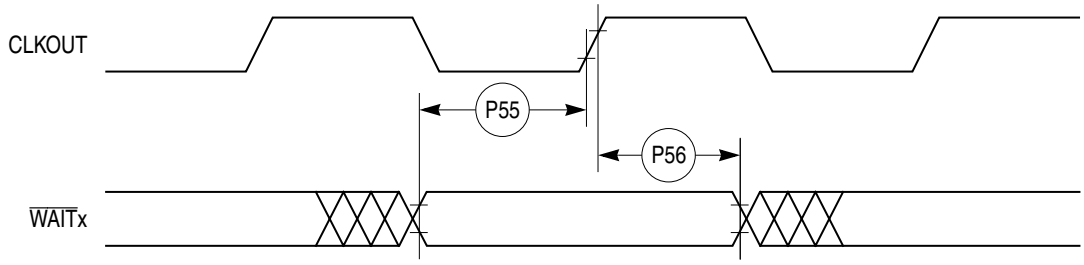


Figure 9-25. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 9-5 shows the PCMCIA port timing for the MPC862/857T/857DSL.

Table 9-5. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx Valid (MAX = 0.00 x B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1](MIN = 0.75 x B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
P59	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 x B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 x B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 9-26 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

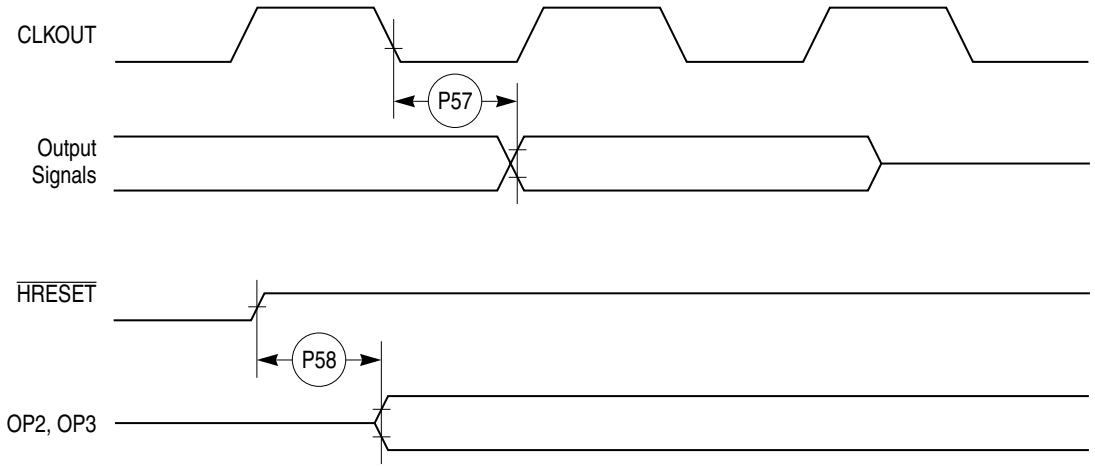


Figure 9-26. PCMCIA Output Port Timing

Figure 9-27 provides the PCMCIA output port timing for the MPC862/857T/857DSL.

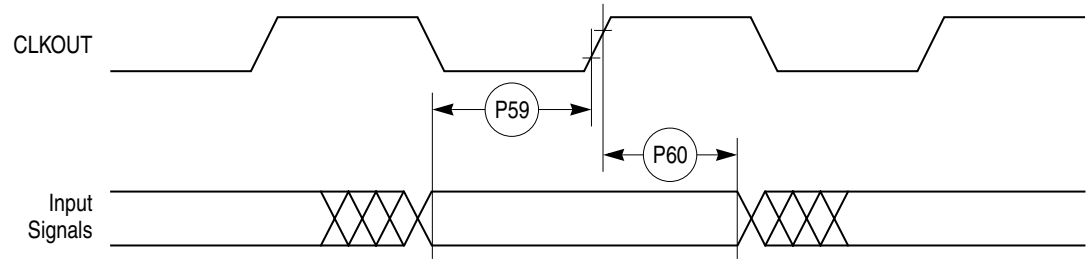


Figure 9-27. PCMCIA Input Port Timing

Table 9-6 shows the debug port timing for the MPC862/857T/857DSL.

Table 9-6. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
D61	DSCK cycle time	$3xT_{CLOCKOUT}$		-
D62	DSCK clock pulse width	$1.25xT_{CLOCKOUT}$		-
D63	DSCK rise and fall times	0.00	3.00	ns
D64	DSDI input data setup time	8.00		ns
D65	DSDI data hold time	5.00		ns
D66	DSCK low to DSDO data valid	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 9-28 provides the input timing for the debug port clock.

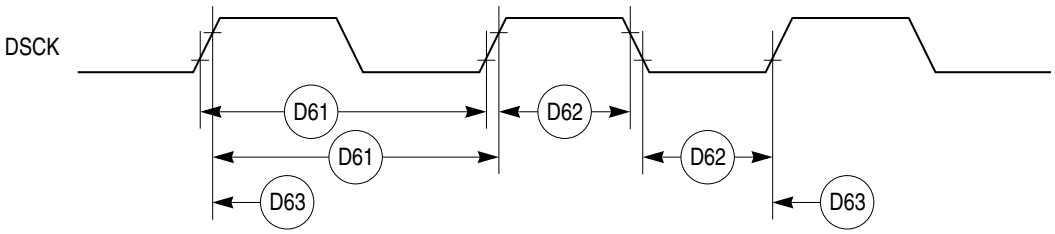


Figure 9-28. Debug Port Clock Input Timing

Figure 9-29 provides the timing for the debug port.

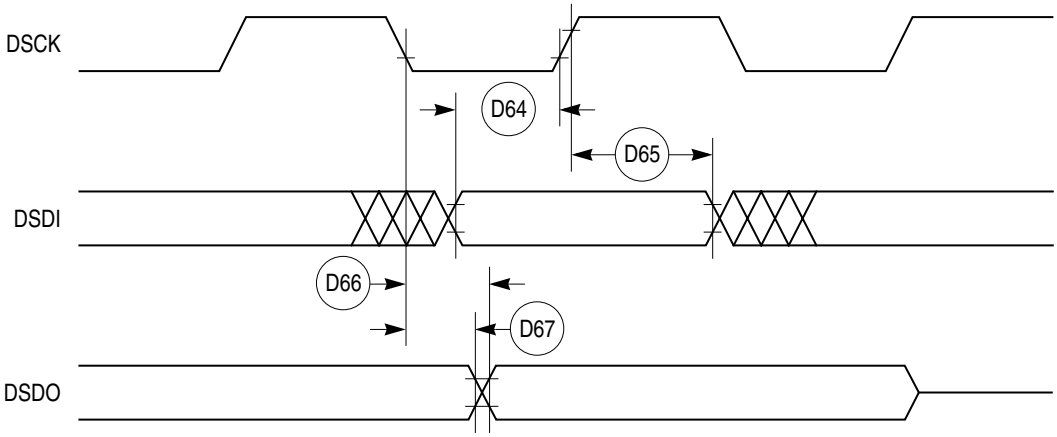


Figure 9-29. Debug Port Timings

Table 9-7 shows the reset timing for the MPC862/857T/857DSL.

Table 9-7. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
R71	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 x B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
R72	—	—	—	—	—	—	—	—	—	—
R73	Configuration data to HRESET rising edge set up time (MIN = 15.00 x B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time (MIN = 0.00 x B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R79	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance. (MAX = 0.00 x B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
R80	DSDI, DSCK set up (MIN = 3.00 x B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
R81	DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Figure 9-30 shows the reset timing for the data bus configuration.

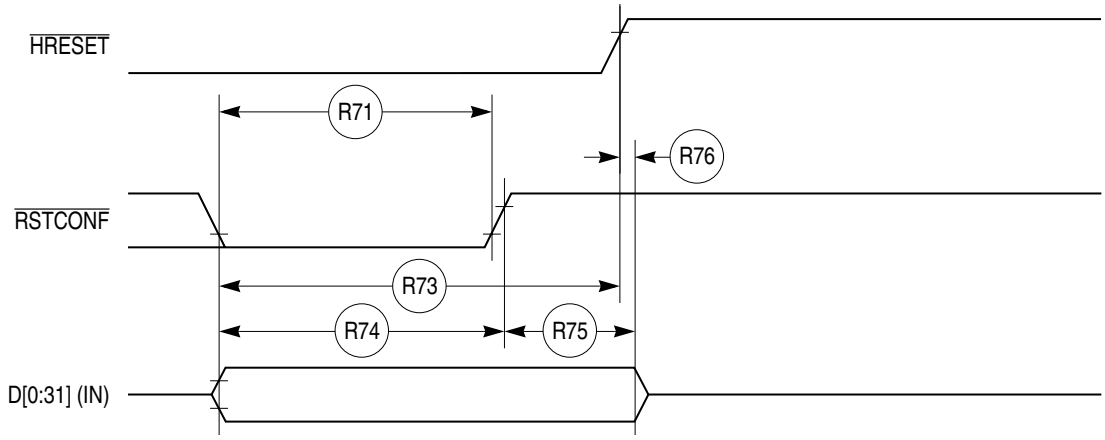


Figure 9-30. Reset Timing—Configuration from Data Bus

Figure 9-31 provides the reset timing for the data bus weak drive during configuration.

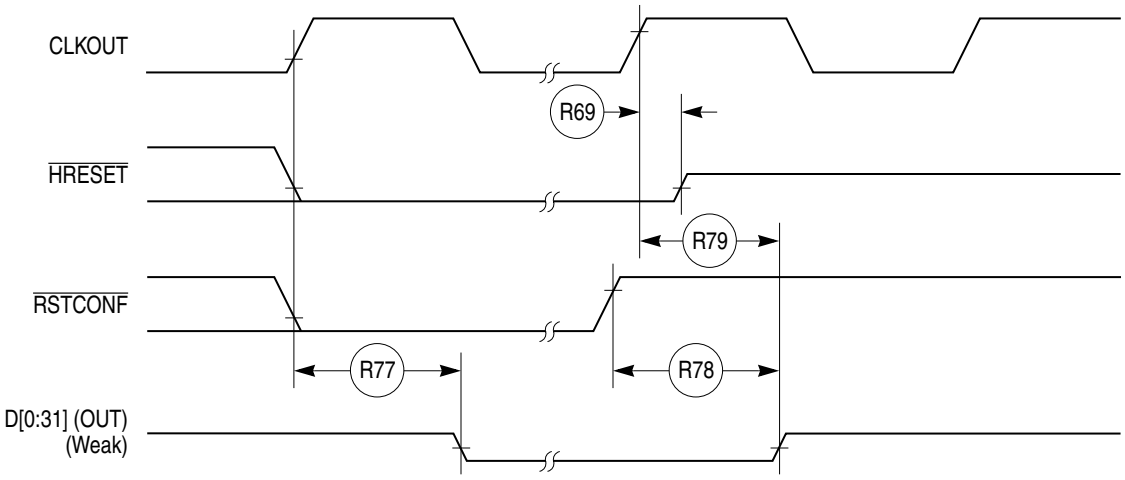


Figure 9-31. Reset Timing—Data Bus Weak Drive during Configuration

Figure 9-32 provides the reset timing for the debug port configuration.

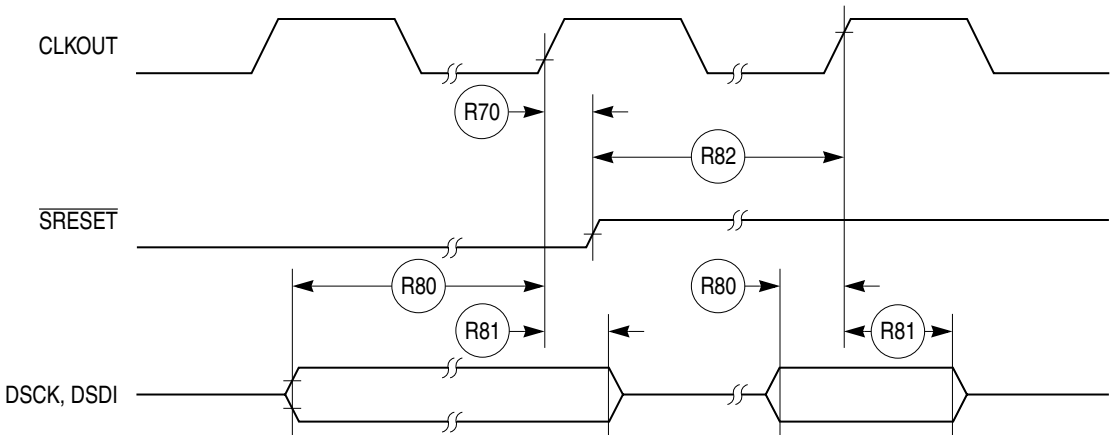


Figure 9-32. Reset Timing—Debug Port Configuration

Part X IEEE 1149.1 Electrical Specifications

Table 10-1 provides the JTAG timings for the MPC862/857T/857DSL shown in Figure 10-1 to Figure 10-4.

Table 10-1. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

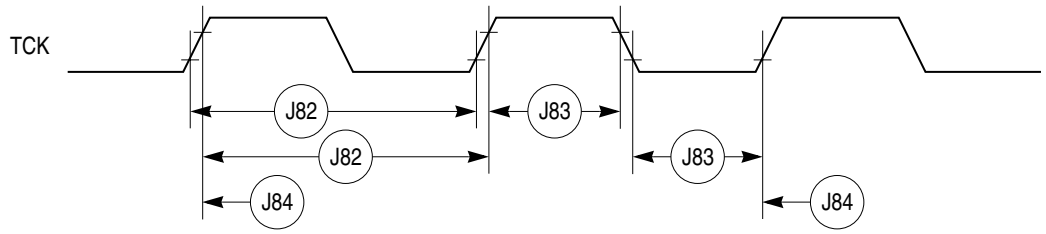


Figure 10-1. JTAG Test Clock Input Timing

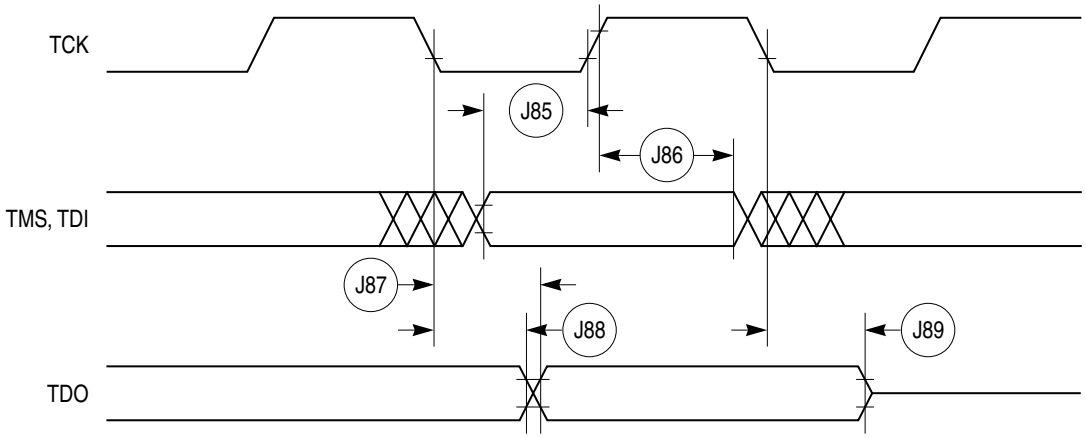


Figure 10-2. JTAG Test Access Port Timing Diagram

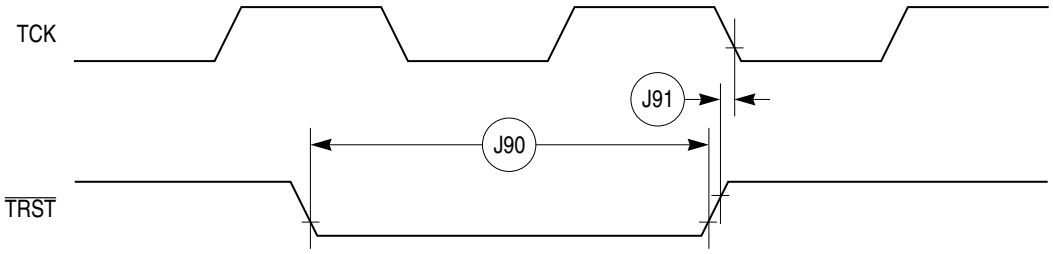


Figure 10-3. JTAG $\overline{\text{TRST}}$ Timing Diagram

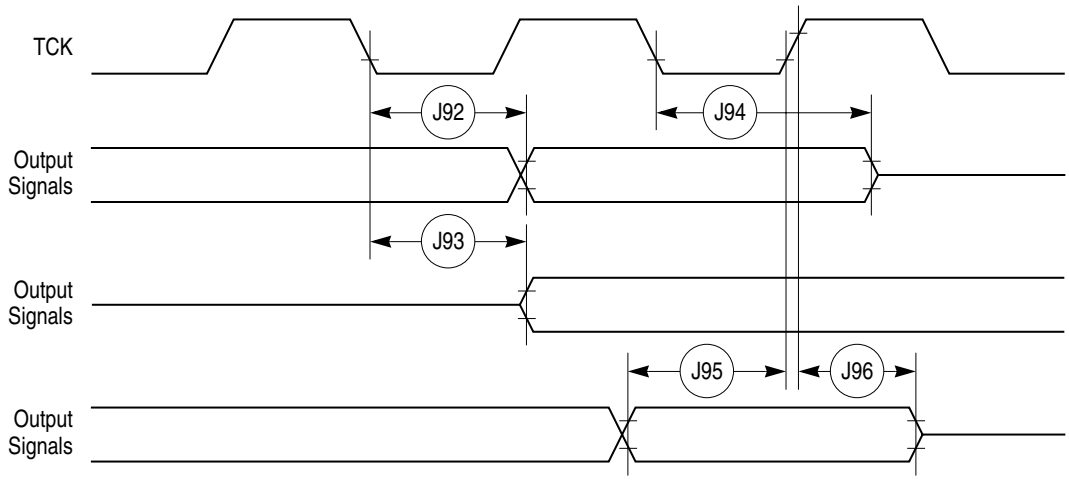


Figure 10-4. Boundary Scan (JTAG) Timing Diagram

Part XI CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC862/857T/857DSL.

11.1 PIP/PIO AC Electrical Specifications

Table 11-1 provides the PIP/PIO AC timings as shown in Figure 11-1 to Figure 11-5.

Table 11-1. PIP/PIO Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
21	Data-in setup time to STBI low	0	—	ns
22	Data-In hold time to STBI high	2.5 – t3 [1]	—	clk
23	STBI pulse width	1.5	—	clk
24	STBO pulse width	1 clk – 5ns	—	ns
25	Data-out setup time to STBO low	2	—	clk
26	Data-out hold time from STBO high	5	—	clk
27	STBI low to STBO low (Rx interlock)	—	2	clk
28	STBI low to STBO high (Tx interlock)	2	—	clk
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

[1] t3 = Specification 23

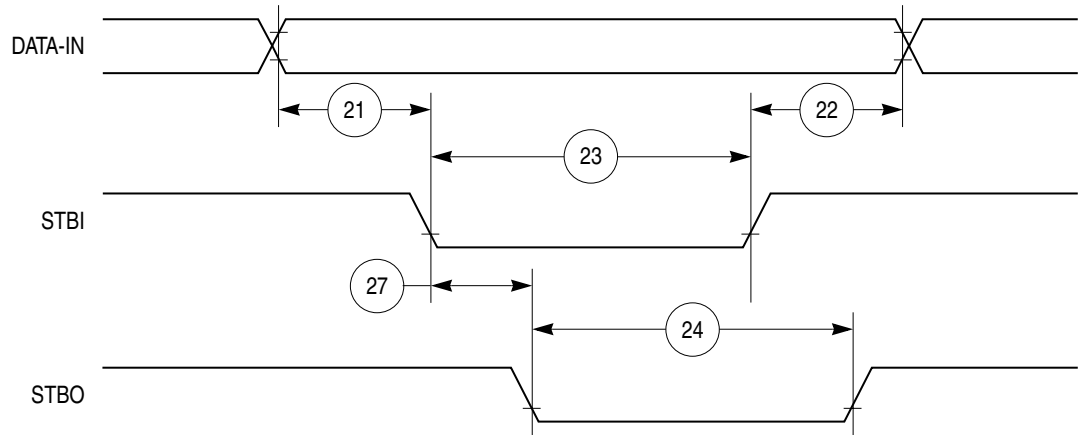


Figure 11-1. PIP Rx (Interlock Mode) Timing Diagram

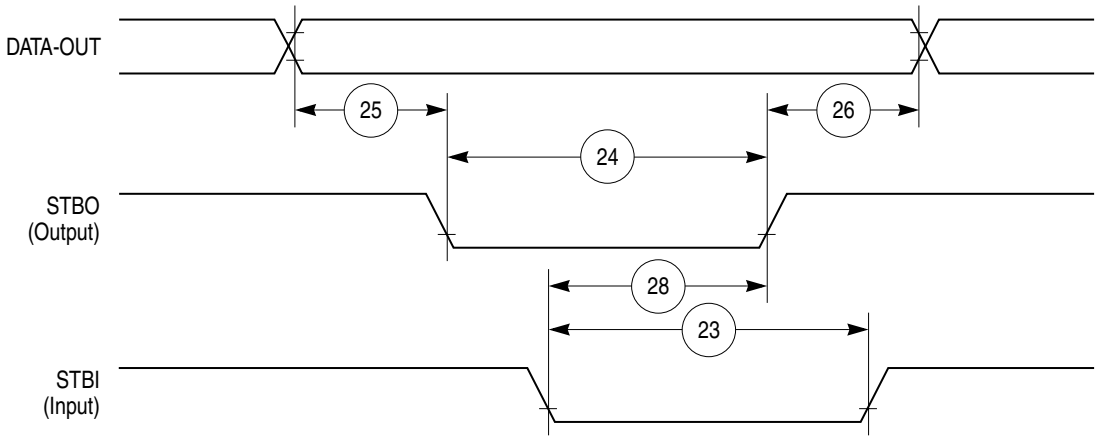


Figure 11-2. PIP Tx (Interlock Mode) Timing Diagram

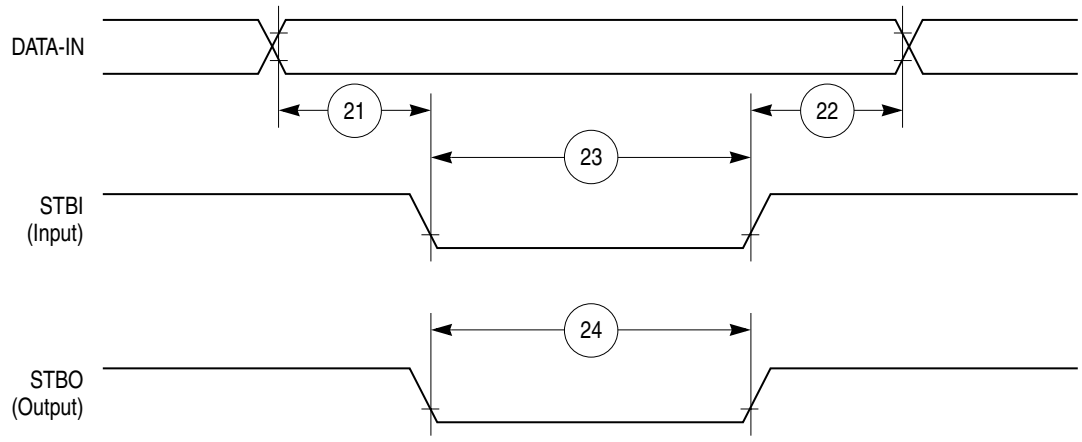


Figure 11-3. PIP Rx (Pulse Mode) Timing Diagram

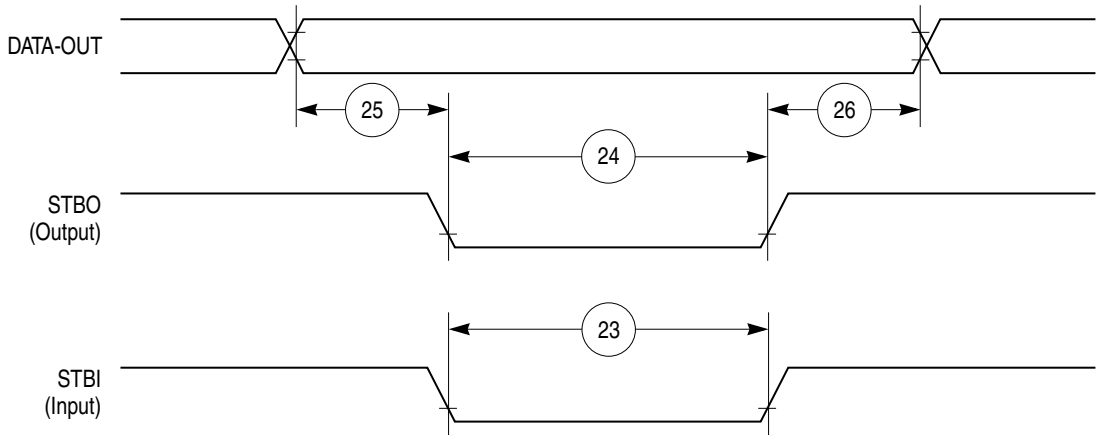


Figure 11-4. PIP TX (Pulse Mode) Timing Diagram

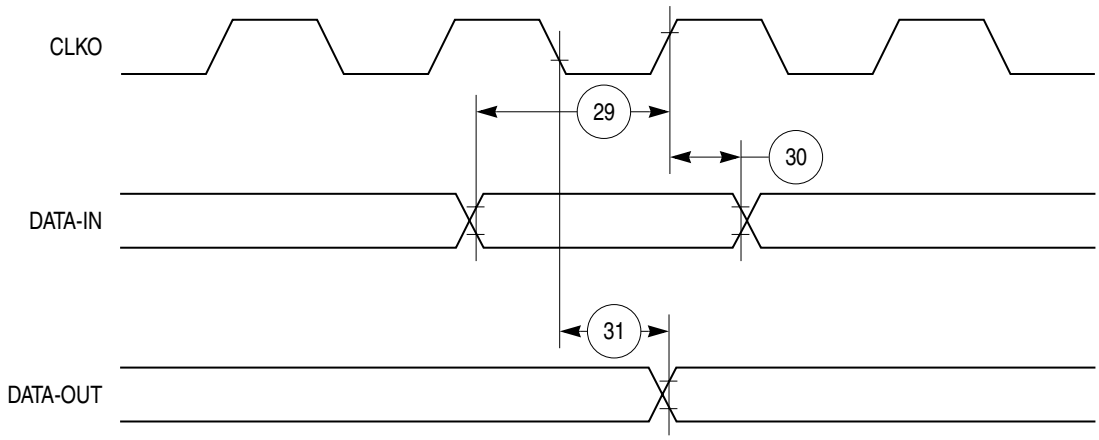


Figure 11-5. Parallel I/O Data-In/Data-Out Timing Diagram

11.2 Port C Interrupt AC Electrical Specifications

Table 11-2 provides the timings for port C interrupts.

Table 11-2. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 11-6 shows the port C interrupt detection timing.

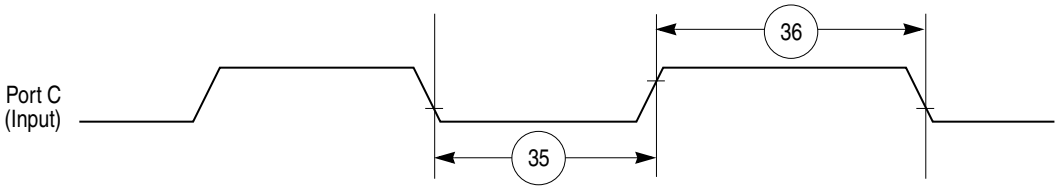


Figure 11-6. Port C Interrupt Detection Timing

11.3 IDMA Controller AC Electrical Specifications

Table 11-3 provides the IDMA controller timings as shown in Figure 11-7 to Figure 11-10.

Table 11-3. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

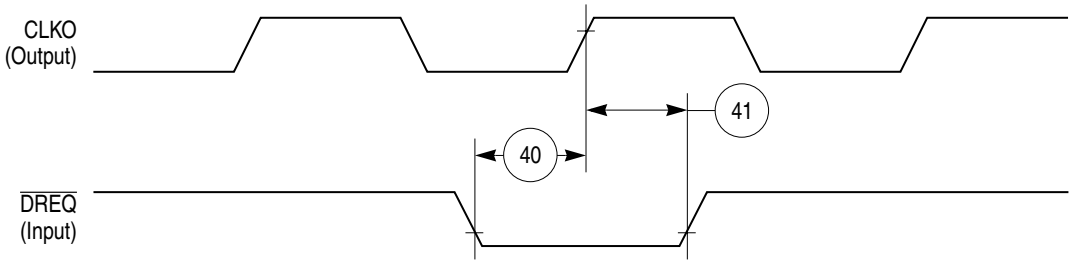


Figure 11-7. IDMA External Requests Timing Diagram

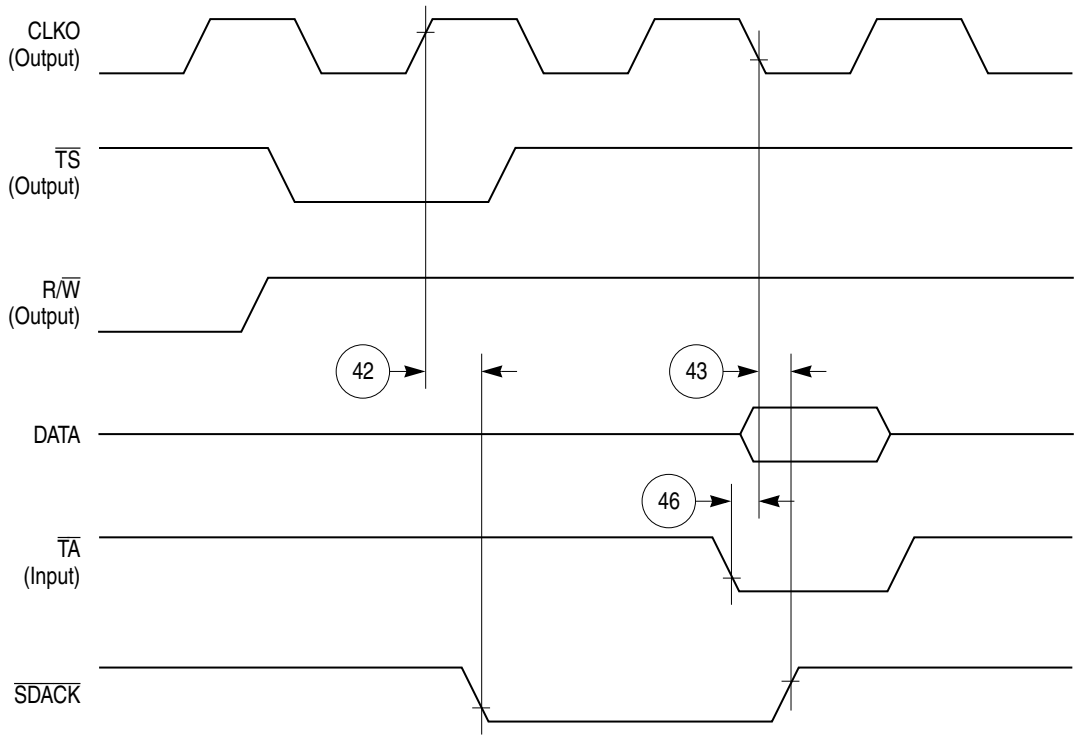


Figure 11-8. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

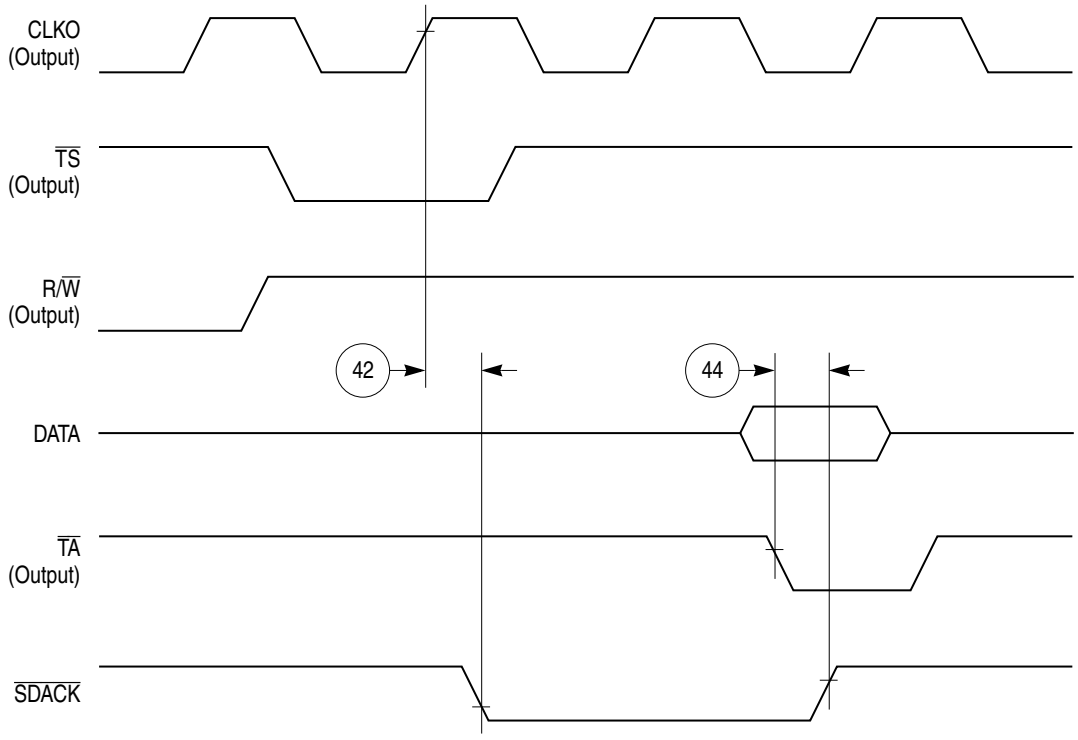


Figure 11-9. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

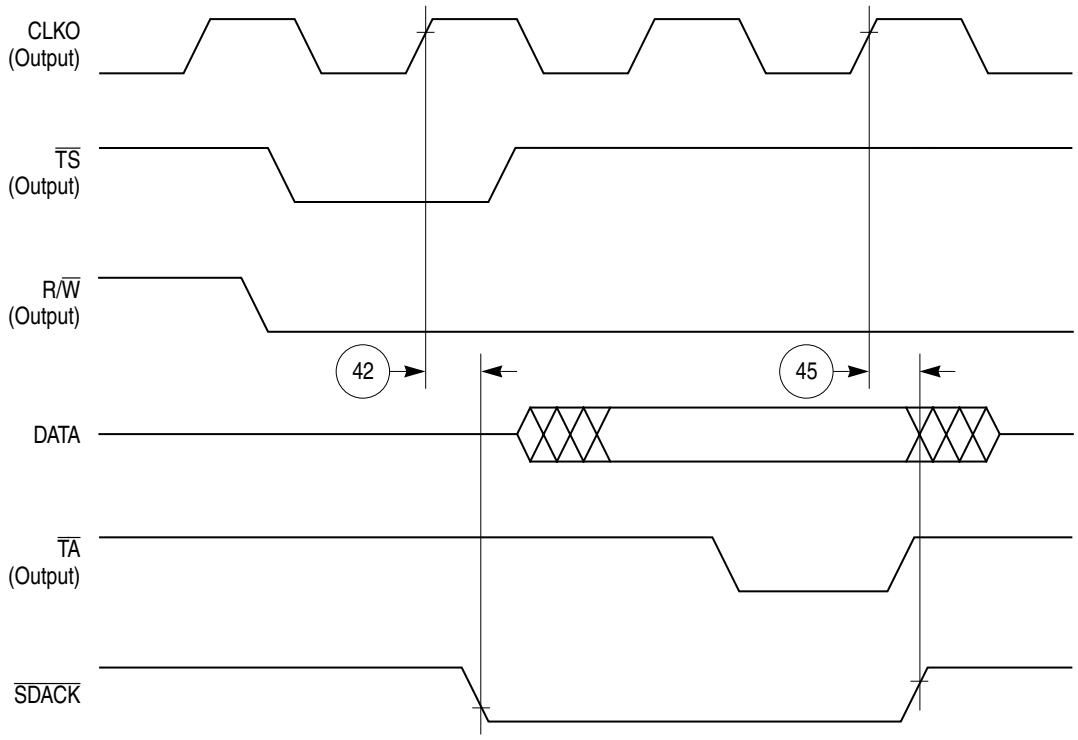


Figure 11-10. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

11.4 Baud Rate Generator AC Electrical Specifications

Table 11-4 provides the baud rate generator timings as shown in Figure 11-11.

Table 11-4. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

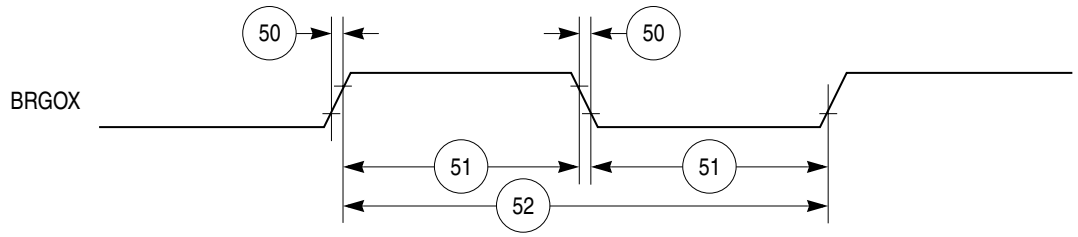


Figure 11-11. Baud Rate Generator Timing Diagram

11.5 Timer AC Electrical Specifications

Table 11-5 provides the general-purpose timer timings as shown in Figure 11-12.

Table 11-5. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	clk
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

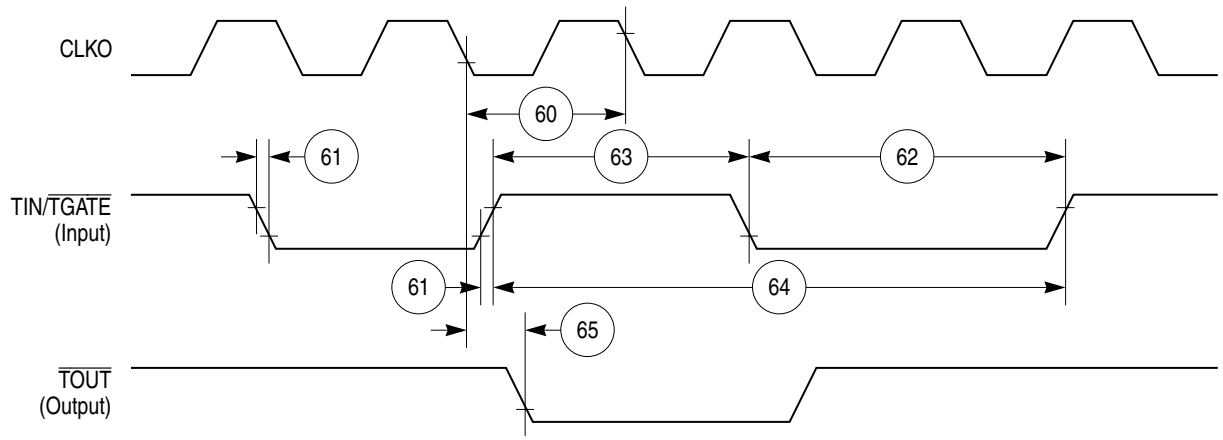


Figure 11-12. CPM General-Purpose Timers Timing Diagram

11.6 Serial Interface AC Electrical Specifications

Table 11-6 provides the serial interface timings as shown in Figure 11-13 to Figure 11-17.

Table 11-6. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time)	20.00	—	ns

Table 11-6. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
74	L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1CLK edge (L1RXD setup time)	17.00	—	ns
77	L1CLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1CLK edge to L1ST(1–4) valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST(1–4) valid	10.00	45.00	ns
79	L1CLK edge to L1ST(1–4) invalid	10.00	45.00	ns
80	L1CLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1CLK edge to L1TXD high impedance	0.00	42.00	ns
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83a	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

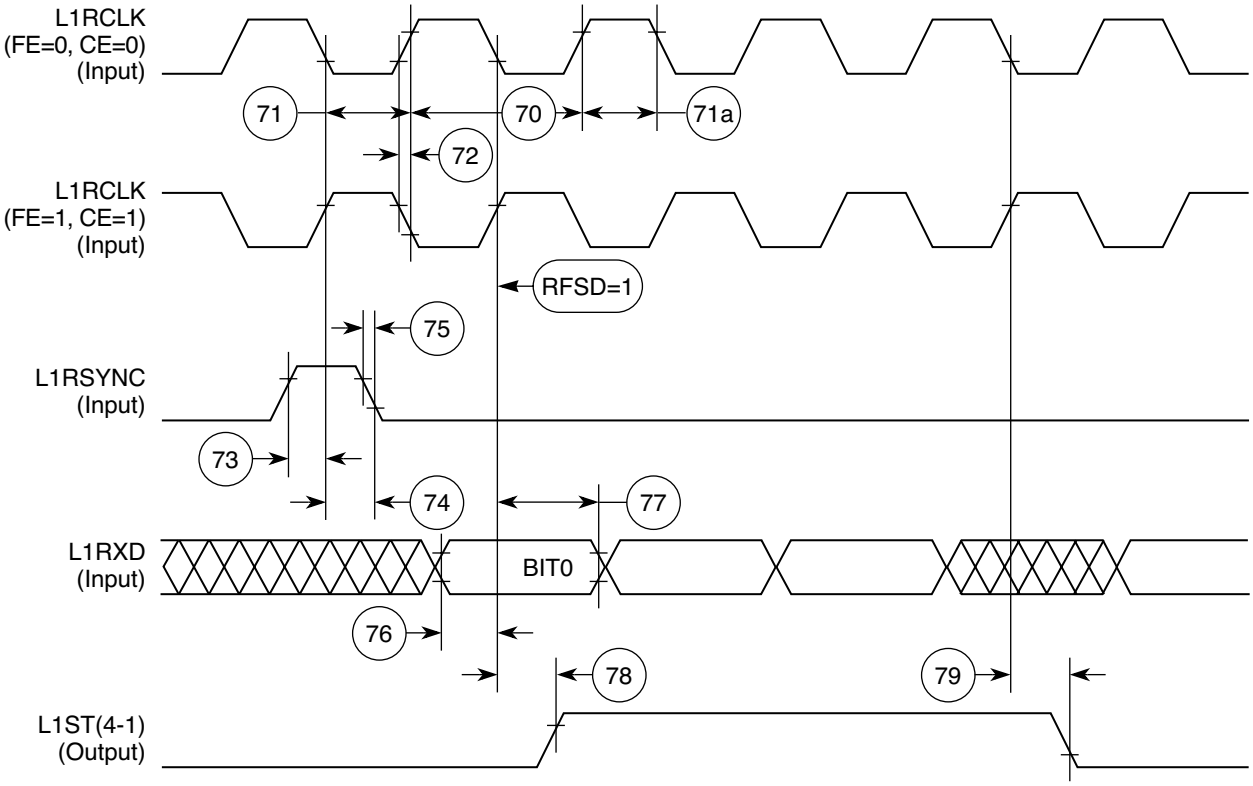


Figure 11-13. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

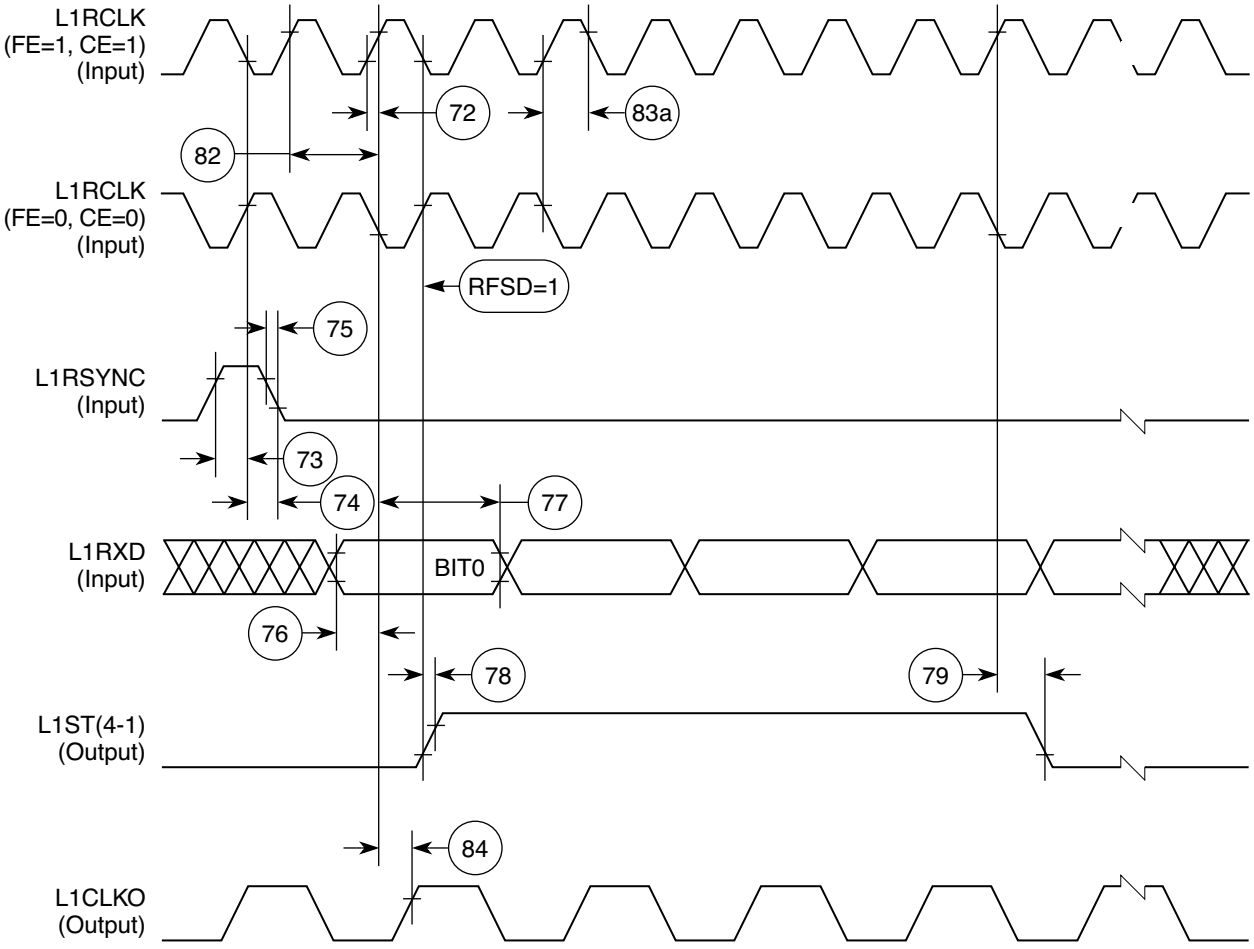


Figure 11-14. SI Receive Timing with Double-Speed Clocking (DSC = 1)

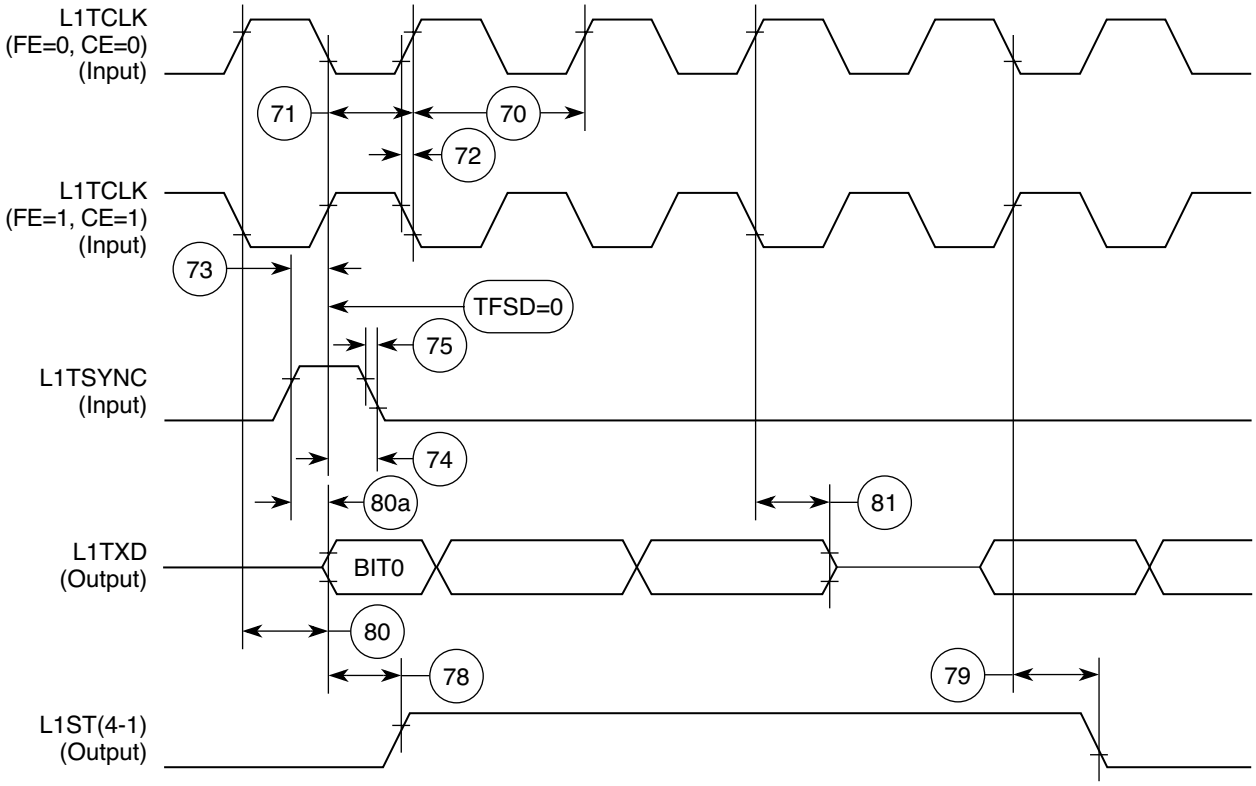


Figure 11-15. SI Transmit Timing Diagram (DSC = 0)

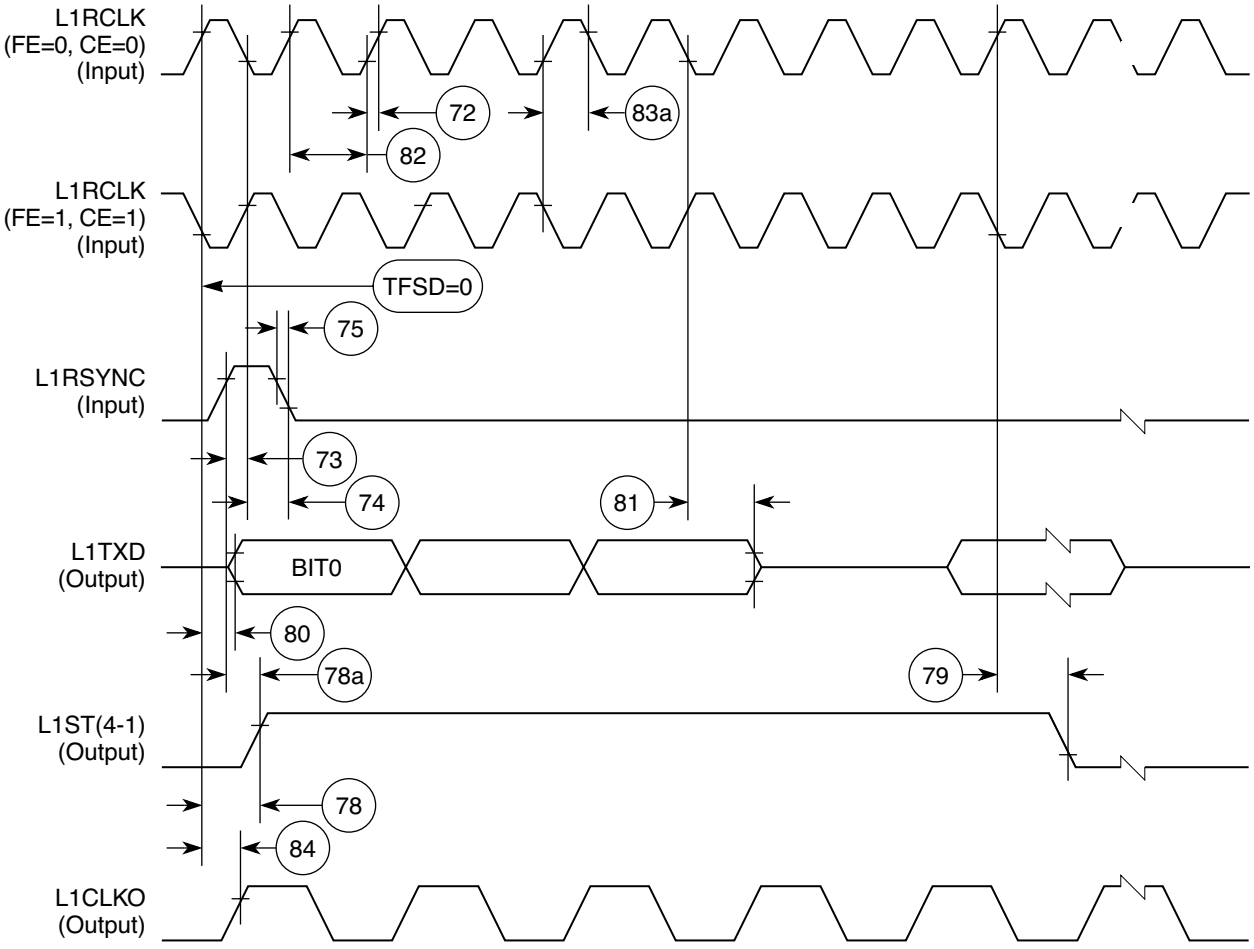


Figure 11-16. SI Transmit Timing with Double Speed Clocking (DSC = 1)

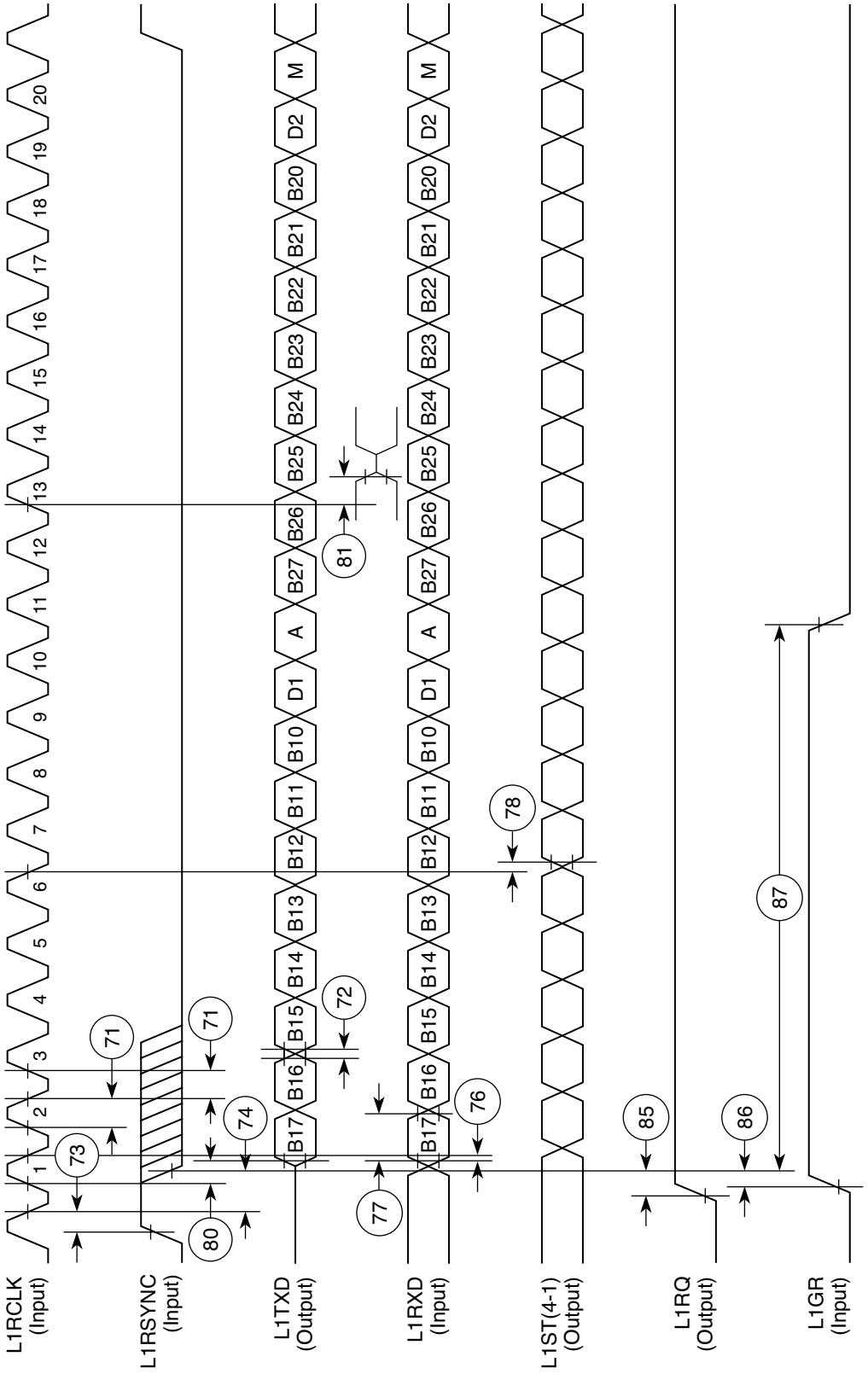


Figure 11-17. IDL Timing

11.7 SCC in NMSI Mode Electrical Specifications

Table 11-7 provides the NMSI external clock timing.

Table 11-7. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 width high [1]	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 width low	1/SYNCCLK +5	—	ns
102	RCLK1 and TCLK1 rise/fall time	—	15.00	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	5.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	5.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD1}}$ setup Time to RCLK1 rising edge	5.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 11-8 provides the NMSI internal clock timing.

Table 11-8. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK1 and TCLK1 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK1 and TCLK1 rise/fall time	—	—	ns
103	TXD1 active delay (from TCLK1 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS1}}$ setup time to TCLK1 rising edge	40.00	—	ns
106	RXD1 setup time to RCLK1 rising edge	40.00	—	ns
107	RXD1 hold time from RCLK1 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD1}}$ setup time to RCLK1 rising edge	40.00	—	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 11-18 through Figure 11-20 show the NMSI timings.

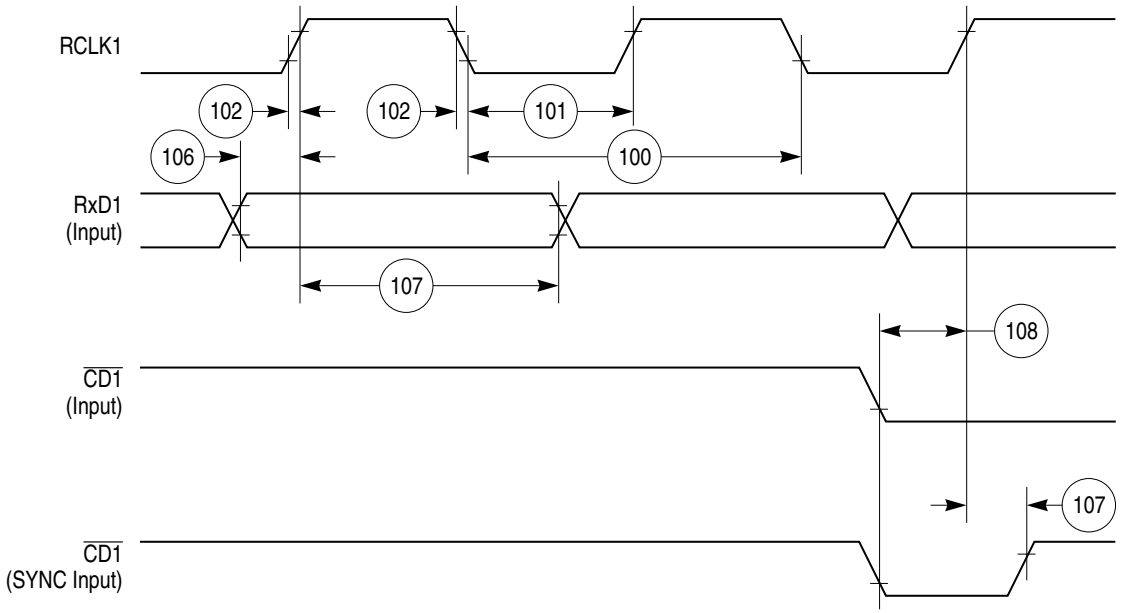


Figure 11-18. SCC NMSI Receive Timing Diagram

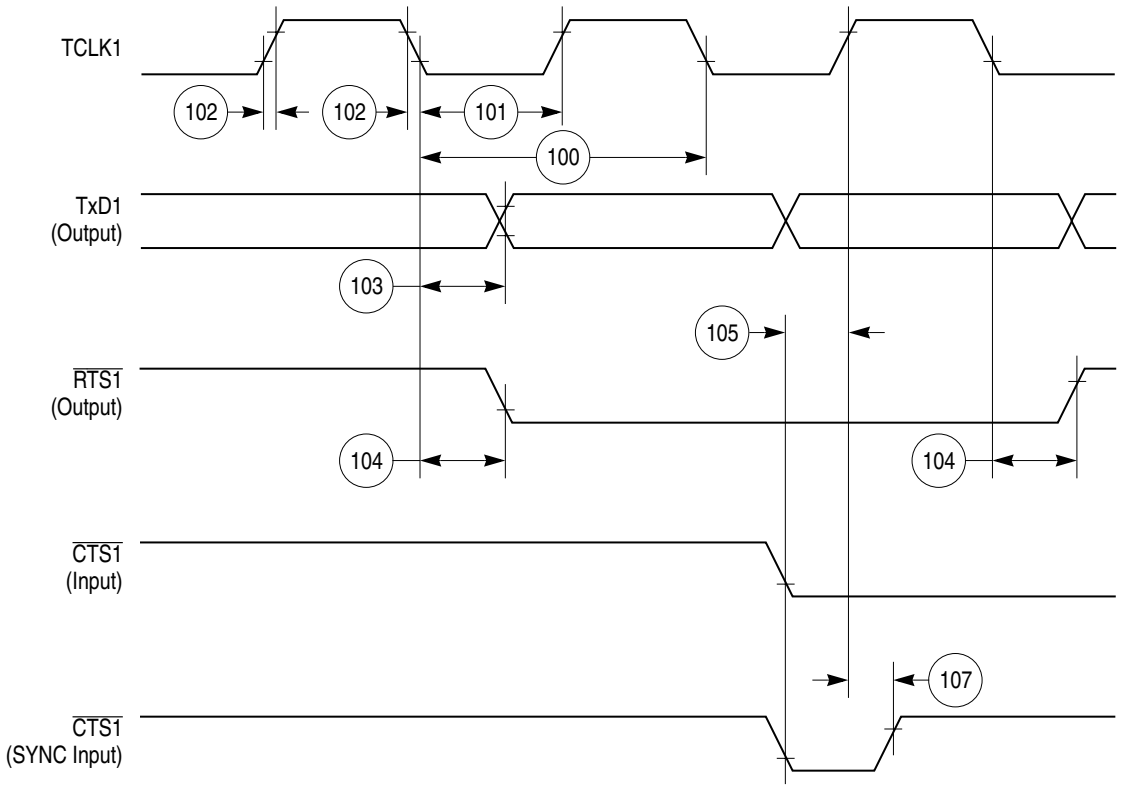


Figure 11-19. SCC NMSI Transmit Timing Diagram

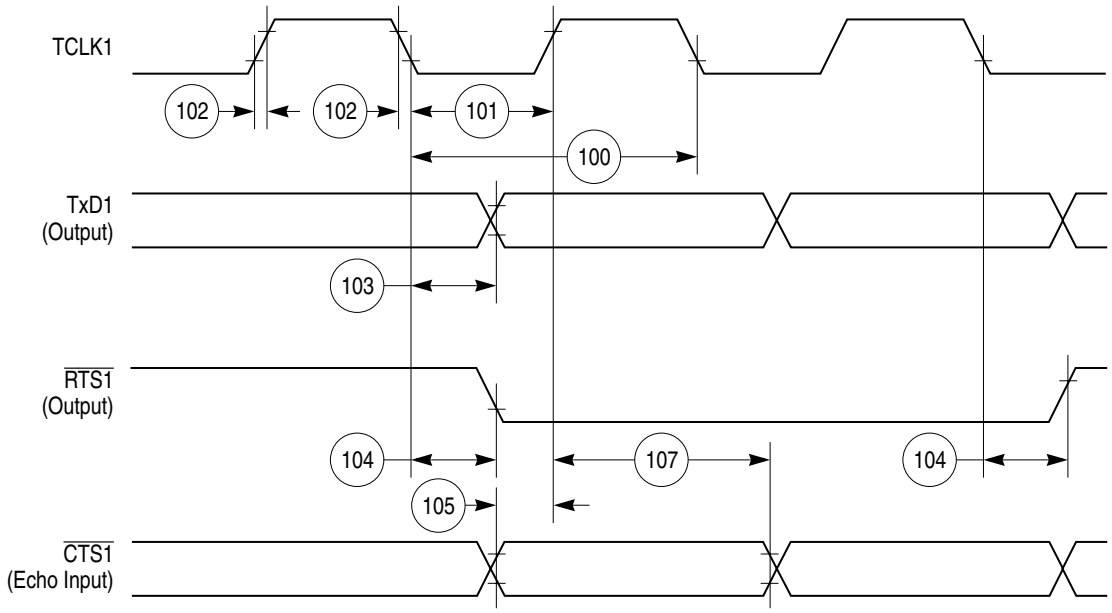


Figure 11-20. HDLC Bus Timing Diagram

11.8 Ethernet Electrical Specifications

Table 11-9 provides the Ethernet timings as shown in Figure 11-21 to Figure 11-25.

Table 11-9. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK1 rise/fall time	—	15	ns
122	RCLK1 width low	40	—	ns
123	RCLK1 clock period [1]	80	120	ns
124	RXD1 setup time	20	—	ns
125	RXD1 hold time	5	—	ns
126	RENA active delay (from RCLK1 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK1 rise/fall time	—	15	ns
129	TCLK1 width low	40	—	ns
130	TCLK1 clock period[1]	99	101	ns
131	TXD1 active delay (from TCLK1 rising edge)	10	50	ns
132	TXD1 inactive delay (from TCLK1 rising edge)	10	50	ns
133	TENA active delay (from TCLK1 rising edge)	10	50	ns

Table 11-9. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK1 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

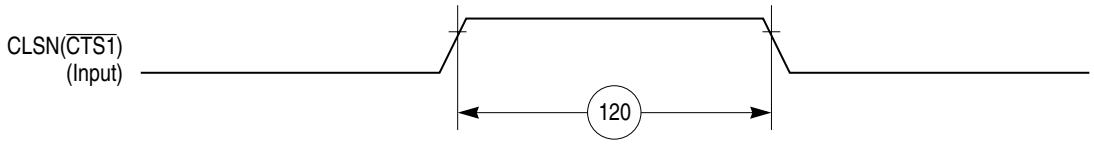


Figure 11-21. Ethernet Collision Timing Diagram

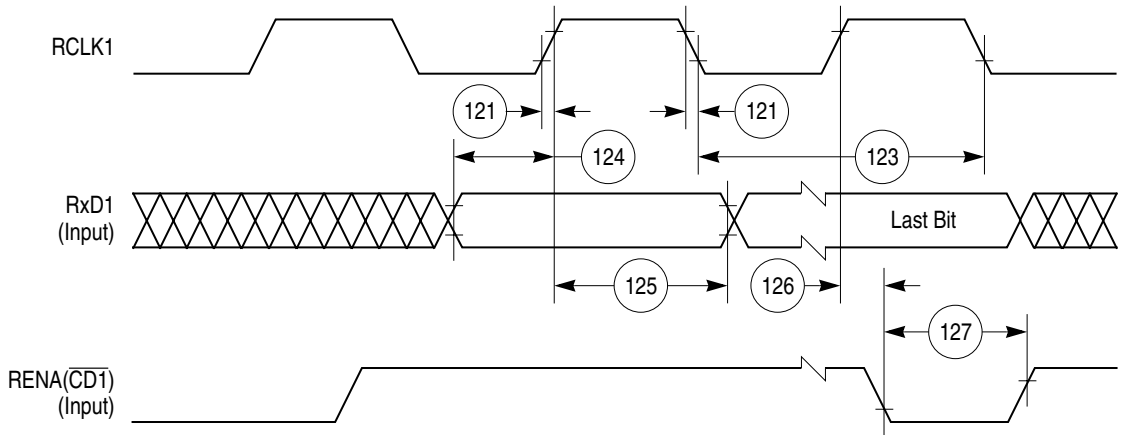
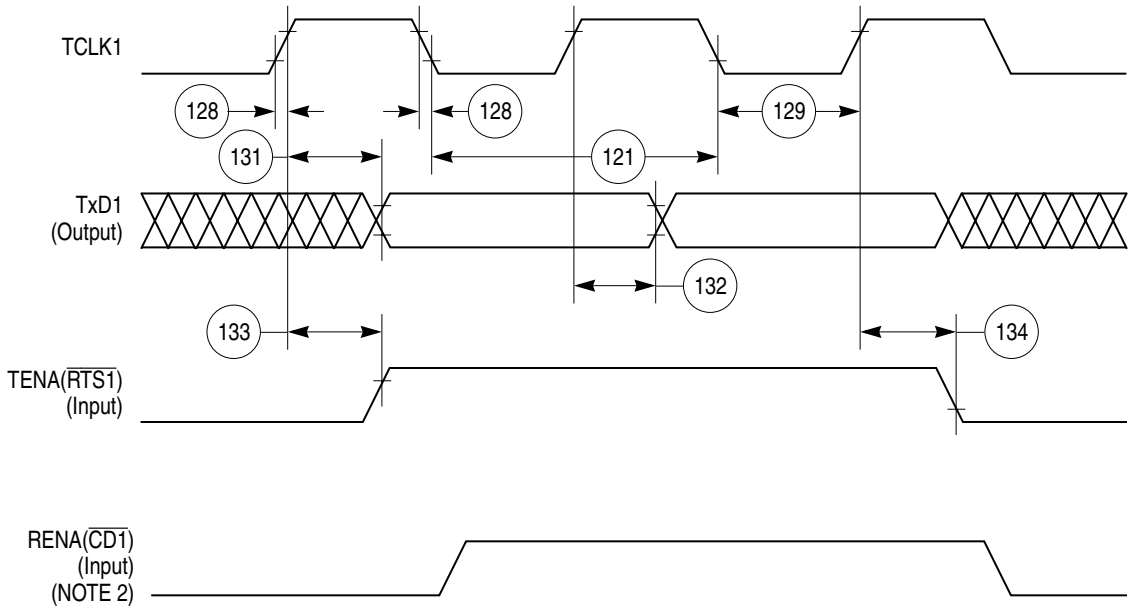


Figure 11-22. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 11-23. Ethernet Transmit Timing Diagram

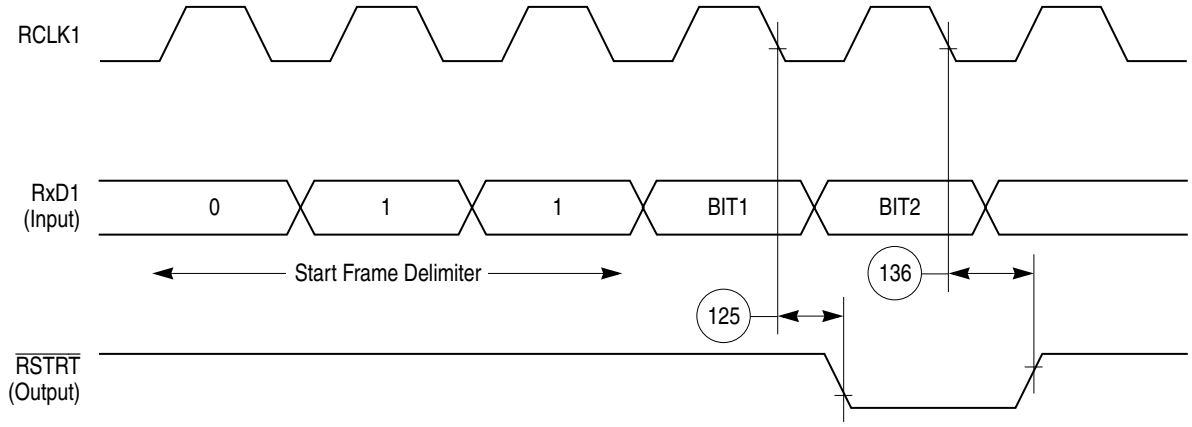


Figure 11-24. CAM Interface Receive Start Timing Diagram

Figure 11-25. CAM Interface REJECT Timing Diagram

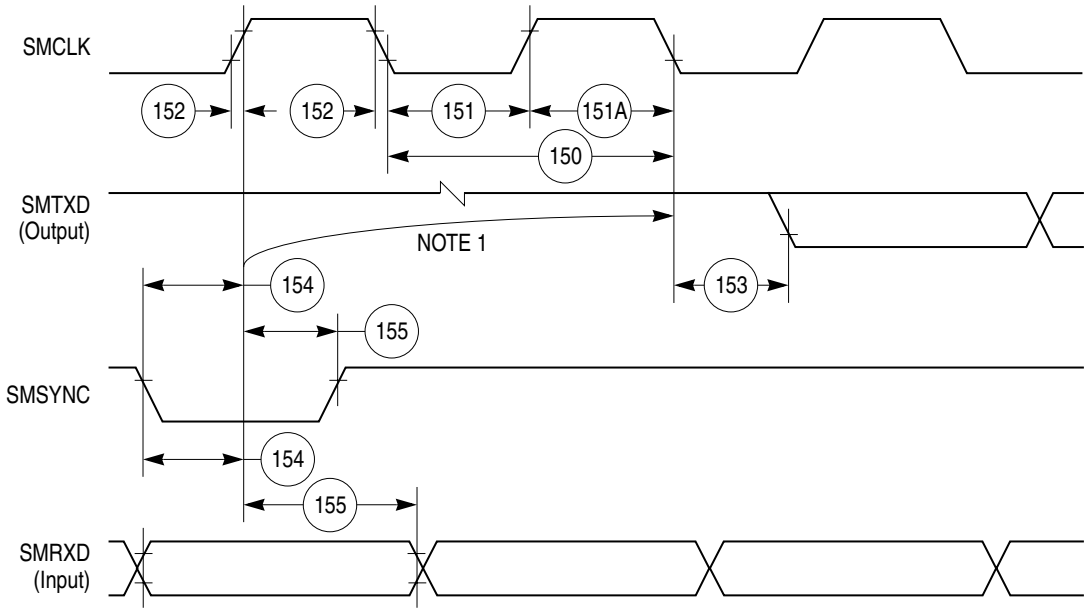
11.9 SMC Transparent AC Electrical Specifications

Table 11-10 provides the SMC transparent timings as shown in Figure 11-26.

Table 11-10. SMC Transparent Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLK clock period [1]	100	—	ns
151	SMCLK width low	50	—	ns
151A	SMCLK width high	50	—	ns
152	SMCLK rise/fall time	—	15	ns
153	SMTXD active delay (from SMCLK falling edge)	10	50	ns
154	SMRXD/SMSYNC setup time	20	—	ns
155	RXD1/SMSYNC hold time	5	—	ns

[1] SyncCLK must be at least twice as fast as SMCLK.



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 11-26. SMC Transparent Timing Diagram

11.10 SPI Master AC Electrical Specifications

Table 11-11 provides the SPI master timings as shown in Figure 11-27 and Figure 11-28.

Table 11-11. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

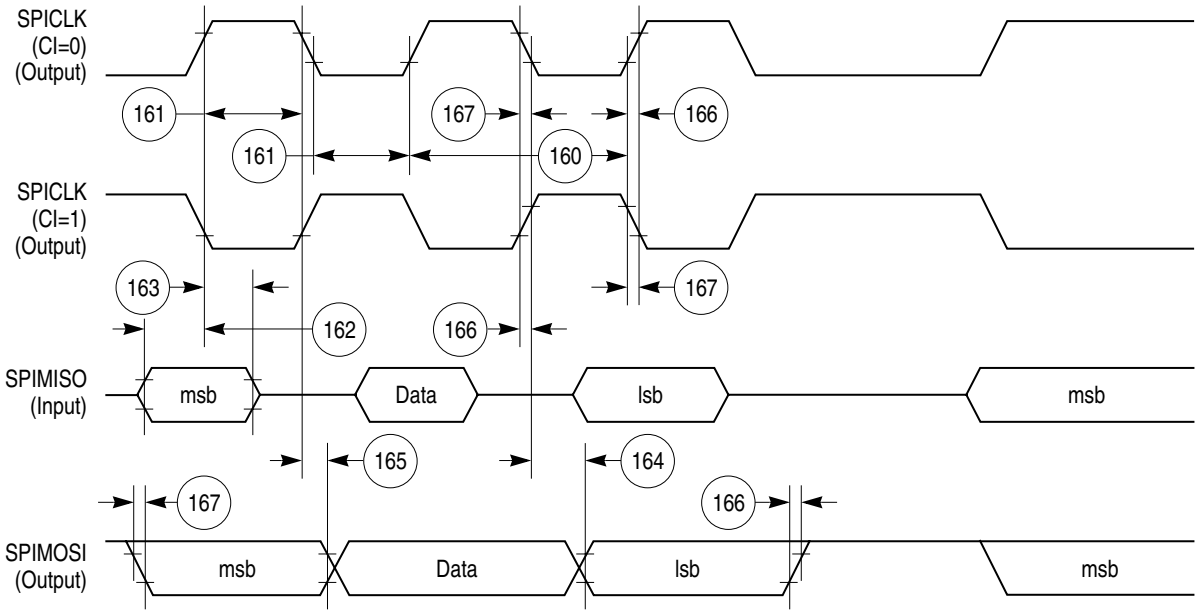


Figure 11-27. SPI Master (CP = 0) Timing Diagram

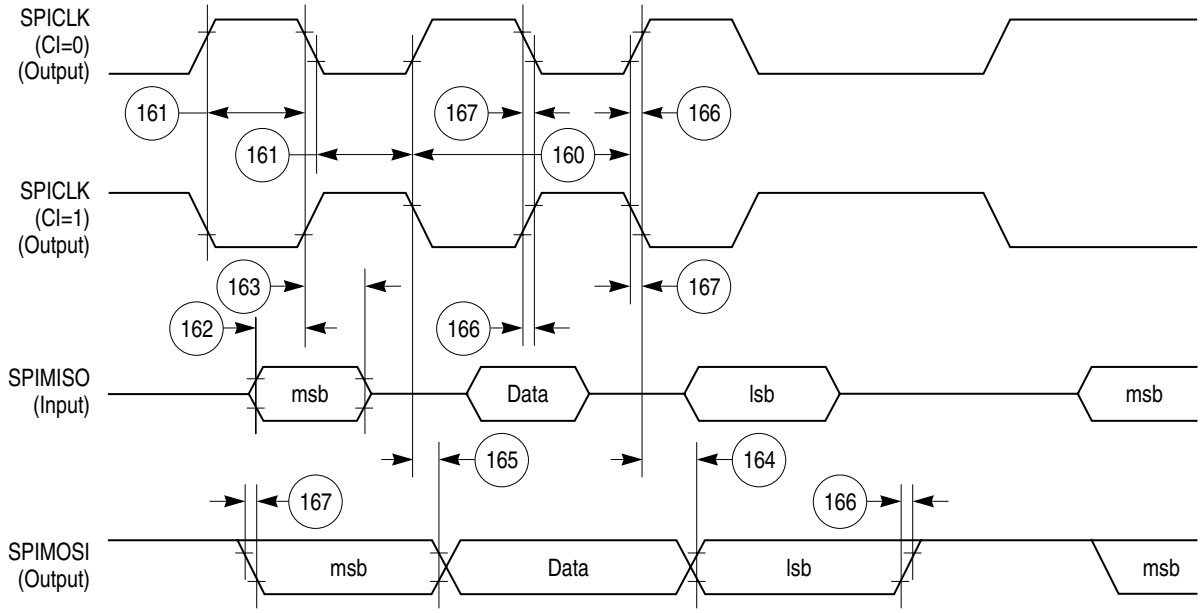


Figure 11-28. SPI Master (CP = 1) Timing Diagram

11.11 SPI Slave AC Electrical Specifications

Table 11-12 provides the SPI slave timings as shown in Figure 11-29 and Figure 11-30.

Table 11-12. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

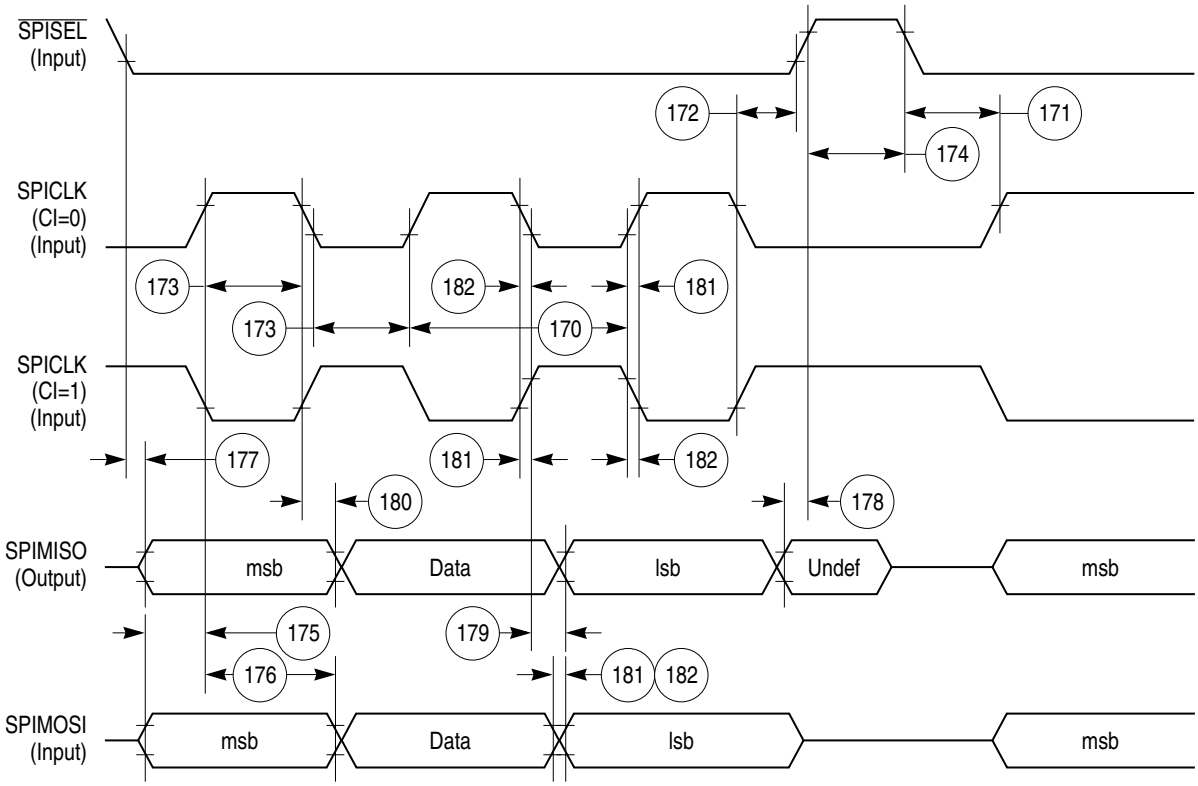


Figure 11-29. SPI Slave (CP = 0) Timing Diagram

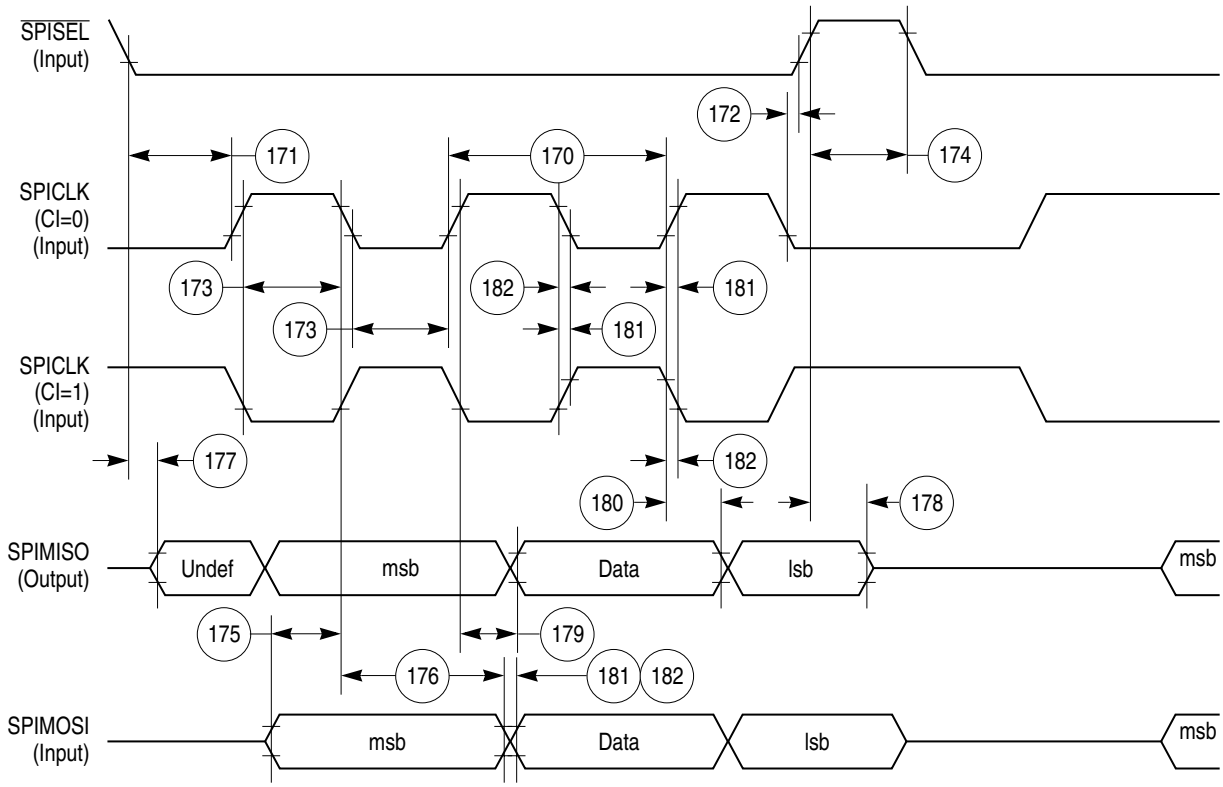


Figure 11-30. SPI Slave (CP = 1) Timing Diagram

11.12 I²C AC Electrical Specifications

Table 11-13 provides the I²C (SCL < 100 KHz) timings.

Table 11-13. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0	100	KHz
200	SCL clock frequency (master) [1]	1.5	100	KHz
202	Bus free time between transmissions	4.7	—	μs
203	Low period of SCL	4.7	—	μs
204	High period of SCL	4.0	—	μs
205	Start condition setup time	4.7	—	μs
206	Start condition hold time	4.0	—	μs
207	Data hold time	0	—	μs
208	Data setup time	250	—	ns
209	SDL/SCL rise time	—	1	μs
210	SDL/SCL fall time	—	300	ns
211	Stop condition setup time	4.7	—	μs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 11-14 provides the I²C (SCL > 100 KHz) timings.

Table 11-14. I²C Timing (SCL > 100 KHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) [1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions	—	1/(2.2 * fSCL)	—	s
203	Low period of SCL	—	1/(2.2 * fSCL)	—	s
204	High period of SCL	—	1/(2.2 * fSCL)	—	s
205	Start condition setup time	—	1/(2.2 * fSCL)	—	s
206	Start condition hold time	—	1/(2.2 * fSCL)	—	s
207	Data hold time	—	0	—	s
208	Data setup time	—	1/(40 * fSCL)	—	s
209	SDL/SCL rise time	—	—	1/(10 * fSCL)	s
210	SDL/SCL fall time	—	—	1/(33 * fSCL)	s
211	Stop condition setup time	—	1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 11-31 shows the I^2C bus timing.

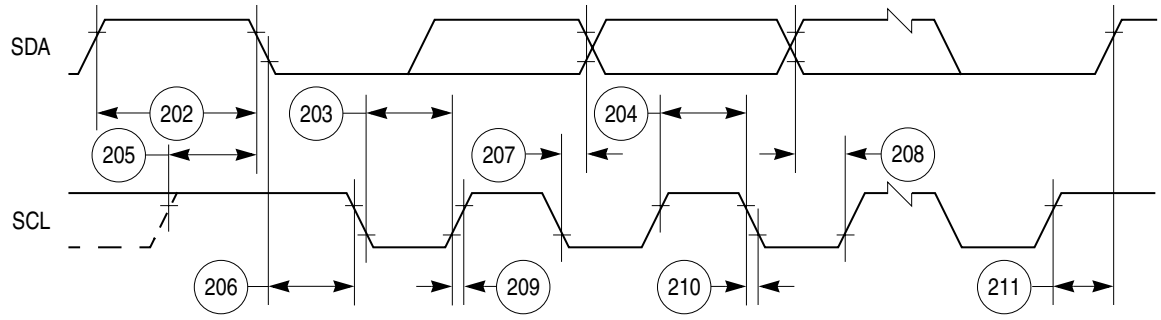


Figure 11-31. I^2C Bus Timing Diagram

Part XII UTOPIA AC Electrical Specifications

Table 12-15 shows the AC electrical specifications for the UTOPIA interface.

Table 12-15. UTOPIA AC Electrical Specifications

Num	Signal Characteristic	Direction	Min	Max	Unit
U1	UtpClk rise/fall time (Internal clock option)	Output		4ns	ns
	Duty cycle		50	50	%
	Frequency			33	Mhz
U1a	UtpClk rise/fall time (external clock option)	Input		4ns	ns
	Duty cycle		40	60	%
	Frequency			33	Mhz
U2	$\overline{\text{RxEnb}}$ and $\overline{\text{TxEnb}}$ active delay	Output	2ns	16ns	ns
U3	UTPB, SOC, Rxclav and Txclav setup time	Input	4ns		ns
U4	UTPB, SOC, Rxclav and Txclav hold time	Input	1ns		ns
U5	UTPB, SOC active delay (and PHREQ and PHSEL active delay in MPHY mode)	Output	2ns	16ns	ns

Figure 12-32 shows signal timings during UTOPIA receive operations.

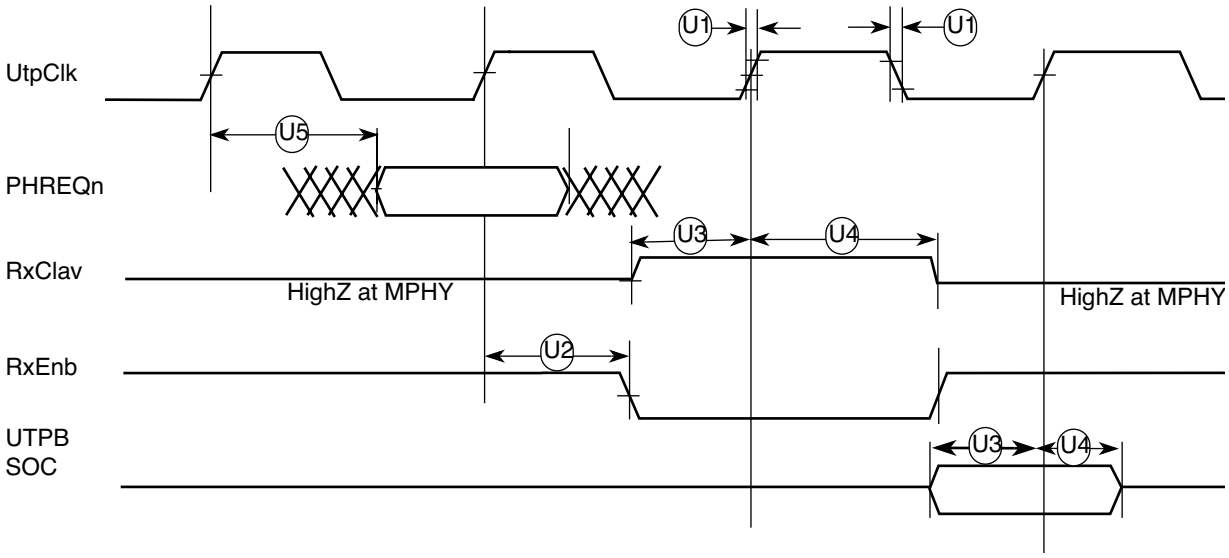


Figure 12-32. UTOPIA Receive Timing

Figure 12-33 shows signal timings during UTOPIA transmit operations.

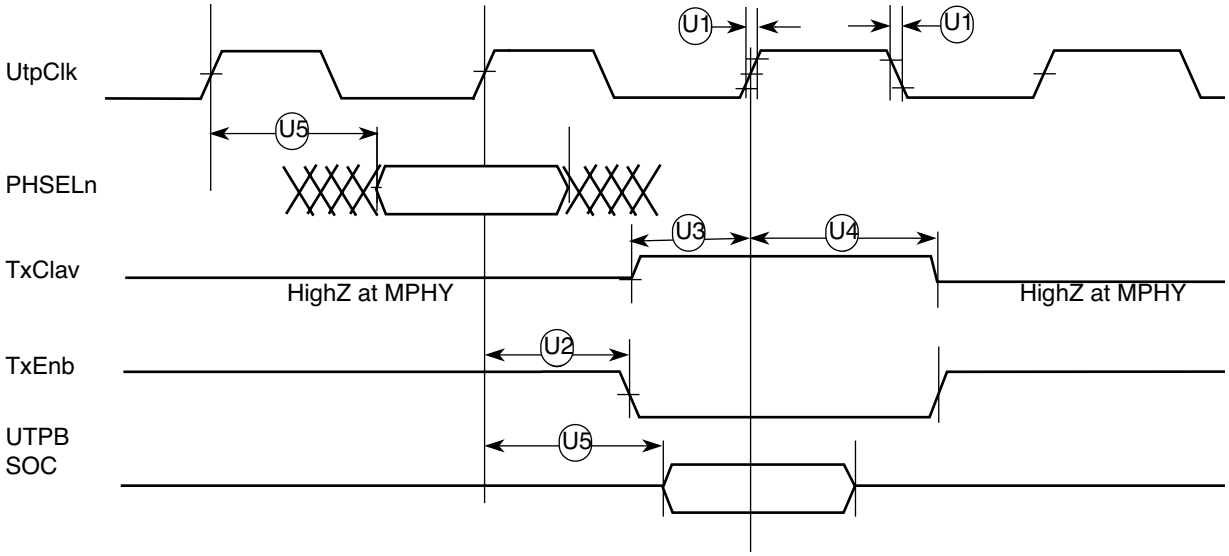


Figure 12-33. UTOPIA Transmit Timing

Part XIII FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

13.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

Table 13-1 provides information on the MII receive signal timing.

Table 13-1. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 13-1 shows MII receive signal timing.

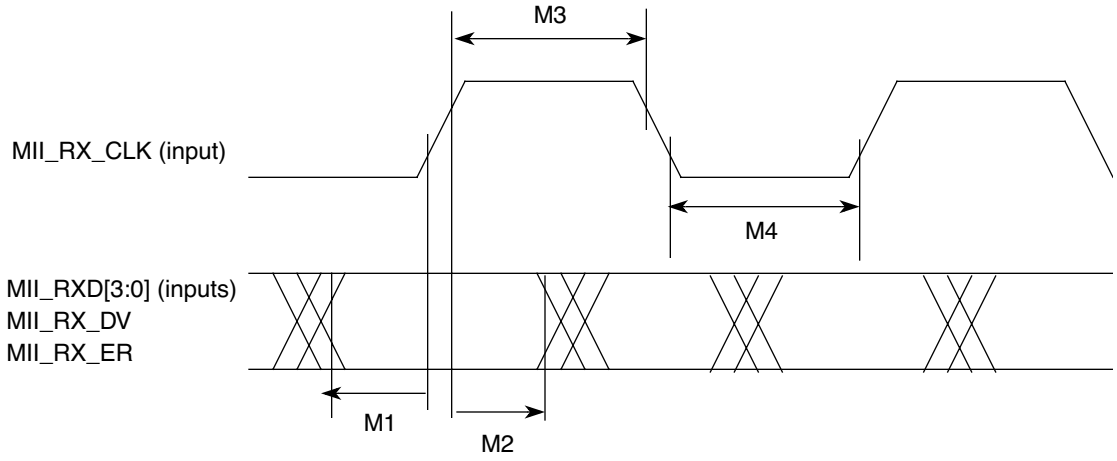


Figure 13-1. MII Receive Signal Timing Diagram

13.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 13-2 provides information on the MII transmit signal timing,.

Table 13-2. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 13-2 shows the MII transmit signal timing diagram.

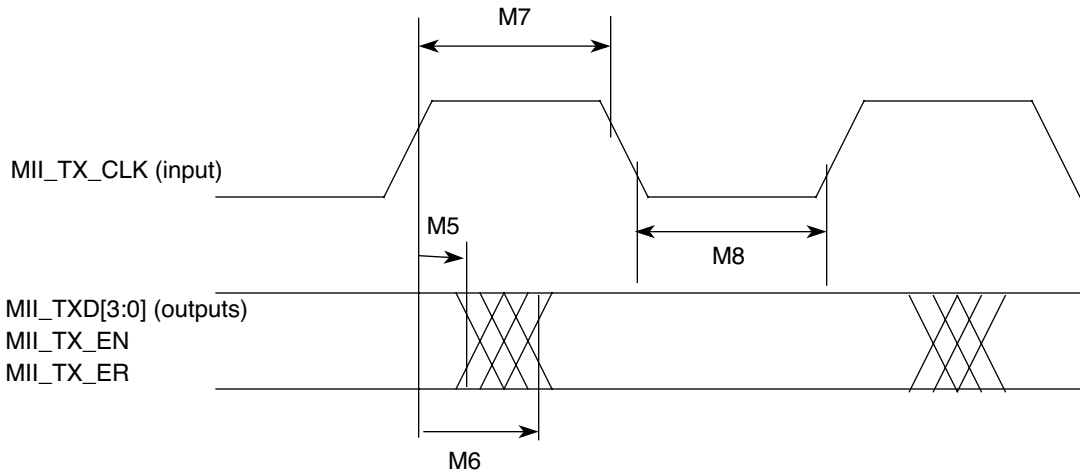


Figure 13-2. MII Transmit Signal Timing Diagram

13.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 13-3 provides information on the MII async inputs signal timing.

Table 13-3. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 13-3 shows the MII asynchronous inputs signal timing diagram.

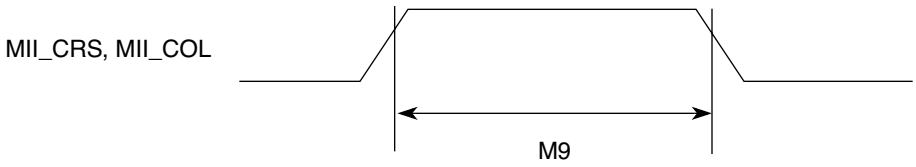


Figure 13-3. MII Async Inputs Timing Diagram

13.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 13-4 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 13-4. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 13-4 shows the MII serial management channel timing diagram.

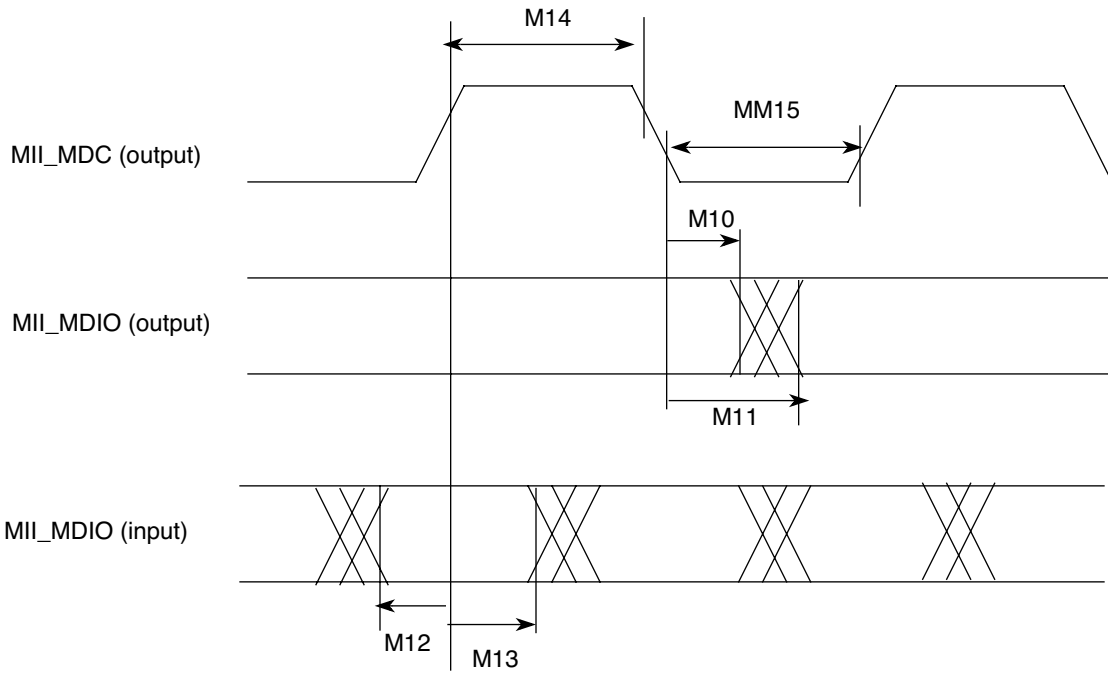


Figure 13-4. MII Serial Management Channel Timing Diagram

Part XIV Mechanical Data and Ordering Information

Table 14-1 provides information on the MPC862/857T/857DSL derivative devices.

Table 14-1. MPC862/857T/857DSL Derivatives

Device	Number of SCCs [1]	Ethernet Support	Multi-Channel HDLC Support	ATM Support	Cache Size	
					Instruction	Data
MPC862T	Four	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbyte
MPC862P	Four	10/100 Mbps	Yes	Yes	16 Kbyte	8 Kbyte
MPC857T	One (SCC1)	10/100 Mbps	Yes	Yes	4 Kbyte	4 Kbyte
MPC857DSL	One (SCC1)	10/100 Mbps	No	Up to 4 addresses	4 Kbyte	4 Kbyte

[1] Serial communications controller (SCC)

Table 14-2 identifies the packages and operating frequencies orderable for the MPC862/857T/857DSL derivative devices.

Table 14-2. MPC862/857T/857DSL Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (ZP suffix)	0°C to 95°C	50	XPC862PZP50B XPC862TZP50B XPC857TZP50B XPC857DSLZP50B
		66	XPC862PZP66B XPC862TZP66B XPC857TZP66B XPC857DSLZP66B
		80	XPC862PZP80B XPC862TZP80B XPC857TZP80B
		100	XPC862PZP100B XPC862TZP100B XPC857TZP100B
Plastic ball grid array (CZP suffix)	-40°C to 115°C	66 [1]	XPC862PCZP66B XPC857TCZP66B

[1] Additional extended temperature devices can be made available at 50MHz, 66MHz, and 80MHz

14.1 .Pin Assignments

Figure 14-1 shows the top view pinout of the PBGA package. For additional information, see the *MPC862 PowerQUICC Family User s Manual*.

NOTE: This is the top view of the device.

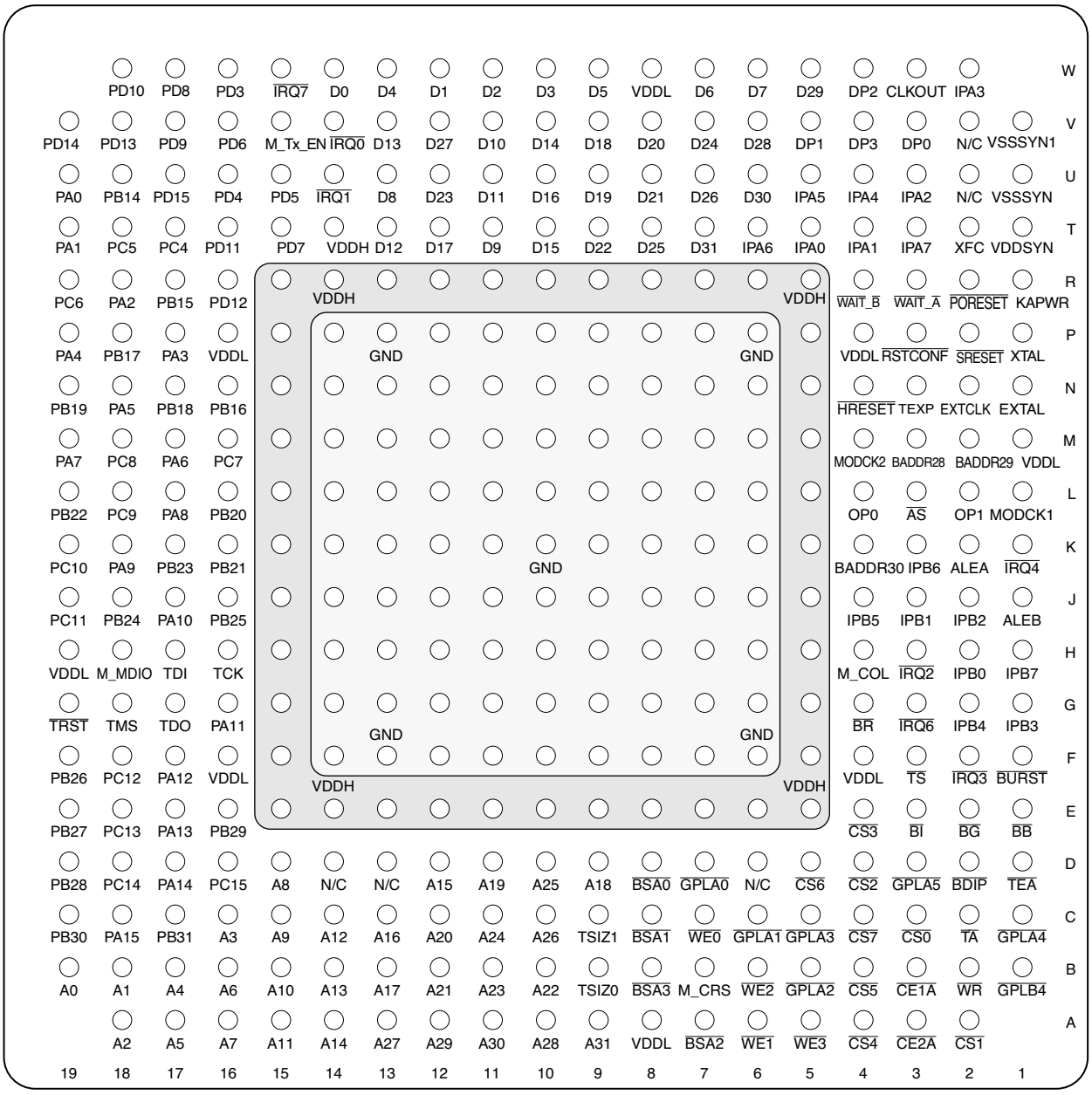


Figure 14-1. Pinout of the PBGA Package

Table 14-3 contains a list of the MPC862 input and output signals and shows multiplexing and pin assignments.

Table 14-3. Pin Assignments

Name	Pin Number	Type
A[0:31]	B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9	Bidirectional Three-state
TSIZ0 $\overline{\text{REG}}$	B9	Bidirectional Three-state
TSIZ1	C9	Bidirectional Three-state
RD/$\overline{\text{WR}}$	B2	Bidirectional Three-state
$\overline{\text{BURST}}$	F1	Bidirectional Three-state
$\overline{\text{BDIP}}$ $\overline{\text{GPL\_B5}}$	D2	Output
$\overline{\text{TS}}$	F3	Bidirectional Active Pull-up
$\overline{\text{TA}}$	C2	Bidirectional Active Pull-up
$\overline{\text{TEA}}$	D1	Open-drain
$\overline{\text{BI}}$	E3	Bidirectional Active Pull-up
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	H3	Bidirectional Three-state
$\overline{\text{IRQ4}}$ $\overline{\text{KR}}$ $\overline{\text{RETRY}}$ SPKROUT	K1	Bidirectional Three-state
$\overline{\text{CR}}$ $\overline{\text{IRQ3}}$	F2	Input
D[0:31]	W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7	Bidirectional Three-state
DP0 $\overline{\text{IRQ3}}$	V3	Bidirectional Three-state
DP1 $\overline{\text{IRQ4}}$	V5	Bidirectional Three-state
DP2 $\overline{\text{IRQ5}}$	W4	Bidirectional Three-state
DP3 $\overline{\text{IRQ6}}$	V4	Bidirectional Three-state
$\overline{\text{BR}}$	G4	Bidirectional
$\overline{\text{BG}}$	E2	Bidirectional

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
$\overline{BB}$	E1	Bidirectional Active Pull-up
FRZ $\overline{IRQ6}$	G3	Bidirectional
$\overline{IRQ0}$	V14	Input
$\overline{IRQ1}$	U14	Input
M_TX_CLK $\overline{IRQ7}$	W15	Input
$\overline{CS}$[0:5]	C3, A2, D4, E4, A4, B4	Output
$\overline{CS6}$ $\overline{CE1\_B}$	D5	Output
$\overline{CS7}$ $\overline{CE2\_B}$	C4	Output
$\overline{WE0}$ $\overline{BS\_B0}$ $\overline{IORD}$	C7	Output
$\overline{WE1}$ $\overline{BS\_B1}$ $\overline{IOWR}$	A6	Output
$\overline{WE2}$ $\overline{BS\_B2}$ $\overline{PCOE}$	B6	Output
$\overline{WE3}$ $\overline{BS\_B3}$ $\overline{PCWE}$	A5	Output
$\overline{BS\_A}$[0:3]	D8, C8, A7, B8	Output
$\overline{GPL\_A0}$ $\overline{GPL\_B0}$	D7	Output
$\overline{OE}$ $\overline{GPL\_A1}$ $\overline{GPL\_B1}$	C6	Output
$\overline{GPL\_A}$[2:3] $\overline{GPL\_B}$[2:3] $\overline{CS}$[2–3]	B5, C5	Output
UPWAITA $\overline{GPL\_A4}$	C1	Bidirectional
UPWAITB $\overline{GPL\_B4}$	B1	Bidirectional
$\overline{GPL\_A5}$	D3	Output
$\overline{PORESET}$	R2	Input
$\overline{RSTCONF}$	P3	Input

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
HRESET	N4	Open-drain
SRESET	P2	Open-drain
XTAL	P1	Analog Output
EXTAL	N1	Analog Input (3.3V only)
XFC	T2	Analog Input
CLKOUT	W3	Output
EXTCLK	N2	Input (3.3V only)
TEXP	N3	Output
ALE_A MII-TXD1	K2	Output
CE1_A MII-TXD2	B3	Output
CE2_A MII-TXD3	A3	Output
WAIT_A SOC_Split[2]	R3	Input
WAIT_B	R4	Input
IP_A0 UTPB_Split0[2] MII-RXD3	T5	Input
IP_A1 UTPB_Split1[2] MII-RXD2	T4	Input
IP_A2 IOIS16_A UTPB_Split2[2] MII-RXD1	U3	Input
IP_A3 UTPB_Split3[2] MII-RXD0	W2	Input
IP_A4 UTPB_Split4[2] MII-RXCLK	U4	Input
IP_A5 UTPB_Split5[2] MII-RXERR	U5	Input
IP_A6 UTPB_Split6[2] MII-TXERR	T6	Input

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
IP_A7 UTPB_Split7[2] MII-RXDV	T3	Input
ALE_B DSCK/AT1	J1	Bidirectional Three-state
IP_B[0:1] IWP[0:1] VFLS[0:1]	H2, J3	Bidirectional
IP_B2 IOIS16_B AT2	J2	Bidirectional Three-state
IP_B3 IWP2 VF2	G1	Bidirectional
IP_B4 LWP0 VF0	G2	Bidirectional
IP_B5 LWP1 VF1	J4	Bidirectional
IP_B6 DSDI AT0	K3	Bidirectional Three-state
IP_B7 PTR AT3	H1	Bidirectional Three-state
OP0 MII-TXD0 UtpClk_Split[2]	L4	Bidirectional
OP1	L2	Output
OP2 MODCK1 STS	L1	Bidirectional
OP3 MODCK2 DSDO	M4	Bidirectional
BADDR30 REG	K4	Output
BADDR[28:29]	M3, M2	Output
AS	L3	Input
PA15 RXD1 RXD4	C18	Bidirectional

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
PA14 TXD1 TXD4	D17	Bidirectional (Optional: Open-drain)
PA13 RXD2	E17	Bidirectional
PA12 TXD2	F17	Bidirectional (Optional: Open-drain)
PA11 L1TXDB RXD3	G16	Bidirectional (Optional: Open-drain)
PA10 L1RXDB TXD3	J17	Bidirectional (Optional: Open-drain)
PA9 L1TXDA RXD4	K18	Bidirectional (Optional: Open-drain)
PA8 L1RXDA TXD4	L17	Bidirectional (Optional: Open-drain)
PA7 CLK1 L1RCLKA BRGO1 TIN1	M19	Bidirectional
PA6 CLK2 $\overline{\text{TOUT1}}$	M17	Bidirectional
PA5 CLK3 L1TCLKA BRGO2 TIN2	N18	Bidirectional
PA4 CLK4 $\overline{\text{TOUT2}}$	P19	Bidirectional
PA3 CLK5 BRGO3 TIN3	P17	Bidirectional
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	R18	Bidirectional

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
PA1 CLK7 BRGO4 TIN4	T19	Bidirectional
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	U19	Bidirectional
PB31 $\overline{\text{SPISEL}}$ $\overline{\text{REJECT1}}$	C17	Bidirectional (Optional: Open-drain)
PB30 SPICLK $\overline{\text{RSTRT2}}$	C19	Bidirectional (Optional: Open-drain)
PB29 SPIMOSI	E16	Bidirectional (Optional: Open-drain)
PB28 SPIMISO BRGO4	D19	Bidirectional (Optional: Open-drain)
PB27 I2CSDA BRGO1	E19	Bidirectional (Optional: Open-drain)
PB26 I2CSCL BRGO2	F19	Bidirectional (Optional: Open-drain)
PB25 RXADDR3[2] SMTXD1	J16	Bidirectional (Optional: Open-drain)
PB24 TXADDR3[2] SMRXD1	J18	Bidirectional (Optional: Open-drain)
PB23 TXADDR2[2] $\overline{\text{SDACK1}}$ $\overline{\text{SMSYN1}}$	K17	Bidirectional (Optional: Open-drain)
PB22 TXADDR4[2] $\overline{\text{SDACK2}}$ $\overline{\text{SMSYN2}}$	L19	Bidirectional (Optional: Open-drain)
PB21 SMTXD2 L1CLKOB PHSEL1 [1] TXADDR1 [2]	K16	Bidirectional (Optional: Open-drain)

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
PB20 SMRXD2 L1CLKOA PHSEL0[1] TXADDR0[2]	L16	Bidirectional (Optional: Open-drain)
PB19 $\overline{\text{RTS1}}$ L1ST1	N19	Bidirectional (Optional: Open-drain)
PB18 RXADDR4[2] $\overline{\text{RTS2}}$ L1ST2	N17	Bidirectional (Optional: Open-drain)
PB17 $\overline{\text{L1RQb}}$ L1ST3 $\overline{\text{RTS3}}$ PHREQ1[1] RXADDR1[2]	P18	Bidirectional (Optional: Open-drain)
PB16 $\overline{\text{L1RQa}}$ L1ST4 $\overline{\text{RTS4}}$ PHREQ0[1] RXADDR0[2]	N16	Bidirectional (Optional: Open-drain)
PB15 BRGO3 TxClav	R17	Bidirectional
PB14 RXADDR2[2] $\overline{\text{RSTRT1}}$	U18	Bidirectional
PC15 $\overline{\text{DREQ0}}$ $\overline{\text{RTS1}}$ L1ST1 RxClav	D16	Bidirectional
PC14 $\overline{\text{DREQ1}}$ $\overline{\text{RTS2}}$ L1ST2	D18	Bidirectional
PC13 $\overline{\text{L1RQb}}$ L1ST3 RTS3	E18	Bidirectional
PC12 $\overline{\text{L1RQa}}$ L1ST4 RTS4	F18	Bidirectional

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
PC11 $\overline{\text{CTS1}}$	J19	Bidirectional
PC10 $\overline{\text{CD1}}$ $\overline{\text{TGATE1}}$	K19	Bidirectional
PC9 $\overline{\text{CTS2}}$	L18	Bidirectional
PC8 $\overline{\text{CD2}}$ $\overline{\text{TGATE2}}$	M18	Bidirectional
PC7 $\overline{\text{CTS3}}$ L1TSYNCB $\overline{\text{SDACK2}}$	M16	Bidirectional
PC6 $\overline{\text{CD3}}$ L1RSYNCB	R19	Bidirectional
PC5 $\overline{\text{CTS4}}$ L1TSYNCA SDACK1	T18	Bidirectional
PC4 $\overline{\text{CD4}}$ L1RSYNCA	T17	Bidirectional
PD15 L1TSYNCA MII-RXD3 UTPB0	U17	Bidirectional
PD14 L1RSYNCA MII-RXD2 UTPB1	V19	Bidirectional
PD13 L1TSYNCB MII-RXD1 UTPB2	V18	Bidirectional
PD12 L1RSYNCB MII-MDC UTPB3	R16	Bidirectional
PD11 RXD3 MII-TXERR $\overline{\text{RXENB}}$	T16	Bidirectional

Table 14-3. Pin Assignments (continued)

Name	Pin Number	Type
PD10 TXD3 MII-RXD0 $\overline{\text{TXENB}}$	W18	Bidirectional
PD9 RXD4 MII-TXD0 UTPCLK	V17	Bidirectional
PD8 TXD4 MII-MDC MII-RXCLK	W17	Bidirectional
PD7 $\overline{\text{RTS3}}$ MII-RXERR UTPB4	T15	Bidirectional
PD6 $\overline{\text{RTS4}}$ MII-RXDV UTPB5	V16	Bidirectional
PD5 $\overline{\text{REJECT2}}$ MII-TXD3 UTPB6	U15	Bidirectional
PD4 $\overline{\text{REJECT3}}$ MII-TXD2 UTPB7	U16	Bidirectional
PD3 $\overline{\text{REJECT4}}$ MII-TXD1 SOC	W16	Bidirectional
TMS	G18	Input
TDI DSDI	H17	Input
TCK DSCK	H16	Input
TRST	G19	Input
TDO DSDO	G17	Output
M_CRS	B7	Input
M_MDIO	H18	Bidirectional
M_TXEN	V15	Output
M_COL	H4	Input

Table 14-3. Pin Assignments (continued)

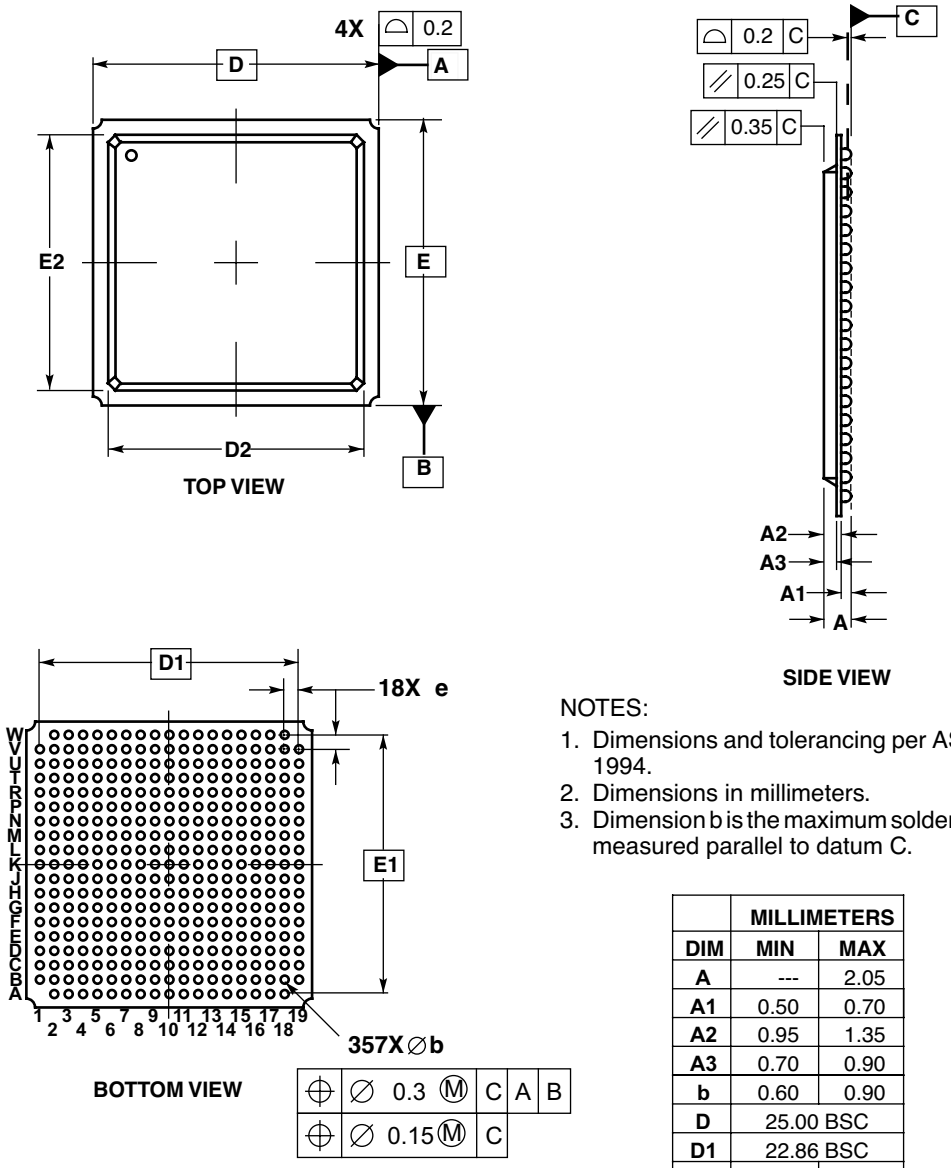
Name	Pin Number	Type
KAPWR	R1	Power
GND	F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14	Power
VDDL	A8, M1, W8, H19, F4, F16, P4, P16	Power
VDDH	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14	Power
N/C	D6, D13, D14, U2, V2	No-connect

[1] Classic SAR mode only

[2] ESAR mode only

14.2 Mechanical Dimensions of the PBGA Package

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Motorola sales office. Figure 14-2 shows the mechanical dimensions of the PBGA package.



NOTES:
1. Dimensions and tolerancing per ASME Y14.5M, 1994.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to datum C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

Case No. 1103-01

Figure 14-2. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

Part XV Document Revision History

Table 15-1 lists significant changes between revisions of this document.

Table 15-1. Document Revision History

Revision	Date	Substantive Changes
0	2001	Initial revision
0.1	9/2001	Change extended temperature from 95 to 105
0.2	11/2001	Revised for new template, changed Table 9-2 B23 max value @ 66Mhz from 2ns to 8ns
0.3	4/2002	Timing modified & equations added, for Rev A and B devices. Also modified power numbers and temperature ranges. Added ESAR UTOPIA timing.
1.0	9/2002	Specification changed to include the MPC857T and MPC857DSL. Changed maximum operating frequency from 80 MHz to 100 MHz. Removed MPC862DP, DT, and SR derivatives and part numbers. Corrected power dissipation numbers. Changed UTOPIA maximum frequency from 50 MHz to 33MHz. Changed part number ordering information to Rev B devices only. To maximum ratings for temperature, added frequency ranges.
1.1	5/2003	Change the SPI Master Timing Specs. 162 and 164

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