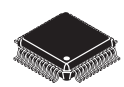
2.5V and 3.3V LVCMOS Clock Fanout Buffer

MPC9443

LOW VOLTAGE SUPPLY 2.5V AND 3.3V LVCMOS CLOCK FANOUT BUFFER



FA SUFFIX
48–LEAD LQFP PACKAGE
CASE 932–03

The MPC9443 is a 2.5V and 3.3V compatible 1:16 clock distribution buffer designed for low-voltage high-performance telecom, networking and computing applications. The device supports 3.3V, 2.5V and dual supply voltage (mixed-voltage) applications. The MPC9443 offers 16 low-skew outputs which are divided into 4 individually configurable banks. Each output bank can be individually supplied by 2.5V or 3.3V, individually set to run at 1X or 1/2X of the input clock frequency or be disabled (logic low output state). Two selectable LVPECL compatible inputs support differential clock distribution systems. In addition, one selectable LVCMOS input is provided for LVCMOS clock distribution systems. The MPC9443 is specified for the extended temperature range of –40 to +85°C.

Features

- Configurable 16 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Output clock frequency up to 350 MHz
- Designed for high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Max. output skew of 250 ps (125 ps within one bank)
- Selectable output configurations per output bank
- Individually per-bank high–impedance tristate
- Output disable (stop in logic low state) control
- 48 ld LQFP package
- Ambient operating temperature range of –40 to 85°C

Functional Description

The MPC9443 is a full static design supporting clock frequencies up to 350 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the four output banks.

Two independent LVPECL compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9443 supports single-ended LVCMOS clock distribution systems. Each of the four output banks can be individually supplied by 2.5V or 3.3V, supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each output bank. The MPC9443 output banks are in high–impedance state by deasserting the OE_N pins. Asserting OE_N will the enable output banks. Please see the Output High–Impedance Control table on page 4 for details. The outputs can be synchronously stopped (logic low state). The outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9443 outputs can drive one or two traces giving the devices an effective fanout of 1:32 at V_{CC} = 3.3V. The device is packaged in a 7x7 mm^2 48-lead LQFP package.

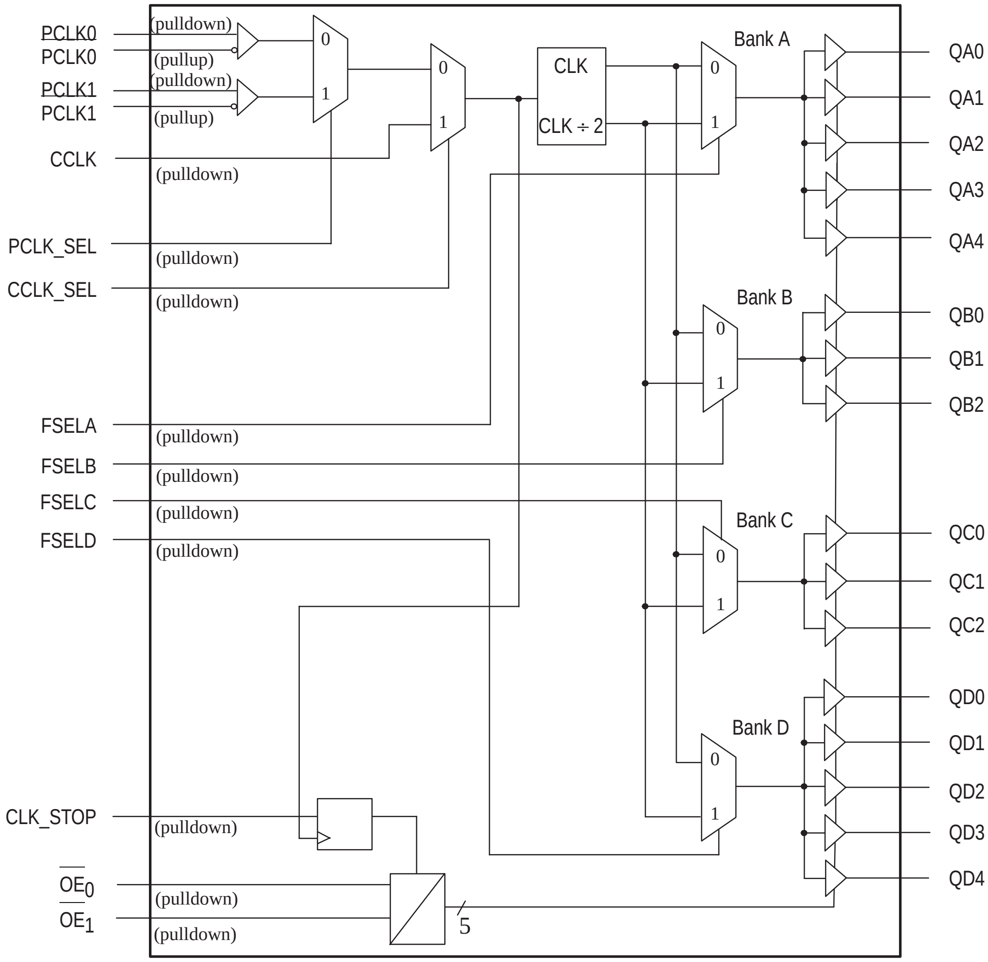


Figure 1. MPC9443 Logic Diagram

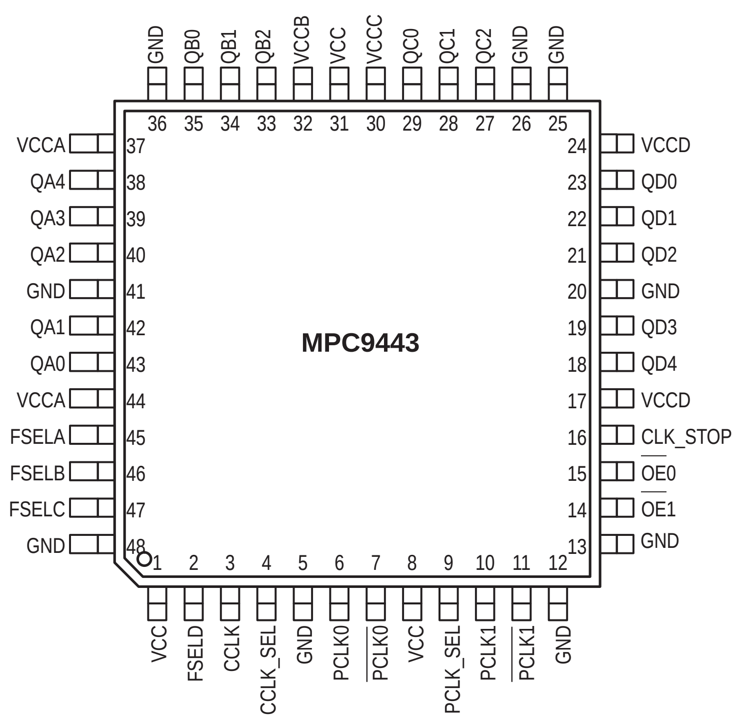


Figure 2. 48–Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	LVCMOS clock inputs
PCLK0, $\overline{PCLK0}$	Input	LVCMOS	LVPECL differential clock input
PCLK1, $\overline{PCLK1}$	Input	LVCMOS	LVPECL differential clock input
$FSEL_A$, $FSEL_B$, $FSEL_C$, $FSEL_D$	Input	LVCMOS	Output bank divide select input
CCLK_SEL	Input	LVCMOS	LVCMOS/LVPECL clock input select
PCLK_SEL	Input	LVCMOS	PCLK0/PCLK1 clock input select
$\overline{OE}_0$, $\overline{OE}_1$	Input	LVCMOS	Output tristate control
CLK_STOP	Input	LVCMOS	Synchronous output enable/disable (clock stop) control
GND		Supply	Negative voltage supply
V_{CCA}, V_{CCB}, V_{CCC}, V_{CCD}		Supply	Positive voltage supply output bank (VCC)
V_{CC}		Supply	Positive voltage supply core (VCC)
QA0 to QA4	Output	LVCMOS	Bank A outputs
QB0 to QB2	Output	LVCMOS	Bank B outputs
QC0 to QC2	Output	LVCMOS	Bank C outputs
QD0 to QD4	Output	LVCMOS	Bank D outputs

Table 2: Supported Single and Dual Supply Configurations

Supply voltage configuration	V_{CC}[a]	V_{CCA}[b]	V_{CCB}[c]	V_{CCC}[d]	V_{CCD}[e]	GND
3.3V supply	3.3V	3.3V	3.3V	3.3V	3.3V	0 V
Mixed mode supply	3.3V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V	0 V
2.5V supply	2.5V	2.5V	2.5V	2.5V	2.5V	0 V

a. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels
b. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels
c. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels
d. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels
e. V_{CCD} is the positive power supply of the bank D outputs. V_{CCD} voltage defines bank D output levels

Table 3: Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	PCLK or PCLK1 active (LVPECL clock mode)	CCLK active (LVCMOS clock mode)
PCLK_SEL	0	PCLK0 active, PCLK1 inactive	PCLK1 active, PCLK0 inactive
$FSEL_A$	0	$f_{QA0:4} = f_{REF}$	$f_{QA0:4} = f_{REF} \div 2$
$FSEL_B$	0	$f_{QB0:2} = f_{REF}$	$f_{QB0:2} = f_{REF} \div 2$
$FSEL_C$	0	$f_{QC0:2} = f_{REF}$	$f_{QC0:2} = f_{REF} \div 2$
$FSEL_D$	0	$f_{QD0:4} = f_{REF}$	$f_{QD0:4} = f_{REF} \div 2$
CLK_STOP	0	Normal operation	Outputs are synchronously disabled (stopped) in logic low state
$\overline{OE}_0$, $\overline{OE}_1$	00	Asynchronous output enable control. See Table 4. $\overline{OE}_N$	

Table 4: Output High–Impedance Control ($\overline{OE_N}$)[a]

$\overline{OE_0}$	$\overline{OE_1}$	QA0 to QA4	QB0 to QB2	QC0 to QC2	QD0 to QD4	Total number of enabled outputs
0	0	Enabled	Enabled	Enabled	Enabled	16
0	1	Enabled	Disabled (tristate)	Disabled (tristate)	Enabled	10
1	0	Enabled	Enabled	Disabled (tristate)	Disabled (tristate)	8
1	1	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	0

a. $\overline{OE_N}$ will tristate (high impedance) output banks independent on the logic state of the output and the status of CLK_STOP.

Table 5: Absolute Maximum Ratings[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 6: General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} \div 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	

Table 7: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD}$ = 3.3V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		-0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-peak Input Voltage	PCLK0, 1	250			mV	LVPECL
V_{CMR}[a]	Common Mode Range	PCLK0, 1	1.1		V_{CC}-0.6	V	LVPECL
I_{IN}	Input Current[b]				200	µA	V_{IN}=GND or V_{IN}=VCC
V_{OH}	Output High Voltage		2.4			V	I_{OH}=-24 mA[c]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL}= 24mA[c] I_{OL}= 12mA
Z_{OUT}	Output Impedance			19		Ω	
I_{CCQ}[d]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
b. Input pull-up / pull-down resistors influence input current.
c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for VCC=3.3V) or one 50Ω series terminated transmission line (for VCC=2.5V).
d. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD}$ = 3.3V ± 5%, T_A = –40 to +85°C)[a]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		350 175	MHz MHz	FSELx=0 FSELx=1
V_{PP}	Peak-to-peak Input Voltage	PCLK0,1	500		1000	mV	LVPECL
V_{CMR}[b]	Common Mode Range	PCLK0,1	1.3		V_{CC}-0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[c]	ns	0.8 to 2.0V
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Propagation Delay	PCLK0,1 to any Q PCLK0,1 to any Q CCLK to any Q CCLK to any Q	2.5 2.4 2.1 1.9		5.0 5.2 4.2 4.6	ns ns ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
t_S, t_H	Setup, hold time (reference clock to CLK_STOP)		500			ps	
$t_{sk(LH, HL)}$	Output-to-output Skew[d]	Within one bank Any output, same output divider Any output, any output divider			125 225 250	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew (LH)[e] Device-to-device Skew (LH, HL)[f]	Using PCLK0,1 Using CCLK Using PCLK0,1 Using CCLK			2.5 2.1 2.8 2.7	ns ns ns ns	
$t_{SK(P)}$ DC_Q	Output pulse skew[g] Output Duty Cycle	Using PCLK0,1 Using CCLK f_Q<140 MHz and using CCLK f_Q<250 MHz and using PCLK0,1	 45 45	 50 50	300 400 55 55	ps ps % %	DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
d. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
e. Device-to-device skew referenced to the rising output edge.
f. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
g. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH} - t_{pHL} |.

Table 9: DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD}$ = 2.5V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		-0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak Input Voltage	PCLK0,1	250			mV	LVPECL
V_{CMR}[a]	Common Mode Range	PCLK0,1	1.1		V_{CC}-0.7	V	LVPECL
I_{IN}	Input Current[b]				200	μA	V_{IN}=GND or V_{IN}=VCC
V_{OH}	Output High Voltage		1.8			V	I_{OH}= -15 mA[c]
V_{OL}	Output Low Voltage				0.6	V	I_{OL}= 15 mA[c]
Z_{OUT}	Output Impedance			22		Ω	
I_{CCQ}[d]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
b. Input pull-up / pull-down resistors influence input current.
c. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives one 50Ω series terminated transmission lines at VCC=2.5V.
d. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 10: AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD}$ = 2.5 ± 5%, T_A = –40 to +85°C)[a]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		350 175	MHz MHz	FSELx=0 FSELx=1
V_{PP}	Peak-to-peak input voltage	PCLK0,1	500		1000	mV	LVPECL
V_{CMR}[b]	Common Mode Range	PCLK0,1	1.1		V_{CC}-0.7	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[c]	ns	0.8 to 2.0V
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Propagation delay	PCLK0,1 to any Q PCLK0,1 to any Q CCLK to any Q CCLK to any Q	2.8 2.7 2.2 2.1		6.0 6.2 5.3 5.5	ns ns ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
t_S, t_H	Setup, hold time (reference clock to CLK_STOP)		500			ps	
$t_{sk(LH, HL)}$	Output-to-output Skew[d]	Within one bank Any output, same output divider Any output, any output divider			125 225 250	ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew (LH)[e] Device-to-device Skew (LH, HL)[f]	Using PCLK0,1 Using CCLK Using PCLK0,1 Using CCLK			3.2 3.1 3.5 3.4	ns ns ns ns	
$t_{SK(p)}$	Output pulse skew[g]	Using PCLK0,1 Using CCLK			300 400	ps ps	DC_{REF} = 50%
DC_Q	Output Duty Cycle	f_Q<140 MHz and using CCLK f_Q<250 MHz and using PCLK0,1	45 45	50 50	55 55	% %	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
c. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
d. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
e. Device-to-device skew referenced to the rising output edge.
f. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
g. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH} - t_{pHL} |.

Table 11: DC Characteristics

(V_{CC} = 3.3V ± 5%, any $V_{CCA,B,C,D}$ = 2.5V ± 5% or 3.3V ± 5% (mixed), T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage		-0.3		0.8	V	LVCMOS
I_{IN}	Input current[a]				200	µA	
V_{OH}	Output High Voltage	2.5V output 3.3V output	1.7 2.0			V	I_{OH}= -15 mA[b] I_{OH}= -24 mA[b]
V_{OL}	Output Low Voltage	2.5V output 3.3V output			0.6 0.55	V	I_{OL}= 15 mA[b] I_{OL}= 24 mA[b]
V_{PP}	Peak-to-peak input voltage	PCLK0,1	250			mV	LVPECL
V_{CMR}[c]	Common Mode Range	PCLK0,1	1.1		V_{CC}-0.6	V	LVPECL
Z_{OUT}	Output impedance	2.5V output 3.3V output		22 19		Ω Ω	
C_{PD}	Power Dissipation Capacitance			10		pF	Per Output
I_{CCQ}[d]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

a. Input pull-up / pull-down resistors influence input current.
b. The MPC9443 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for VCC=3.3V) or one 50Ω series terminated transmission line (for VCC=2.5V).
c. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
d. ICCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 12: AC Characteristics

(V_{CC} = 3.3V ± 5%, any $V_{CCA,B,C,D}$ = 2.5V ± 5% or 3.3V ± 5% (mixed), T_A = –40 to +85°C)[a b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(LH, HL)}$	Output-to-output Skew[c]	Any output, same output divider Any output, any output divider			275 350	ps ps	
$t_{sk(PP)}$	Device-to-device Skew		See 3.3V AC table				
$t_{PLH, HL}$	Propogation Delay		See 3.3V AC table				
$t_{SK(P)}$	Output pulse skew[d]	Using PCLK0,1 Using CCLK			400 500	ps ps	DC_{REF} = 50%
DC_Q	Output Duty Cycle	f_Q<140 MHz and using CCLK f_Q<250 MHz and using PCLK0,1	45 45	50 50	55 55	% %	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b. This table only specifies AC parameter im mixed voltage supply conditions that vary from the corresponding AC tables. All other parameters, see the 3.3V (for 3.3V outputs) or 2.5V AC table (for 2.5V outputs).
c. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
d. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH} - t_{pHL} |.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9443 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines at V_{CC} = 3.3V. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9443 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9443 clock driver is effectively doubled due to its capability to drive multiple lines (at V_{CC} = 3.3V).

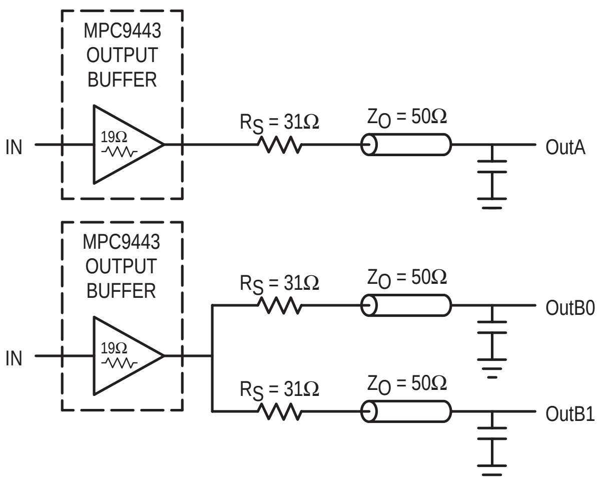


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9443 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9443. The output waveform in Figure 4. "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 31Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 31\Omega \parallel 31\Omega$$
$$R_0 = 19\Omega$$
$$V_L = 3.0 (25 \div (15.5+19+25)$$
$$= 1.26V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.52V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

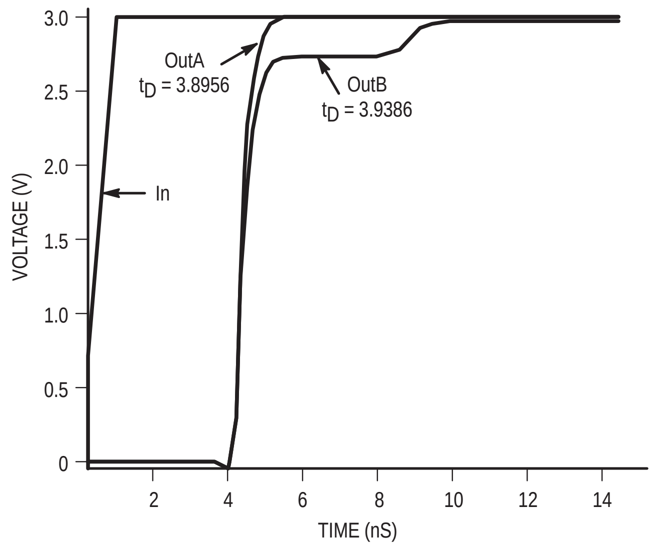
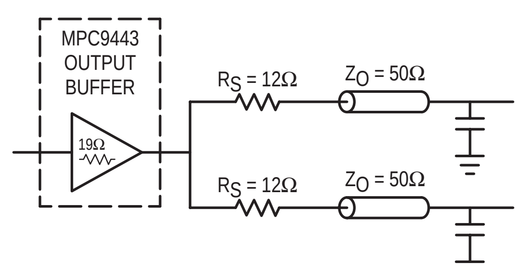


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5. "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$19\Omega + 12\Omega \parallel 12\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 5. Optimized Dual Line Termination

Power Consumption of the MPC9443 and Thermal Management

The MPC9443 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9443 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperture, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9443 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 13: Die junction temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9443 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9443 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC9443, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 16 in case of the MPC9443). The MPC9443 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cyle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 13, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC9443 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 13. R_{thja} can be derived from Table 14. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 14: Thermal package impedance of the 48ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W	R_{thja} (2P2S board), K/W
Still air	69	53
100 lfpm		
200 lfpm	64	50
300 lfpm		
400 lfpm		
500 lfpm		

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9443. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{J,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

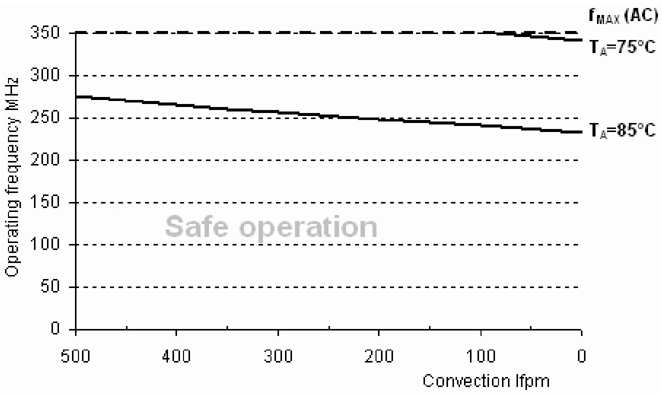


Figure 6. Maximum MPC9443 frequency, V_{CC} = 3.3V, MTBF 9.1 years, driving series terminated transmission lines

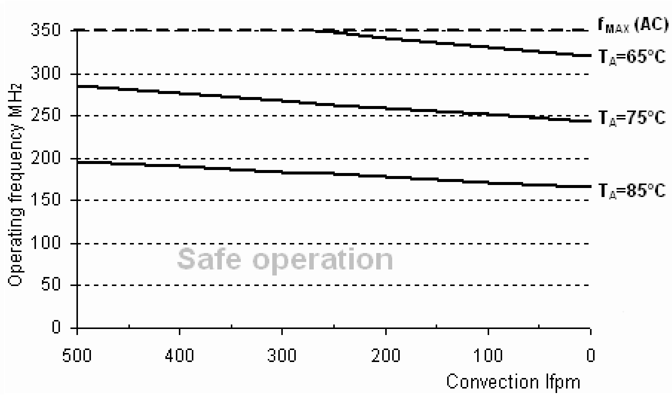


Figure 7. Maximum MPC9443 frequency, V_{CC} = 3.3V, MTBF 9.1 years, 4 pF load per line

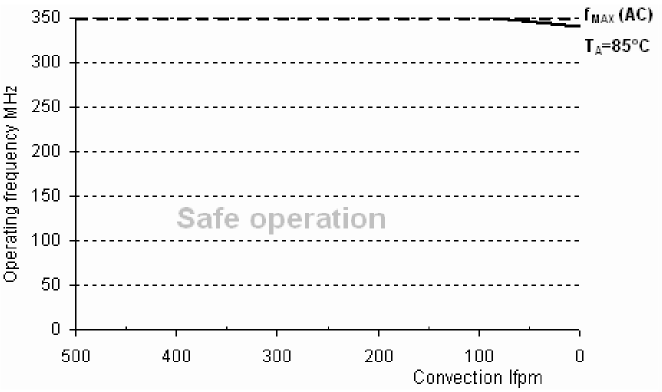


Figure 8. Maximum MPC9443 frequency, V_{CC} = 3.3V, MTBF 4 years, driving series terminated transmission lines

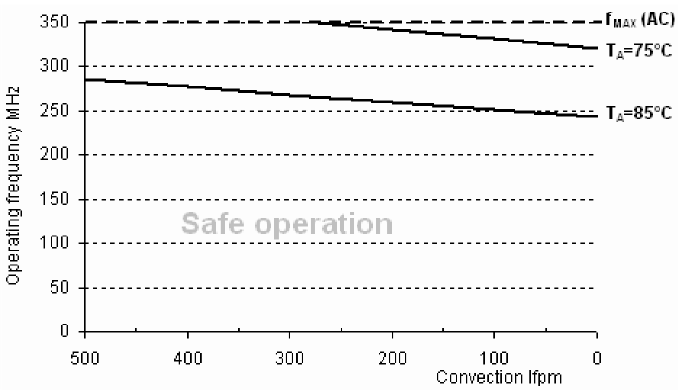


Figure 9. Maximum MPC9443 frequency, V_{CC} = 3.3V, MTBF 4 years, 4 pF load per line

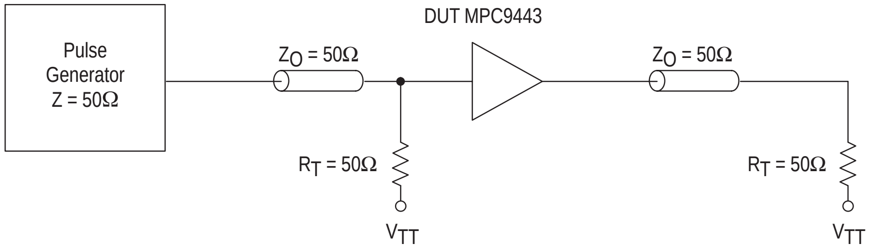


Figure 10. CCLK MPC9443 AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V

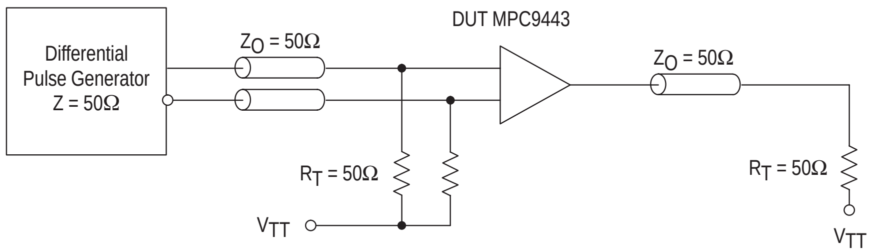


Figure 11. PCLK MPC9443 AC test reference

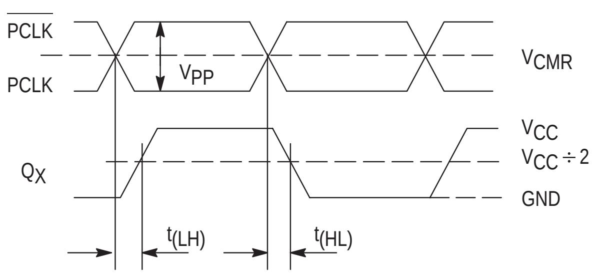


Figure 12. Propagation delay (t_{PD}) test reference

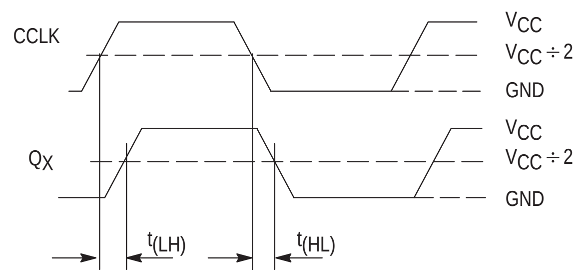
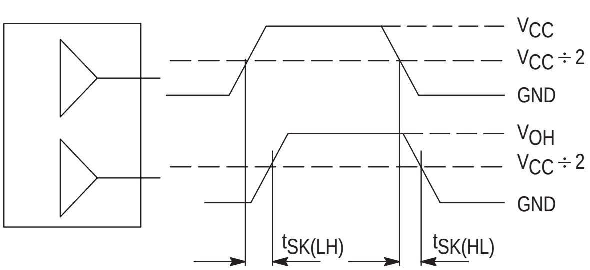
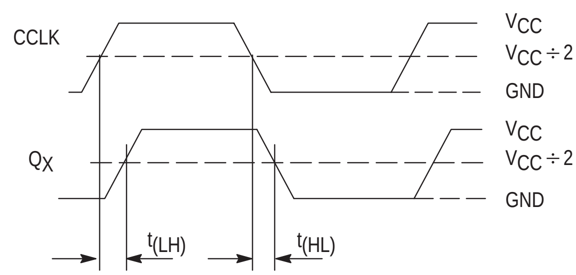


Figure 13. Propagation delay (t_{PD}) test reference



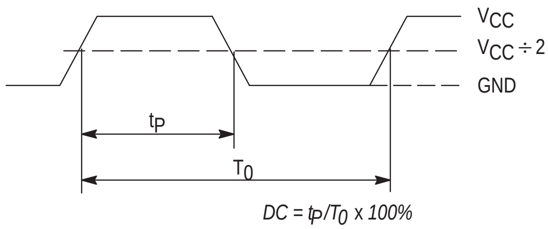
The pin–to–pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device

Figure 14. Output–to–output Skew $t_{SK(LH, HL)}$



$t_{SK(P)} = | t_{PLH} - t_{PHL} |$

Figure 15. Output Pulse Skew $t_{SK(P)}$ test reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)

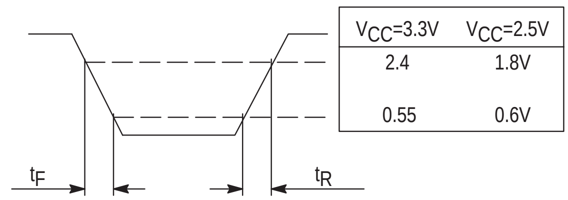
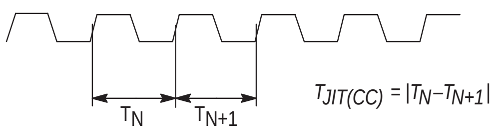


Figure 17. Output Transition Time test reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle–to–cycle Jitter

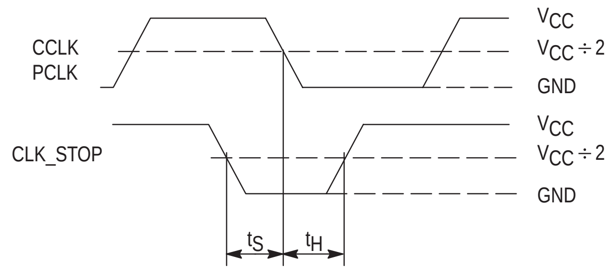
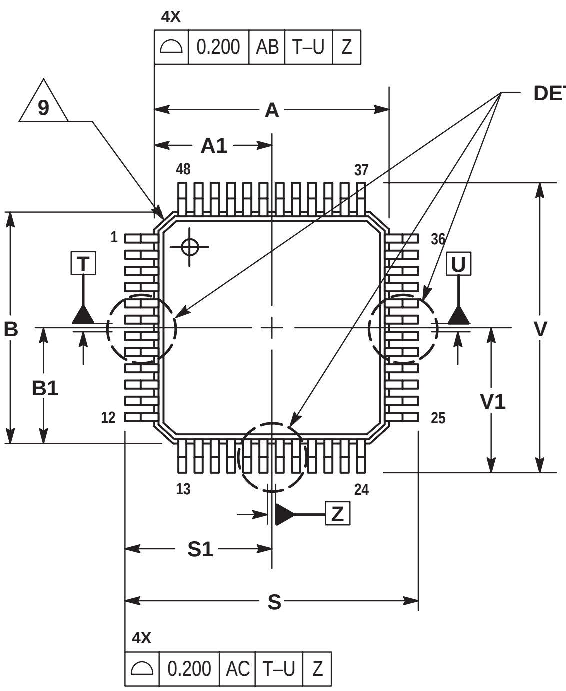
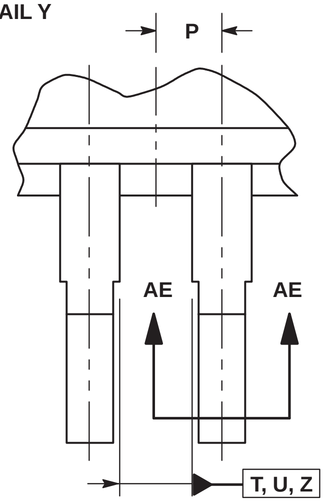


Figure 19. Setup and hold time (t_S, t_H) test reference

OUTLINE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 932-03
ISSUE F

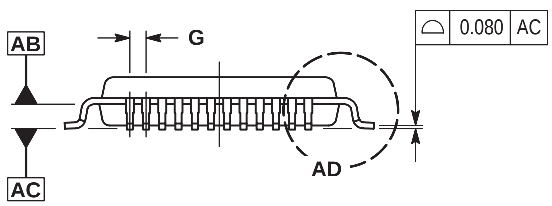


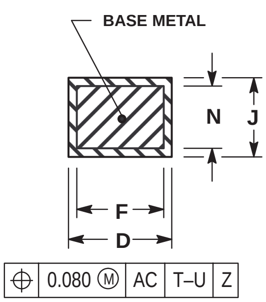


DETAIL Y

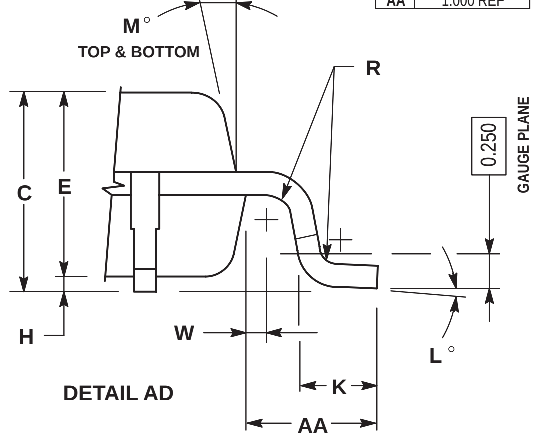
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12 °REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





SECTION AE–AE



DETAIL AD

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