- **Source Driver LSI for Active-Matrix LCDs**
- **Compatible With Dot Reverse Driving and Source Line Reverse Driving**
- **No Precharging**
- **Liquid Crystal Drive Outputs: 384**
- **Fine Pitch/TCP**
- **Driver With Internal 8-Bit Digital Input DAC (16.77 Million Colors)**
- **Maximum Operating Clock Frequencies: 55 MHz (Logic Section Power Supply Voltage: 2.5 V – 3.6 V)**
- **Dual-Port Input**
- **Allows for Input Data Reversing**
- **Gamma Correction: 7+7 or 8+8 is Selectable as a TCP Option**
- **No Need for an External Reference Voltage Generation Circuit (or for Ramp Voltage or a Multi-Value Power Supply)**
- **Low-Power Consumption Is Achieved by Automatically Stopping the Clock After a Fixed Amount of Data has Been Captured**
- **Lower System Power Consumption Can Be Accomplished Using the Low-Power Mode**
- **Can Handle Heavy Loads Using the LCD Capacity Switching Mode**
- **Logic Section Power Supply Voltage: 2.5 V – 3.6 V**
- **Liquid Crystal Drive Section Power Supply Voltage: 13.5 V Maximum**

description

The MPT57571 is a source driver LSI that drives an active-matrix LCD panel, as well as a 256-gradation driver that implements multi-pin configuration and reduced power consumption.

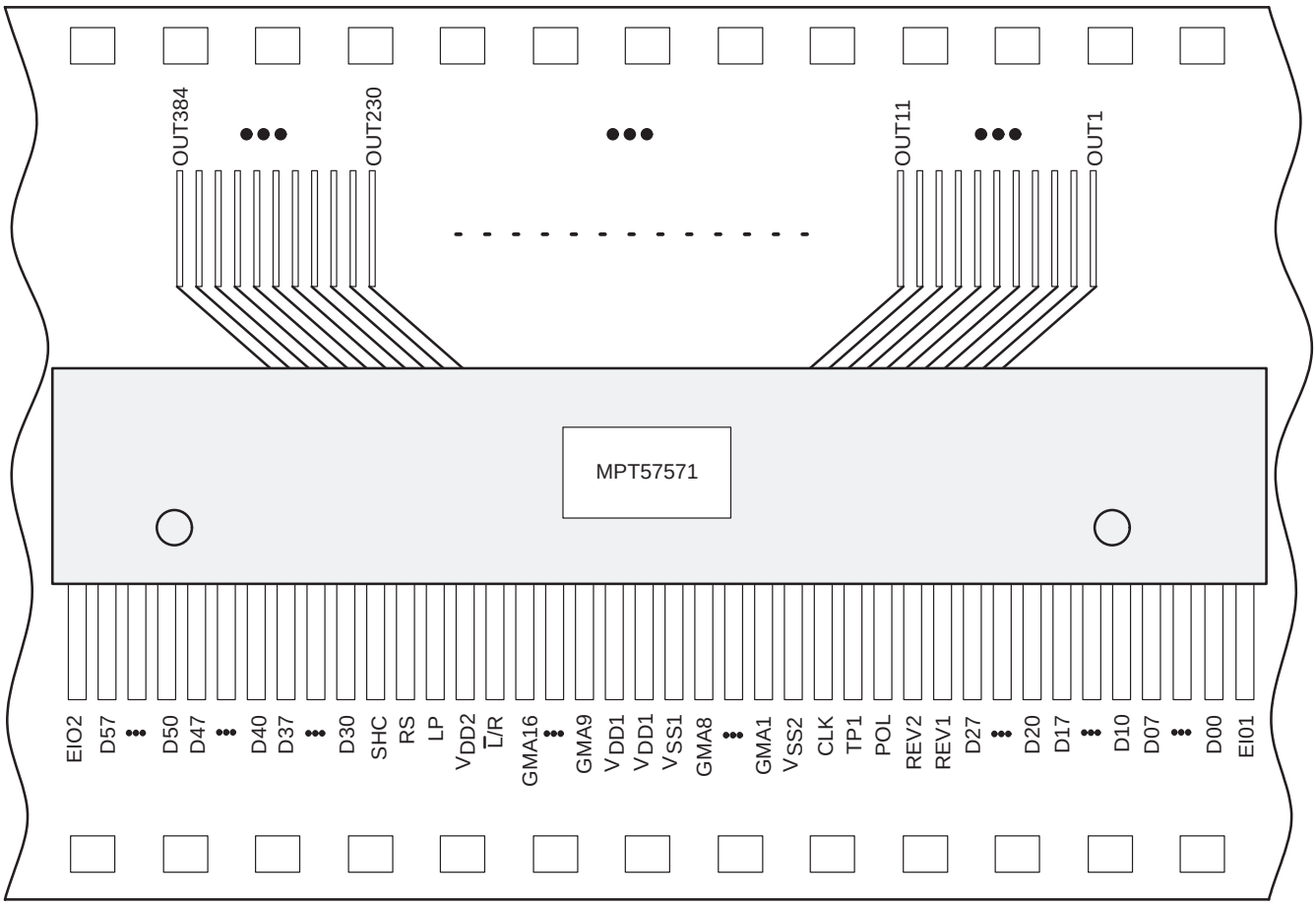
The MPT57571 has 384 panel-drive outputs. Because it is expandable, the MPT57571 is used in multiple applications, the screen can be enlarged, and the L/R (shift-direction switching) terminals simplify LCD panel interconnection.

The device has a large output dynamic range (13.1 V_{PP}) that makes the reverse driving of opposing electrodes in the LCD panel unnecessary. This reduces system power consumption and produces a high-quality picture. The device is also compatible with single-sided mounting, dot reverse driving, and source line reverse driving.

The MPT57571s 384 outputs ensure XGA/VGA compatibility, making it useful in a wider range of applications.

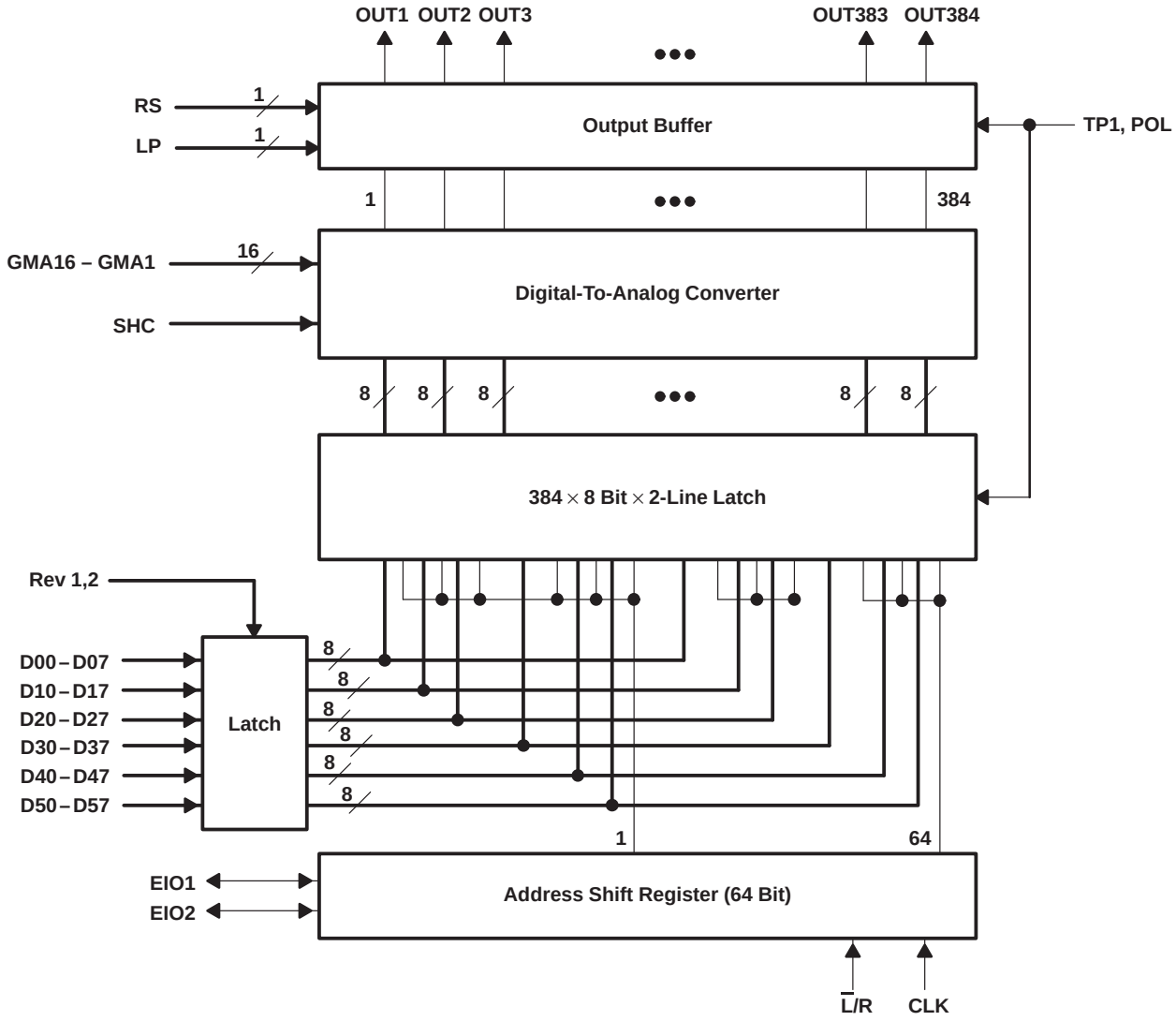
The maximum operating clock frequency of the MPT57571 is 55 MHz when the power supply voltage for the logic section is between 2.5 V and 3.6 V and the single-side driving of an LCD panel has been implemented.

tab package



NOTES: A. This figure shows the copper foil side. The TAB outline is not described.
B. There are 80 input terminals and 384 output terminals.

functional block diagram



Terminal Functions

<table>
<tr><th colspan="2">TERMINAL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><th>NAME</th><th>FUNCTION</th><th></th><th></th></tr>
<tr><td>D00 – D07
D10 – D17
D20 – D27</td><td>Port 1
Image signal input terminal</td><td>I</td><td rowspan="2">Image signal input terminal
Inputs image signals with a 48-bit width: 8-bit gradation data x 6 dots (for 2 pixels).
Dn0: LSB, Dn7: MSB</td></tr>
<tr><td>D30 – D37
D40 – D47
D50 – D57</td><td>Port 2
Image signal input terminal</td><td>I</td></tr>
<tr><td>EIO1
EIO2</td><td>Start pulse I/O terminal</td><td>I/O</td><td>Internal shift register’s start pulse I/O terminal
<table>
<tr><th></th><th>$\overline{L}$/R = H</th><th>$\overline{L}$/R =L</th></tr>
<tr><td>EIO1</td><td>Right-shift input</td><td>Left-shift output</td></tr>
<tr><td>EIO2</td><td>Right-shift output</td><td>Left-shift input</td></tr>
</table></td></tr>
<tr><td>$\overline{L}$/R</td><td>Shift direction selection signal input terminal</td><td>I</td><td>Shift direction selection signal
Right shift (OUT1 → OUT 384): H
Left shift (OUT384 → OUT1): L</td></tr>
<tr><td>CLK</td><td>Shift clock input terminal</td><td>I</td><td>Shift register transfer clock input terminal. CLK writes the display data to the data register at the leading edge.</td></tr>
<tr><td>V_{DD1} (*1)
V_{DD1} (*2)
V_{SS1}</td><td>Analog power supply</td><td>I</td><td>Power supply for analog circuits
V_{DD1} (*1) is used as the analog circuit reference potential
Stable electric potential must be supplied.
V_{DD1} (*2) is used for output circuits, etc.</td></tr>
<tr><td>V_{DD2},
V_{SS2}</td><td>Digital power supply</td><td>I</td><td>Power supply for digital circuits</td></tr>
<tr><td>GMA1...GMA16</td><td>Gamma correction reference potential input terminal</td><td>I</td><td>Potential input terminal for gamma correction
Reference potential should be maintained when outputting the gradation voltage.
See recommended operating conditions for potential-related information.
7+7 GMA input is possible by processing GMA11 and GMA6 in the TCP option.</td></tr>
<tr><td>TP1</td><td>Latch input terminal</td><td>I</td><td>Latches the data register contents with the leading edge, transfers it to the D/A converter, and outputs the gradation voltage with the trailing edge.</td></tr>
<tr><td>POL</td><td>Polarity reversal terminal</td><td>I</td><td>POL = L: odd-numbered outputs GMA1-GMA8 and even-numbered outputs GMA9-GMA16 are reference power supplies.
POL = H: odd-numbered outputs GMA9-GMA16 and even-numbered outputs GMA1-GMA8 are reference power supplies.</td></tr>
<tr><td>REV1
REV2</td><td>Input data reversal terminal</td><td>I</td><td>Selects reversal/nonreversal of input data:
REV1: controls reversal/nonreversal of port 1.
REV1: controls reversal/nonreversal of port 2.
REV1,2 = H: reversal
REV1,2 = L: nonreversal
This terminal can be processed within TCP.
H and L are identified at the leading edge of each CLK, like the data (Dxx).</td></tr>
<tr><td>OUT1 – OUT384</td><td>LCD control output terminal</td><td>O</td><td>Subpixel output. OUT1–OUT384 provides 256 gray-scale signals to the LCD panel.</td></tr>
<tr><td>SHC</td><td>Output circuit control signal input terminal</td><td>I</td><td>Signal used for output circuit control.</td></tr>
<tr><td>RS</td><td>LCD drive capacity switching terminal</td><td>I</td><td>Switched LCD drive capacity:
RS = H: heavy-load mode
RS = L: spec-load mode</td></tr>
<tr><td>LP</td><td>Low-power mode selection terminal</td><td>I</td><td>Reduces charge and discharge current to a load:
LP = H: low-power mode
LP = L: normal mode
See application Information for details.</td></tr>
</table>

detailed description

image signal capture

EIOn = H (n = 1 or n = 2) is captured internally at the leading edge of CLK. After the decay of EIOn, the image signal data are captured in the internal latch with the rise of the next CLK.

After all data (that is, 384 channels of data) have been captured, the device automatically switches to the standby state. New data are not captured until EIOn receives another input, even if there is a CLK input. If EIOn receives an input in the meantime, new image signal data is captured at the rise of the next CLK after EIOn decays.

It is possible to reverse the input data for each port by means of the REV1 and REV2 signals.

output expansion

The number of image signal output terminals can be expanded by cascading these devices, thereby enabling compatibility with large screens. Expansion is controlled by using the $\overline{L}$/R terminal:

$\overline{L}$/R = L: the previous-stage EIO1 terminal is connected to the next-stage EIO2, and input terminals other than EIO1 and EIO2 are connected together on each device.

$\overline{L}$/R = H: the previous-stage EIO2 terminal is connected to the next-stage EIO1, and input terminals other than EIO1 and EIO2 are connected together on each device.

relationship between input data values and output voltage

The output voltage is determined by the input data value and the 16 gamma-correction potentials (GMA[1-16]). Also, since the output voltage is compatible with dot-reverse driving, it is possible to output gradation voltages for the opposing-electrode voltages with polarities that differ for even and odd-numbered outputs.

Input potentials with the same polarity relative to the opposing-electrode voltages should be applied for GMA1-8 and GMA9-16 of the gamma-correction reference power supply.

Reference potential inputs for correction (GMA[1-16]) should be applied externally as desired. Reference potential should be maintained during gradation voltage output. Refer to the recommended operating conditions for the relative magnitude of each potential. An 8+8 or 7+7 correction reference potential input is selectable as a TCP option. When a 7+7 correction reference is used, processing is performed internally to the TCP without GMA6 and GMA11. In this case, the relation between the GMAs and the input data is used as an output after dividing input data CO through FE by the IC's internal resistance.

Details of Pixel Signal Data:
Data format: 8-bits x 2 RGB
Input width: 48 bits (2-pixel data)

MSB							LSB
Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0

detailed description (continued)

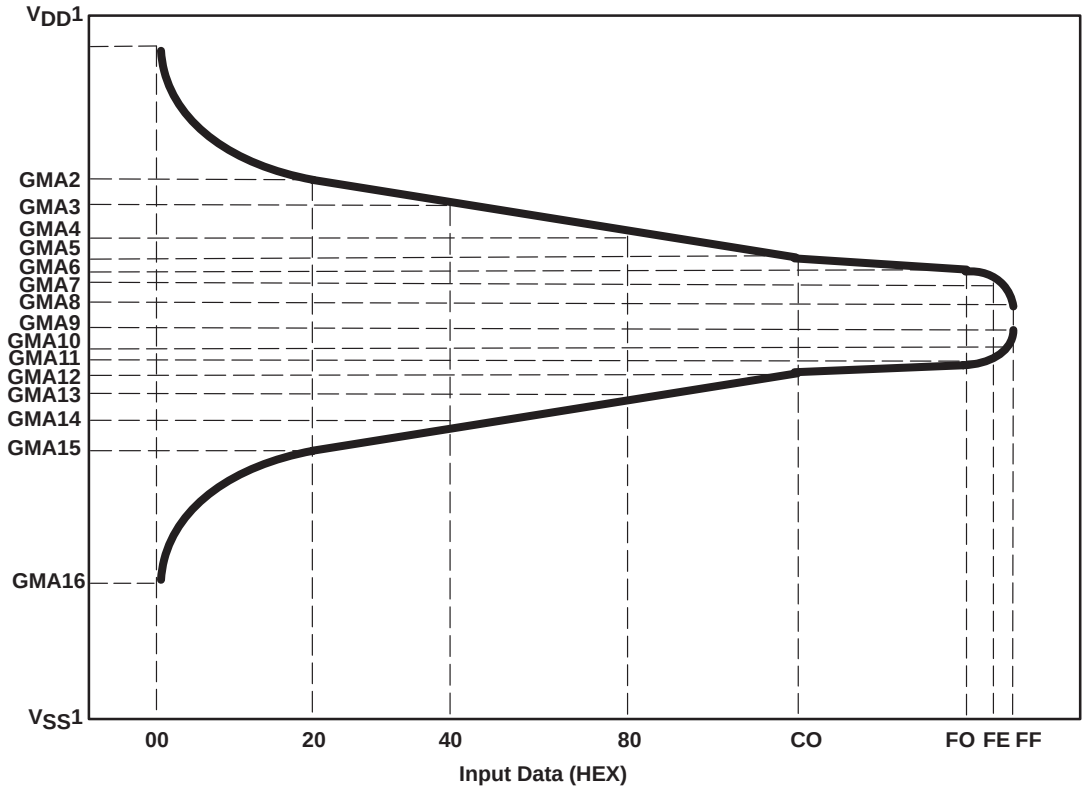
Relationship between shift direction and output data:

$\overline{L}$/R = H (right shift)

Output	Out 1	Out 2	Out 3	Out 4	Out 5	Out 6	...	Out 384
Data	D00~D07	D10~D17	D20~D27	D30~D37	D40~D47	D50~D57		D50~D57

$\overline{L}$/R = L (left shift)

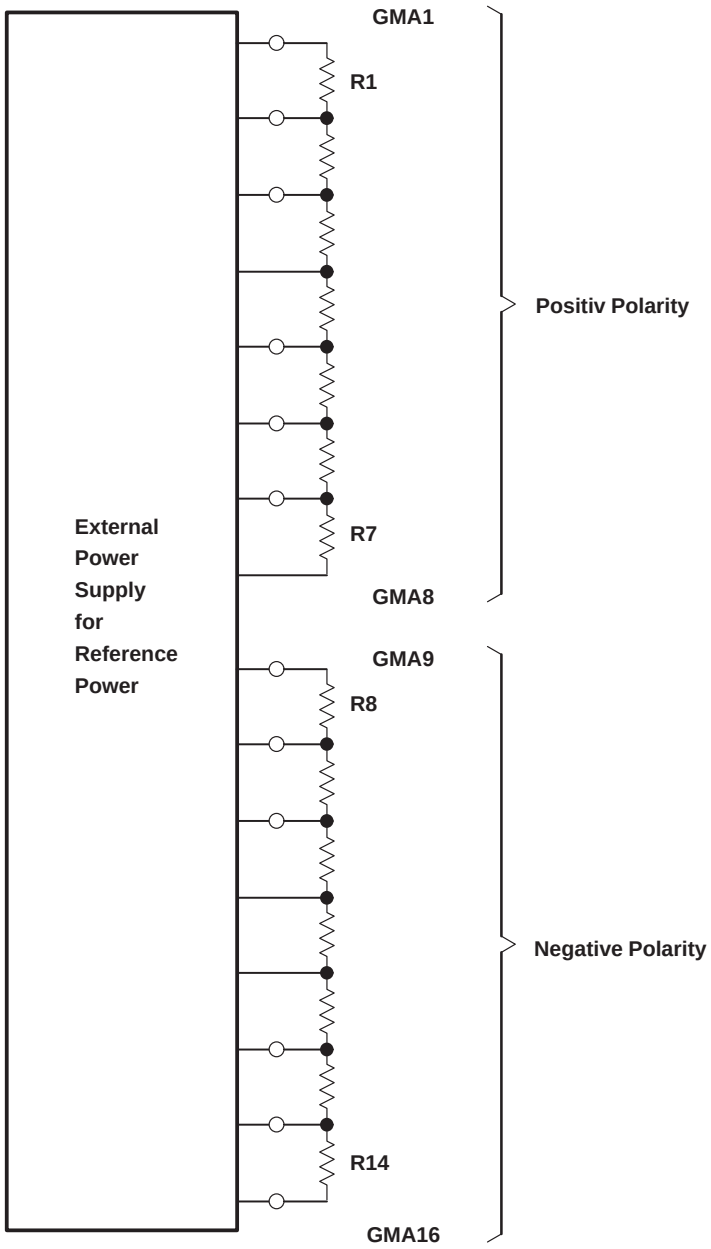
Output	Out 384	...	Out 6	Out 5	Out 4	Out 3	Out 2	Out 1
Data	D50~D57		D50~D57	D40~D47	D30~D37	D20~D27	D10~D17	D00~D07



NOTE: For input terminals GMA6 and GMA11, the TCP option can be used for internal processing.

Figure 1. Conceptual Drawing of Gamma Correction

detailed description (continued)



R1, R14	218 Ω
R2, R13	70 Ω
R3, R12	64 Ω
R4, R11	64 Ω
R5, R10	76 Ω
R6, R9	87 Ω
R7, R8	29 Ω

NOTE: GMA6 and GMA11 are processed within the TCP after selecting the TCP option 7+7. The internal resistances between GMA5–7 and between GMA10–12 become R5 + R6 and R9 + R10.

Figure 2. Resistance Between Reference Potential Input Terminals for Gamma Correction (Reference)

relationship between input data and output voltage at positive polarity

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
00	0	0	0	0	0	0	0	0	GMA1
01	0	0	0	0	0	0	0	1	GMA2+(GMA1–GMA2)x197/218
02	0	0	0	0	0	0	1	0	GMA2+(GMA1–GMA2)x176/218
03	0	0	0	0	0	0	1	1	GMA2+(GMA1–GMA2)x161/218
04	0	0	0	0	0	1	0	0	GMA2+(GMA1–GMA2)x146/218
05	0	0	0	0	0	1	0	1	GMA2+(GMA1–GMA2)x135/218
06	0	0	0	0	0	1	1	0	GMA2+(GMA1–GMA2)x124/218
07	0	0	0	0	0	1	1	1	GMA2+(GMA1–GMA2)x116/218
08	0	0	0	0	1	0	0	0	GMA2+(GMA1–GMA2)x108/218
09	0	0	0	0	1	0	0	1	GMA2+(GMA1–GMA2)x100/218
0A	0	0	0	0	1	0	1	0	GMA2+(GMA1–GMA2)x92/218
0B	0	0	0	0	1	0	1	1	GMA2+(GMA1–GMA2)x84/218
0C	0	0	0	0	1	1	0	0	GMA2+(GMA1–GMA2)x76/218
0D	0	0	0	0	1	1	0	1	GMA2+(GMA1–GMA2)x71/218
0E	0	0	0	0	1	1	1	0	GMA2+(GMA1–GMA2)x66/218
0F	0	0	0	0	1	1	1	1	GMA2+(GMA1–GMA2)x61/218
10	0	0	0	1	0	0	0	0	GMA2+(GMA1–GMA2)x56/218
11	0	0	0	1	0	0	0	1	GMA2+(GMA1–GMA2)x52/218
12	0	0	0	1	0	0	1	0	GMA2+(GMA1–GMA2)x48/218
13	0	0	0	1	0	0	1	1	GMA2+(GMA1–GMA2)x44/218
14	0	0	0	1	0	1	0	0	GMA2+(GMA1–GMA2)x40/218
15	0	0	0	1	0	1	0	1	GMA2+(GMA1–GMA2)x36/218
16	0	0	0	1	0	1	1	0	GMA2+(GMA1–GMA2)x32/218
17	0	0	0	1	0	1	1	1	GMA2+(GMA1–GMA2)x28/218
18	0	0	0	1	1	0	0	0	GMA2+(GMA1–GMA2)x24/218
19	0	0	0	1	1	0	0	1	GMA2+(GMA1–GMA2)x21/218
1A	0	0	0	1	1	0	1	0	GMA2+(GMA1–GMA2)x18/218
1B	0	0	0	1	1	0	1	1	GMA2+(GMA1–GMA2)x15/218
1C	0	0	0	1	1	1	0	0	GMA2+(GMA1–GMA2)x12/218
1D	0	0	0	1	1	1	0	1	GMA2+(GMA1–GMA2)x9/218
1E	0	0	0	1	1	1	1	0	GMA2+(GMA1–GMA2)x6/218
1F	0	0	0	1	1	1	1	1	GMA2+(GMA1–GMA2)x3/218
20	0	0	1	0	0	0	0	0	GMA2
21	0	0	1	0	0	0	0	1	GMA3+(GMA2–GMA3)x67/70
22	0	0	1	0	0	0	1	0	GMA3+(GMA2–GMA3)x64/70
23	0	0	1	0	0	0	1	1	GMA3+(GMA2–GMA3)x61/70
24	0	0	1	0	0	1	0	0	GMA3+(GMA2–GMA3)x58/70
25	0	0	1	0	0	1	0	1	GMA3+(GMA2–GMA3)x55/70
26	0	0	1	0	0	1	1	0	GMA3+(GMA2–GMA3)x52/70
27	0	0	1	0	0	1	1	1	GMA3+(GMA2–GMA3)x49/70
28	0	0	1	0	1	0	0	0	GMA3+(GMA2–GMA3)x47/70
29	0	0	1	0	1	0	0	1	GMA3+(GMA2–GMA3)x45/70
2A	0	0	1	0	1	0	1	0	GMA3+(GMA2–GMA3)x43/70
2B	0	0	1	0	1	0	1	1	GMA3+(GMA2–GMA3)x41/70
2C	0	0	1	0	1	1	0	0	GMA3+(GMA2–GMA3)x39/70
2D	0	0	1	0	1	1	0	1	GMA3+(GMA2–GMA3)x37/70
2E	0	0	1	0	1	1	1	0	GMA3+(GMA2–GMA3)x35/70
2F	0	0	1	0	1	1	1	1	GMA3+(GMA2–GMA3)x33/70

relationship between input data and output voltage at positive polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
30	0	0	1	1	0	0	0	0	GMA3+(GMA2–GMA3)x31/70
31	0	0	1	1	0	0	0	1	GMA3+(GMA2–GMA3)x29/70
32	0	0	1	1	0	0	1	0	GMA3+(GMA2–GMA3)x27/70
33	0	0	1	1	0	0	1	1	GMA3+(GMA2–GMA3)x25/70
34	0	0	1	1	0	1	0	0	GMA3+(GMA2–GMA3)x23/70
35	0	0	1	1	0	1	0	1	GMA3+(GMA2–GMA3)x21/70
36	0	0	1	1	0	1	1	0	GMA3+(GMA2–GMA3)x19/70
37	0	0	1	1	0	1	1	1	GMA3+(GMA2–GMA3)x17/70
38	0	0	1	1	1	0	0	0	GMA3+(GMA2–GMA3)x15/70
39	0	0	1	1	1	0	0	1	GMA3+(GMA2–GMA3)x13/70
3A	0	0	1	1	1	0	1	0	GMA3+(GMA2–GMA3)x11/70
3B	0	0	1	1	1	0	1	1	GMA3+(GMA2–GMA3)x9/70
3C	0	0	1	1	1	1	0	0	GMA3+(GMA2–GMA3)x7/70
3D	0	0	1	1	1	1	0	1	GMA3+(GMA2–GMA3)x5/70
3E	0	0	1	1	1	1	1	0	GMA3+(GMA2–GMA3)x3/70
3F	0	0	1	1	1	1	1	1	GMA3+(GMA2–GMA3)x1/70
40	0	1	0	0	0	0	0	0	GMA3
41	0	1	0	0	0	0	0	1	GMA4+(GMA3–GMA4)x63/64
42	0	1	0	0	0	0	1	0	GMA4+(GMA3–GMA4)x62/64
43	0	1	0	0	0	0	1	1	GMA4+(GMA3–GMA4)x61/64
44	0	1	0	0	0	1	0	0	GMA4+(GMA3–GMA4)x60/64
45	0	1	0	0	0	1	0	1	GMA4+(GMA3–GMA4)x59/64
46	0	1	0	0	0	1	1	0	GMA4+(GMA3–GMA4)x58/64
47	0	1	0	0	0	1	1	1	GMA4+(GMA3–GMA4)x57/64
48	0	1	0	0	1	0	0	0	GMA4+(GMA3–GMA4)x56/64
49	0	1	0	0	1	0	0	1	GMA4+(GMA3–GMA4)x55/64
4A	0	1	0	0	1	0	1	0	GMA4+(GMA3–GMA4)x54/64
4B	0	1	0	0	1	0	1	1	GMA4+(GMA3–GMA4)x53/64
4C	0	1	0	0	1	1	0	0	GMA4+(GMA3–GMA4)x52/64
4D	0	1	0	0	1	1	0	1	GMA4+(GMA3–GMA4)x51/64
4E	0	1	0	0	1	1	1	0	GMA4+(GMA3–GMA4)x50/64
4F	0	1	0	0	1	1	1	1	GMA4+(GMA3–GMA4)x49/64
50	0	1	0	1	0	0	0	0	GMA4+(GMA3–GMA4)x48/64
51	0	1	0	1	0	0	0	1	GMA4+(GMA3–GMA4)x47/64
52	0	1	0	1	0	0	1	0	GMA4+(GMA3–GMA4)x46/64
53	0	1	0	1	0	0	1	1	GMA4+(GMA3–GMA4)x45/64
54	0	1	0	1	0	1	0	0	GMA4+(GMA3–GMA4)x44/64
55	0	1	0	1	0	1	0	1	GMA4+(GMA3–GMA4)x43/64
56	0	1	0	1	0	1	1	0	GMA4+(GMA3–GMA4)x42/64
57	0	1	0	1	0	1	1	1	GMA4+(GMA3–GMA4)x41/64
58	0	1	0	1	1	0	0	0	GMA4+(GMA3–GMA4)x40/64
59	0	1	0	1	1	0	0	1	GMA4+(GMA3–GMA4)x39/64
5A	0	1	0	1	1	0	1	0	GMA4+(GMA3–GMA4)x38/64
5B	0	1	0	1	1	0	1	1	GMA4+(GMA3–GMA4)x37/64
5C	0	1	0	1	1	1	0	0	GMA4+(GMA3–GMA4)x36/64
5D	0	1	0	1	1	1	0	1	GMA4+(GMA3–GMA4)x35/64
5E	0	1	0	1	1	1	1	0	GMA4+(GMA3–GMA4)x34/64
5F	0	1	0	1	1	1	1	1	GMA4+(GMA3–GMA4)x33/64

relationship between input data and output voltage at positive polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
60	0	1	1	0	0	0	0	0	GMA4+(GMA3–GMA4)x32/64
61	0	1	1	0	0	0	0	1	GMA4+(GMA3–GMA4)x31/64
62	0	1	1	0	0	0	1	0	GMA4+(GMA3–GMA4)x30/64
63	0	1	1	0	0	0	1	1	GMA4+(GMA3–GMA4)x29/64
64	0	1	1	0	0	1	0	0	GMA4+(GMA3–GMA4)x28/64
65	0	1	1	0	0	1	0	1	GMA4+(GMA3–GMA4)x27/64
66	0	1	1	0	0	1	1	0	GMA4+(GMA3–GMA4)x26/64
67	0	1	1	0	0	1	1	1	GMA4+(GMA3–GMA4)x25/64
68	0	1	1	0	1	0	0	0	GMA4+(GMA3–GMA4)x24/64
69	0	1	1	0	1	0	0	1	GMA4+(GMA3–GMA4)x23/64
6A	0	1	1	0	1	0	1	0	GMA4+(GMA3–GMA4)x22/64
6B	0	1	1	0	1	0	1	1	GMA4+(GMA3–GMA4)x21/64
6C	0	1	1	0	1	1	0	0	GMA4+(GMA3–GMA4)x20/64
6D	0	1	1	0	1	1	0	1	GMA4+(GMA3–GMA4)x19/64
6E	0	1	1	0	1	1	1	0	GMA4+(GMA3–GMA4)x18/64
6F	0	1	1	0	1	1	1	1	GMA4+(GMA3–GMA4)x17/64
70	0	1	1	1	0	0	0	0	GMA4+(GMA3–GMA4)x16/64
71	0	1	1	1	0	0	0	1	GMA4+(GMA3–GMA4)x15/64
72	0	1	1	1	0	0	1	0	GMA4+(GMA3–GMA4)x14/64
73	0	1	1	1	0	0	1	1	GMA4+(GMA3–GMA4)x13/64
74	0	1	1	1	0	1	0	0	GMA4+(GMA3–GMA4)x12/64
75	0	1	1	1	0	1	0	1	GMA4+(GMA3–GMA4)x11/64
76	0	1	1	1	0	1	1	0	GMA4+(GMA3–GMA4)x10/64
77	0	1	1	1	0	1	1	1	GMA4+(GMA3–GMA4)x9/64
78	0	1	1	1	1	0	0	0	GMA4+(GMA3–GMA4)x8/64
79	0	1	1	1	1	0	0	1	GMA4+(GMA3–GMA4)x7/64
7A	0	1	1	1	1	0	1	0	GMA4+(GMA3–GMA4)x6/64
7B	0	1	1	1	1	0	1	1	GMA4+(GMA3–GMA4)x5/64
7C	0	1	1	1	1	1	0	0	GMA4+(GMA3–GMA4)x4/64
7D	0	1	1	1	1	1	0	1	GMA4+(GMA3–GMA4)x3/64
7E	0	1	1	1	1	1	1	0	GMA4+(GMA3–GMA4)x2/64
7F	0	1	1	1	1	1	1	1	GMA4+(GMA3–GMA4)x1/64
80	1	0	0	0	0	0	0	0	GMA4
81	1	0	0	0	0	0	0	1	GMA5+(GMA4–GMA5)x63/64
82	1	0	0	0	0	0	1	0	GMA5+(GMA4–GMA5)x62/64
83	1	0	0	0	0	0	1	1	GMA5+(GMA4–GMA5)x61/64
84	1	0	0	0	0	1	0	0	GMA5+(GMA4–GMA5)x60/64
85	1	0	0	0	0	1	0	1	GMA5+(GMA4–GMA5)x59/64
86	1	0	0	0	0	1	1	0	GMA5+(GMA4–GMA5)x58/64
87	1	0	0	0	0	1	1	1	GMA5+(GMA4–GMA5)x57/64
88	1	0	0	0	1	0	0	0	GMA5+(GMA4–GMA5)x56/64
89	1	0	0	0	1	0	0	1	GMA5+(GMA4–GMA5)x55/64
8A	1	0	0	0	1	0	1	0	GMA5+(GMA4–GMA5)x54/64
8B	1	0	0	0	1	0	1	1	GMA5+(GMA4–GMA5)x53/64
8C	1	0	0	0	1	1	0	0	GMA5+(GMA4–GMA5)x52/64
8D	1	0	0	0	1	1	0	1	GMA5+(GMA4–GMA5)x51/64
8E	1	0	0	0	1	1	1	0	GMA5+(GMA4–GMA5)x50/64
8F	1	0	0	0	1	1	1	1	GMA5+(GMA4–GMA5)x49/64

relationship between input data and output voltage at positive polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
90	1	0	0	1	0	0	0	0	GMA5+(GMA4–GMA5)x48/64
91	1	0	0	1	0	0	0	1	GMA5+(GMA4–GMA5)x47/64
92	1	0	0	1	0	0	1	0	GMA5+(GMA4–GMA5)x46/64
93	1	0	0	1	0	0	1	1	GMA5+(GMA4–GMA5)x45/64
94	1	0	0	1	0	1	0	0	GMA5+(GMA4–GMA5)x44/64
95	1	0	0	1	0	1	0	1	GMA5+(GMA4–GMA5)x43/64
96	1	0	0	1	0	1	1	0	GMA5+(GMA4–GMA5)x42/64
97	1	0	0	1	0	1	1	1	GMA5+(GMA4–GMA5)x41/64
98	1	0	0	1	1	0	0	0	GMA5+(GMA4–GMA5)x40/64
99	1	0	0	1	1	0	0	1	GMA5+(GMA4–GMA5)x39/64
9A	1	0	0	1	1	0	1	0	GMA5+(GMA4–GMA5)x38/64
9B	1	0	0	1	1	0	1	1	GMA5+(GMA4–GMA5)x37/64
9C	1	0	0	1	1	1	0	0	GMA5+(GMA4–GMA5)x36/64
9D	1	0	0	1	1	1	0	1	GMA5+(GMA4–GMA5)x35/64
9E	1	0	0	1	1	1	1	0	GMA5+(GMA4–GMA5)x34/64
9F	1	0	0	1	1	1	1	1	GMA5+(GMA4–GMA5)x33/64
A0	1	0	1	0	0	0	0	0	GMA5+(GMA4–GMA5)x32/64
A1	1	0	1	0	0	0	0	1	GMA5+(GMA4–GMA5)x31/64
A2	1	0	1	0	0	0	1	0	GMA5+(GMA4–GMA5)x30/64
A3	1	0	1	0	0	0	1	1	GMA5+(GMA4–GMA5)x29/64
A4	1	0	1	0	0	1	0	0	GMA5+(GMA4–GMA5)x28/64
A5	1	0	1	0	0	1	0	1	GMA5+(GMA4–GMA5)x27/64
A6	1	0	1	0	0	1	1	0	GMA5+(GMA4–GMA5)x26/64
A7	1	0	1	0	0	1	1	1	GMA5+(GMA4–GMA5)x25/64
A8	1	0	1	0	1	0	0	0	GMA5+(GMA4–GMA5)x24/64
A9	1	0	1	0	1	0	0	1	GMA5+(GMA4–GMA5)x23/64
AA	1	0	1	0	1	0	1	0	GMA5+(GMA4–GMA5)x22/64
AB	1	0	1	0	1	0	1	1	GMA5+(GMA4–GMA5)x21/64
AC	1	0	1	0	1	1	0	0	GMA5+(GMA4–GMA5)x20/64
AD	1	0	1	0	1	1	0	1	GMA5+(GMA4–GMA5)x19/64
AE	1	0	1	0	1	1	1	0	GMA5+(GMA4–GMA5)x18/64
AF	1	0	1	0	1	1	1	1	GMA5+(GMA4–GMA5)x17/64
B0	1	0	1	1	0	0	0	0	GMA5+(GMA4–GMA5)x16/64
B1	1	0	1	1	0	0	0	1	GMA5+(GMA4–GMA5)x15/64
B2	1	0	1	1	0	0	1	0	GMA5+(GMA4–GMA5)x14/64
B3	1	0	1	1	0	0	1	1	GMA5+(GMA4–GMA5)x13/64
B4	1	0	1	1	0	1	0	0	GMA5+(GMA4–GMA5)x12/64
B5	1	0	1	1	0	1	0	1	GMA5+(GMA4–GMA5)x11/64
B6	1	0	1	1	0	1	1	0	GMA5+(GMA4–GMA5)x10/64
B7	1	0	1	1	0	1	1	1	GMA5+(GMA4–GMA5)x9/64
B8	1	0	1	1	1	0	0	0	GMA5+(GMA4–GMA5)x8/64
B9	1	0	1	1	1	0	0	1	GMA5+(GMA4–GMA5)x7/64
BA	1	0	1	1	1	0	1	0	GMA5+(GMA4–GMA5)x6/64
BB	1	0	1	1	1	0	1	1	GMA5+(GMA4–GMA5)x5/64
BC	1	0	1	1	1	1	0	0	GMA5+(GMA4–GMA5)x4/64
BD	1	0	1	1	1	1	0	1	GMA5+(GMA4–GMA5)x3/64
BE	1	0	1	1	1	1	1	0	GMA5+(GMA4–GMA5)x2/64
BF	1	0	1	1	1	1	1	1	GMA5+(GMA4–GMA5)x1/64

relationship between input data and output voltage at positive polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
C0	1	1	0	0	0	0	0	0	GMA5
C1	1	1	0	0	0	0	0	1	GMA6+(GMA5–GMA6)x75/76
C2	1	1	0	0	0	0	1	0	GMA6+(GMA5–GMA6)x74/76
C3	1	1	0	0	0	0	1	1	GMA6+(GMA5–GMA6)x73/76
C4	1	1	0	0	0	1	0	0	GMA6+(GMA5–GMA6)x72/76
C5	1	1	0	0	0	1	0	1	GMA6+(GMA5–GMA6)x71/76
C6	1	1	0	0	0	1	1	0	GMA6+(GMA5–GMA6)x70/76
C7	1	1	0	0	0	1	1	1	GMA6+(GMA5–GMA6)x69/76
C8	1	1	0	0	1	0	0	0	GMA6+(GMA5–GMA6)x68/76
C9	1	1	0	0	1	0	0	1	GMA6+(GMA5–GMA6)x67/76
CA	1	1	0	0	1	0	1	0	GMA6+(GMA5–GMA6)x66/76
CB	1	1	0	0	1	0	1	1	GMA6+(GMA5–GMA6)x65/76
CC	1	1	0	0	1	1	0	0	GMA6+(GMA5–GMA6)x64/76
CD	1	1	0	0	1	1	0	1	GMA6+(GMA5–GMA6)x63/76
CE	1	1	0	0	1	1	1	0	GMA6+(GMA5–GMA6)x62/76
CF	1	1	0	0	1	1	1	1	GMA6+(GMA5–GMA6)x61/76
D0	1	1	0	1	0	0	0	0	GMA6+(GMA5–GMA6)x60/76
D1	1	1	0	1	0	0	0	1	GMA6+(GMA5–GMA6)x59/76
D2	1	1	0	1	0	0	1	0	GMA6+(GMA5–GMA6)x58/76
D3	1	1	0	1	0	0	1	1	GMA6+(GMA5–GMA6)x57/76
D4	1	1	0	1	0	1	0	0	GMA6+(GMA5–GMA6)x56/76
D5	1	1	0	1	0	1	0	1	GMA6+(GMA5–GMA6)x55/76
D6	1	1	0	1	0	1	1	0	GMA6+(GMA5–GMA6)x54/76
D7	1	1	0	1	0	1	1	1	GMA6+(GMA5–GMA6)x53/76
D8	1	1	0	1	1	0	0	0	GMA6+(GMA5–GMA6)x51/76
D9	1	1	0	1	1	0	0	1	GMA6+(GMA5–GMA6)x49/76
DA	1	1	0	1	1	0	1	0	GMA6+(GMA5–GMA6)x47/76
DB	1	1	0	1	1	0	1	1	GMA6+(GMA5–GMA6)x45/76
DC	1	1	0	1	1	1	0	0	GMA6+(GMA5–GMA6)x43/76
DD	1	1	0	1	1	1	0	1	GMA6+(GMA5–GMA6)x41/76
DE	1	1	0	1	1	1	1	0	GMA6+(GMA5–GMA6)x39/76
DF	1	1	0	1	1	1	1	1	GMA6+(GMA5–GMA6)x37/76
E0	1	1	1	0	0	0	0	0	GMA6+(GMA5–GMA6)x35/76
E1	1	1	1	0	0	0	0	1	GMA6+(GMA5–GMA6)x33/76
E2	1	1	1	0	0	0	1	0	GMA6+(GMA5–GMA6)x31/76
E3	1	1	1	0	0	0	1	1	GMA6+(GMA5–GMA6)x29/76
E4	1	1	1	0	0	1	0	0	GMA6+(GMA5–GMA6)x27/76
E5	1	1	1	0	0	1	0	1	GMA6+(GMA5–GMA6)x25/76
E6	1	1	1	0	0	1	1	0	GMA6+(GMA5–GMA6)x23/76
E7	1	1	1	0	0	1	1	1	GMA6+(GMA5–GMA6)x21/76
E8	1	1	1	0	1	0	0	0	GMA6+(GMA5–GMA6)x19/76
E9	1	1	1	0	1	0	0	1	GMA6+(GMA5–GMA6)x17/76
EA	1	1	1	0	1	0	1	0	GMA6+(GMA5–GMA6)x15/76
EB	1	1	1	0	1	0	1	1	GMA6+(GMA5–GMA6)x13/76
EC	1	1	1	0	1	1	0	0	GMA6+(GMA5–GMA6)x11/76
ED	1	1	1	0	1	1	0	1	GMA6+(GMA5–GMA6)x9/76
EE	1	1	1	0	1	1	1	0	GMA6+(GMA5–GMA6)x6/76
EF	1	1	1	0	1	1	1	1	GMA6+(GMA5–GMA6)x3/76

relationship between input data and output voltage at positive polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
F0	1	1	1	1	0	0	0	0	GMA6
F1	1	1	1	1	0	0	0	1	GMA7+(GMA6–GMA7)x84/87
F2	1	1	1	1	0	0	1	0	GMA7+(GMA6–GMA7)x81/87
F3	1	1	1	1	0	0	1	1	GMA7+(GMA6–GMA7)x78/87
F4	1	1	1	1	0	1	0	0	GMA7+(GMA6–GMA7)x75/87
F5	1	1	1	1	0	1	0	1	GMA7+(GMA6–GMA7)x72/87
F6	1	1	1	1	0	1	1	0	GMA7+(GMA6–GMA7)x68/87
F7	1	1	1	1	0	1	1	1	GMA7+(GMA6–GMA7)x64/87
F8	1	1	1	1	1	0	0	0	GMA7+(GMA6–GMA7)x60/87
F9	1	1	1	1	1	0	0	1	GMA7+(GMA6–GMA7)x55/87
FA	1	1	1	1	1	0	1	0	GMA7+(GMA6–GMA7)x50/87
FB	1	1	1	1	1	0	1	1	GMA7+(GMA6–GMA7)x42/87
FC	1	1	1	1	1	1	0	0	GMA7+(GMA6–GMA7)x32/87
FD	1	1	1	1	1	1	0	1	GMA7+(GMA6–GMA7)x19/87
FE	1	1	1	1	1	1	1	0	GMA7
FF	1	1	1	1	1	1	1	1	GMA8

For 7x7 gamma correction reference potential (only data (H) C0-FD change):

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
C0	1	1	0	0	0	0	0	0	GMA5
C1	1	1	0	0	0	0	0	1	GMA7+(GMA5–GMA7)x162/163
C2	1	1	0	0	0	0	1	0	GMA7+(GMA5–GMA7)x161/163
C3	1	1	0	0	0	0	1	1	GMA7+(GMA5–GMA7)x160/163
C4	1	1	0	0	0	1	0	0	GMA7+(GMA5–GMA7)x159/163
C5	1	1	0	0	0	1	0	1	GMA7+(GMA5–GMA7)x158/163
C6	1	1	0	0	0	1	1	0	GMA7+(GMA5–GMA7)x157/163
C7	1	1	0	0	0	1	1	1	GMA7+(GMA5–GMA7)x156/163
C8	1	1	0	0	1	0	0	0	GMA7+(GMA5–GMA7)x155/163
C9	1	1	0	0	1	0	0	1	GMA7+(GMA5–GMA7)x154/163
CA	1	1	0	0	1	0	1	0	GMA7+(GMA5–GMA7)x153/163
CB	1	1	0	0	1	0	1	1	GMA7+(GMA5–GMA7)x152/163
CC	1	1	0	0	1	1	0	0	GMA7+(GMA5–GMA7)x151/163
CD	1	1	0	0	1	1	0	1	GMA7+(GMA5–GMA7)x150/163
CE	1	1	0	0	1	1	1	0	GMA7+(GMA5–GMA7)x149/163
CF	1	1	0	0	1	1	1	1	GMA7+(GMA5–GMA7)x148/163
D0	1	1	0	1	0	0	0	0	GMA7+(GMA5–GMA7)x147/163
D1	1	1	0	1	0	0	0	1	GMA7+(GMA5–GMA7)x146/163
D2	1	1	0	1	0	0	1	0	GMA7+(GMA5–GMA7)x145/163
D3	1	1	0	1	0	0	1	1	GMA7+(GMA5–GMA7)x144/163
D4	1	1	0	1	0	1	0	0	GMA7+(GMA5–GMA7)x143/163
D5	1	1	0	1	0	1	0	1	GMA7+(GMA5–GMA7)x142/163
D6	1	1	0	1	0	1	1	0	GMA7+(GMA5–GMA7)x141/163
D7	1	1	0	1	0	1	1	1	GMA7+(GMA5–GMA7)x140/163
D8	1	1	0	1	1	0	0	0	GMA7+(GMA5–GMA7)x138/163
D9	1	1	0	1	1	0	0	1	GMA7+(GMA5–GMA7)x136/163
DA	1	1	0	1	1	0	1	0	GMA7+(GMA5–GMA7)x134/163
DB	1	1	0	1	1	0	1	1	GMA7+(GMA5–GMA7)x132/163
DC	1	1	0	1	1	1	0	0	GMA7+(GMA5–GMA7)x130/163
DD	1	1	0	1	1	1	0	1	GMA7+(GMA5–GMA7)x128/163
DE	1	1	0	1	1	1	1	0	GMA7+(GMA5–GMA7)x126/163
DF	1	1	0	1	1	1	1	1	GMA7+(GMA5–GMA7)x124/163

relationship between input data and output voltage at positive polarity (continued)

For 7x7 gamma correction reference potential (only data (H) C0-FD change):

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
E0	1	1	1	0	0	0	0	0	GMA7+(GMA5–GMA7)x122/163
E1	1	1	1	0	0	0	0	1	GMA7+(GMA5–GMA7)x120/163
E2	1	1	1	0	0	0	1	0	GMA7+(GMA5–GMA7)x118/163
E3	1	1	1	0	0	0	1	1	GMA7+(GMA5–GMA7)x116/163
E4	1	1	1	0	0	1	0	0	GMA7+(GMA5–GMA7)x114/163
E5	1	1	1	0	0	1	0	1	GMA7+(GMA5–GMA7)x112/163
E6	1	1	1	0	0	1	1	0	GMA7+(GMA5–GMA7)x110/163
E7	1	1	1	0	0	1	1	1	GMA7+(GMA5–GMA7)x108/163
E8	1	1	1	0	1	0	0	0	GMA7+(GMA5–GMA7)x106/163
E9	1	1	1	0	1	0	0	1	GMA7+(GMA5–GMA7)x104/163
EA	1	1	1	0	1	0	1	0	GMA7+(GMA5–GMA7)x102/163
EB	1	1	1	0	1	0	1	1	GMA7+(GMA5–GMA7)x100/163
EC	1	1	1	0	1	1	0	0	GMA7+(GMA5–GMA7)x98/163
ED	1	1	1	0	1	1	0	1	GMA7+(GMA5–GMA7)x96/163
EE	1	1	1	0	1	1	1	0	GMA7+(GMA5–GMA7)x93/163
EF	1	1	1	0	1	1	1	1	GMA7+(GMA5–GMA7)x90/163
F0	1	1	1	1	0	0	0	0	GMA7+(GMA5–GMA7)x87/163
F1	1	1	1	1	0	0	0	1	GMA7+(GMA5–GMA7)x84/163
F2	1	1	1	1	0	0	1	0	GMA7+(GMA5–GMA7)x81/163
F3	1	1	1	1	0	0	1	1	GMA7+(GMA5–GMA7)x78/163
F4	1	1	1	1	0	1	0	0	GMA7+(GMA5–GMA7)x75/163
F5	1	1	1	1	0	1	0	1	GMA7+(GMA5–GMA7)x72/163
F6	1	1	1	1	0	1	1	0	GMA7+(GMA5–GMA7)x68/163
F7	1	1	1	1	0	1	1	1	GMA7+(GMA5–GMA7)x64/163
F8	1	1	1	1	1	0	0	0	GMA7+(GMA5–GMA7)x60/163
F9	1	1	1	1	1	0	0	1	GMA7+(GMA5–GMA7)x55/163
FA	1	1	1	1	1	0	1	0	GMA7+(GMA5–GMA7)x50/163
FB	1	1	1	1	1	0	1	1	GMA7+(GMA5–GMA7)x42/163
FC	1	1	1	1	1	1	0	0	GMA7+(GMA5–GMA7)x32/163
FD	1	1	1	1	1	1	0	1	GMA7+(GMA5–GMA7)x19/163
FE	1	1	1	1	1	1	1	0	GMA7
FF	1	1	1	1	1	1	1	1	GMA8

relationship between input data and output voltage at negative polarity

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
00	0	0	0	0	0	0	0	0	GMA16
01	0	0	0	0	0	0	0	1	GMA16+(GMA15–GMA16)x21/218
02	0	0	0	0	0	0	1	0	GMA16+(GMA15–GMA16)x42/218
03	0	0	0	0	0	0	1	1	GMA16+(GMA15–GMA16)x57/218
04	0	0	0	0	0	1	0	0	GMA16+(GMA15–GMA16)x72/218
05	0	0	0	0	0	1	0	1	GMA16+(GMA15–GMA16)x83/218
06	0	0	0	0	0	1	1	0	GMA16+(GMA15–GMA16)x94/218
07	0	0	0	0	0	1	1	1	GMA16+(GMA15–GMA16)x102/218
08	0	0	0	0	1	0	0	0	GMA16+(GMA15–GMA16)x110/218
09	0	0	0	0	1	0	0	1	GMA16+(GMA15–GMA16)x118/218
0A	0	0	0	0	1	0	1	0	GMA16+(GMA15–GMA16)x126/218
0B	0	0	0	0	1	0	1	1	GMA16+(GMA15–GMA16)x134/218
0C	0	0	0	0	1	1	0	0	GMA16+(GMA15–GMA16)x142/218
0D	0	0	0	0	1	1	0	1	GMA16+(GMA15–GMA16)x147/218
0E	0	0	0	0	1	1	1	0	GMA16+(GMA15–GMA16)x152/218
0F	0	0	0	0	1	1	1	1	GMA16+(GMA15–GMA16)x157/218
10	0	0	0	1	0	0	0	0	GMA16+(GMA15–GMA16)x162/218
11	0	0	0	1	0	0	0	1	GMA16+(GMA15–GMA16)x166/218
12	0	0	0	1	0	0	1	0	GMA16+(GMA15–GMA16)x170/218
13	0	0	0	1	0	0	1	1	GMA16+(GMA15–GMA16)x174/218
14	0	0	0	1	0	1	0	0	GMA16+(GMA15–GMA16)x178/218
15	0	0	0	1	0	1	0	1	GMA16+(GMA15–GMA16)x182/218
16	0	0	0	1	0	1	1	0	GMA16+(GMA15–GMA16)x186/218
17	0	0	0	1	0	1	1	1	GMA16+(GMA15–GMA16)x190/218
18	0	0	0	1	1	0	0	0	GMA16+(GMA15–GMA16)x194/218
19	0	0	0	1	1	0	0	1	GMA16+(GMA15–GMA16)x197/218
1A	0	0	0	1	1	0	1	0	GMA16+(GMA15–GMA16)x200/218
1B	0	0	0	1	1	0	1	1	GMA16+(GMA15–GMA16)x203/218
1C	0	0	0	1	1	1	0	0	GMA16+(GMA15–GMA16)x206/218
1D	0	0	0	1	1	1	0	1	GMA16+(GMA15–GMA16)x209/218
1E	0	0	0	1	1	1	1	0	GMA16+(GMA15–GMA16)x212/218
1F	0	0	0	1	1	1	1	1	GMA16+(GMA15–GMA16)x215/218
20	0	0	1	0	0	0	0	0	GMA15
21	0	0	1	0	0	0	0	1	GMA15+(GMA14–GMA15)x3/70
22	0	0	1	0	0	0	1	0	GMA15+(GMA14–GMA15)x6/70
23	0	0	1	0	0	0	1	1	GMA15+(GMA14–GMA15)x9/70
24	0	0	1	0	0	1	0	0	GMA15+(GMA14–GMA15)x12/70
25	0	0	1	0	0	1	0	1	GMA15+(GMA14–GMA15)x15/70
26	0	0	1	0	0	1	1	0	GMA15+(GMA14–GMA15)x18/70
27	0	0	1	0	0	1	1	1	GMA15+(GMA14–GMA15)x21/70
28	0	0	1	0	1	0	0	0	GMA15+(GMA14–GMA15)x23/70
29	0	0	1	0	1	0	0	1	GMA15+(GMA14–GMA15)x25/70
2A	0	0	1	0	1	0	1	0	GMA15+(GMA14–GMA15)x27/70
2B	0	0	1	0	1	0	1	1	GMA15+(GMA14–GMA15)x29/70
2C	0	0	1	0	1	1	0	0	GMA15+(GMA14–GMA15)x31/70
2D	0	0	1	0	1	1	0	1	GMA15+(GMA14–GMA15)x33/70
2E	0	0	1	0	1	1	1	0	GMA15+(GMA14–GMA15)x35/70
2F	0	0	1	0	1	1	1	1	GMA15+(GMA14–GMA15)x37/70

relationship between input data and output voltage at negative polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
30	0	0	1	1	0	0	0	0	GMA15+(GMA14–GMA15)x39/70
31	0	0	1	1	0	0	0	1	GMA15+(GMA14–GMA15)x41/70
32	0	0	1	1	0	0	1	0	GMA15+(GMA14–GMA15)x43/70
33	0	0	1	1	0	0	1	1	GMA15+(GMA14–GMA15)x45/70
34	0	0	1	1	0	1	0	0	GMA15+(GMA14–GMA15)x47/70
35	0	0	1	1	0	1	0	1	GMA15+(GMA14–GMA15)x49/70
36	0	0	1	1	0	1	1	0	GMA15+(GMA14–GMA15)x51/70
37	0	0	1	1	0	1	1	1	GMA15+(GMA14–GMA15)x53/70
38	0	0	1	1	1	0	0	0	GMA15+(GMA14–GMA15)x55/70
39	0	0	1	1	1	0	0	1	GMA15+(GMA14–GMA15)x57/70
3A	0	0	1	1	1	0	1	0	GMA15+(GMA14–GMA15)x59/70
3B	0	0	1	1	1	0	1	1	GMA15+(GMA14–GMA15)x61/70
3C	0	0	1	1	1	1	0	0	GMA15+(GMA14–GMA15)x63/70
3D	0	0	1	1	1	1	0	1	GMA15+(GMA14–GMA15)x65/70
3E	0	0	1	1	1	1	1	0	GMA15+(GMA14–GMA15)x67/70
3F	0	0	1	1	1	1	1	1	GMA15+(GMA14–GMA15)x69/70
40	0	1	0	0	0	0	0	0	GMA14
41	0	1	0	0	0	0	0	1	GMA14+(GMA13–GMA14)x1/64
42	0	1	0	0	0	0	1	0	GMA14+(GMA13–GMA14)x2/64
43	0	1	0	0	0	0	1	1	GMA14+(GMA13–GMA14)x3/64
44	0	1	0	0	0	1	0	0	GMA14+(GMA13–GMA14)x4/64
45	0	1	0	0	0	1	0	1	GMA14+(GMA13–GMA14)x5/64
46	0	1	0	0	0	1	1	0	GMA14+(GMA13–GMA14)x6/64
47	0	1	0	0	0	1	1	1	GMA14+(GMA13–GMA14)x7/64
48	0	1	0	0	1	0	0	0	GMA14+(GMA13–GMA14)x8/64
49	0	1	0	0	1	0	0	1	GMA14+(GMA13–GMA14)x9/64
4A	0	1	0	0	1	0	1	0	GMA14+(GMA13–GMA14)x10/64
4B	0	1	0	0	1	0	1	1	GMA14+(GMA13–GMA14)x11/64
4C	0	1	0	0	1	1	0	0	GMA14+(GMA13–GMA14)x12/64
4D	0	1	0	0	1	1	0	1	GMA14+(GMA13–GMA14)x13/64
4E	0	1	0	0	1	1	1	0	GMA14+(GMA13–GMA14)x14/64
4F	0	1	0	0	1	1	1	1	GMA14+(GMA13–GMA14)x15/64
50	0	1	0	1	0	0	0	0	GMA14+(GMA13–GMA14)x16/64
51	0	1	0	1	0	0	0	1	GMA14+(GMA13–GMA14)x17/64
52	0	1	0	1	0	0	1	0	GMA14+(GMA13–GMA14)x18/64
53	0	1	0	1	0	0	1	1	GMA14+(GMA13–GMA14)x19/64
54	0	1	0	1	0	1	0	0	GMA14+(GMA13–GMA14)x20/64
55	0	1	0	1	0	1	0	1	GMA14+(GMA13–GMA14)x21/64
56	0	1	0	1	0	1	1	0	GMA14+(GMA13–GMA14)x22/64
57	0	1	0	1	0	1	1	1	GMA14+(GMA13–GMA14)x23/64
58	0	1	0	1	1	0	0	0	GMA14+(GMA13–GMA14)x24/64
59	0	1	0	1	1	0	0	1	GMA14+(GMA13–GMA14)x25/64
5A	0	1	0	1	1	0	1	0	GMA14+(GMA13–GMA14)x26/64
5B	0	1	0	1	1	0	1	1	GMA14+(GMA13–GMA14)x27/64
5C	0	1	0	1	1	1	0	0	GMA14+(GMA13–GMA14)x28/64
5D	0	1	0	1	1	1	0	1	GMA14+(GMA13–GMA14)x29/64
5E	0	1	0	1	1	1	1	0	GMA14+(GMA13–GMA14)x30/64
5F	0	1	0	1	1	1	1	1	GMA14+(GMA13–GMA14)x31/64

relationship between input data and output voltage at negative polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
60	0	1	1	0	0	0	0	0	GMA14+(GMA13–GMA14)x32/64
61	0	1	1	0	0	0	0	1	GMA14+(GMA13–GMA14)x33/64
62	0	1	1	0	0	0	1	0	GMA14+(GMA13–GMA14)x34/64
63	0	1	1	0	0	0	1	1	GMA14+(GMA13–GMA14)x35/64
64	0	1	1	0	0	1	0	0	GMA14+(GMA13–GMA14)x36/64
65	0	1	1	0	0	1	0	1	GMA14+(GMA13–GMA14)x37/64
66	0	1	1	0	0	1	1	0	GMA14+(GMA13–GMA14)x38/64
67	0	1	1	0	0	1	1	1	GMA14+(GMA13–GMA14)x39/64
68	0	1	1	0	1	0	0	0	GMA14+(GMA13–GMA14)x40/64
69	0	1	1	0	1	0	0	1	GMA14+(GMA13–GMA14)x41/64
6A	0	1	1	0	1	0	1	0	GMA14+(GMA13–GMA14)x42/64
6B	0	1	1	0	1	0	1	1	GMA14+(GMA13–GMA14)x43/64
6C	0	1	1	0	1	1	0	0	GMA14+(GMA13–GMA14)x44/64
6D	0	1	1	0	1	1	0	1	GMA14+(GMA13–GMA14)x45/64
6E	0	1	1	0	1	1	1	0	GMA14+(GMA13–GMA14)x46/64
6F	0	1	1	0	1	1	1	1	GMA14+(GMA13–GMA14)x47/64
70	0	1	1	1	0	0	0	0	GMA14+(GMA13–GMA14)x48/64
71	0	1	1	1	0	0	0	1	GMA14+(GMA13–GMA14)x49/64
72	0	1	1	1	0	0	1	0	GMA14+(GMA13–GMA14)x50/64
73	0	1	1	1	0	0	1	1	GMA14+(GMA13–GMA14)x51/64
74	0	1	1	1	0	1	0	0	GMA14+(GMA13–GMA14)x52/64
75	0	1	1	1	0	1	0	1	GMA14+(GMA13–GMA14)x53/64
76	0	1	1	1	0	1	1	0	GMA14+(GMA13–GMA14)x54/64
77	0	1	1	1	0	1	1	1	GMA14+(GMA13–GMA14)x55/64
78	0	1	1	1	1	0	0	0	GMA14+(GMA13–GMA14)x56/64
79	0	1	1	1	1	0	0	1	GMA14+(GMA13–GMA14)x57/64
7A	0	1	1	1	1	0	1	0	GMA14+(GMA13–GMA14)x58/64
7B	0	1	1	1	1	0	1	1	GMA14+(GMA13–GMA14)x59/64
7C	0	1	1	1	1	1	0	0	GMA14+(GMA13–GMA14)x60/64
7D	0	1	1	1	1	1	0	1	GMA14+(GMA13–GMA14)x61/64
7E	0	1	1	1	1	1	1	0	GMA14+(GMA13–GMA14)x62/64
7F	0	1	1	1	1	1	1	1	GMA14+(GMA13–GMA14)x63/64
80	1	0	0	0	0	0	0	0	GMA13
81	1	0	0	0	0	0	0	1	GMA13+(GMA12–GMA13)x1/64
82	1	0	0	0	0	0	1	0	GMA13+(GMA12–GMA13)x2/64
83	1	0	0	0	0	0	1	1	GMA13+(GMA12–GMA13)x3/64
84	1	0	0	0	0	1	0	0	GMA13+(GMA12–GMA13)x4/64
85	1	0	0	0	0	1	0	1	GMA13+(GMA12–GMA13)x5/64
86	1	0	0	0	0	1	1	0	GMA13+(GMA12–GMA13)x6/64
87	1	0	0	0	0	1	1	1	GMA13+(GMA12–GMA13)x7/64
88	1	0	0	0	1	0	0	0	GMA13+(GMA12–GMA13)x8/64
89	1	0	0	0	1	0	0	1	GMA13+(GMA12–GMA13)x9/64
8A	1	0	0	0	1	0	1	0	GMA13+(GMA12–GMA13)x10/64
8B	1	0	0	0	1	0	1	1	GMA13+(GMA12–GMA13)x11/64
8C	1	0	0	0	1	1	0	0	GMA13+(GMA12–GMA13)x12/64
8D	1	0	0	0	1	1	0	1	GMA13+(GMA12–GMA13)x13/64
8E	1	0	0	0	1	1	1	0	GMA13+(GMA12–GMA13)x14/64
8F	1	0	0	0	1	1	1	1	GMA13+(GMA12–GMA13)x15/64

relationship between input data and output voltage at negative polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
90	1	0	0	1	0	0	0	0	GMA13+(GMA12–GMA13)x16/64
91	1	0	0	1	0	0	0	1	GMA13+(GMA12–GMA13)x17/64
92	1	0	0	1	0	0	1	0	GMA13+(GMA12–GMA13)x18/64
93	1	0	0	1	0	0	1	1	GMA13+(GMA12–GMA13)x19/64
94	1	0	0	1	0	1	0	0	GMA13+(GMA12–GMA13)x20/64
95	1	0	0	1	0	1	0	1	GMA13+(GMA12–GMA13)x21/64
96	1	0	0	1	0	1	1	0	GMA13+(GMA12–GMA13)x22/64
97	1	0	0	1	0	1	1	1	GMA13+(GMA12–GMA13)x23/64
98	1	0	0	1	1	0	0	0	GMA13+(GMA12–GMA13)x24/64
99	1	0	0	1	1	0	0	1	GMA13+(GMA12–GMA13)x25/64
9A	1	0	0	1	1	0	1	0	GMA13+(GMA12–GMA13)x26/64
9B	1	0	0	1	1	0	1	1	GMA13+(GMA12–GMA13)x27/64
9C	1	0	0	1	1	1	0	0	GMA13+(GMA12–GMA13)x28/64
9D	1	0	0	1	1	1	0	1	GMA13+(GMA12–GMA13)x29/64
9E	1	0	0	1	1	1	1	0	GMA13+(GMA12–GMA13)x30/64
9F	1	0	0	1	1	1	1	1	GMA13+(GMA12–GMA13)x31/64
A0	1	0	1	0	0	0	0	0	GMA13+(GMA12–GMA13)x32/64
A1	1	0	1	0	0	0	0	1	GMA13+(GMA12–GMA13)x33/64
A2	1	0	1	0	0	0	1	0	GMA13+(GMA12–GMA13)x34/64
A3	1	0	1	0	0	0	1	1	GMA13+(GMA12–GMA13)x35/64
A4	1	0	1	0	0	1	0	0	GMA13+(GMA12–GMA13)x36/64
A5	1	0	1	0	0	1	0	1	GMA13+(GMA12–GMA13)x37/64
A6	1	0	1	0	0	1	1	0	GMA13+(GMA12–GMA13)x38/64
A7	1	0	1	0	0	1	1	1	GMA13+(GMA12–GMA13)x39/64
A8	1	0	1	0	1	0	0	0	GMA13+(GMA12–GMA13)x40/64
A9	1	0	1	0	1	0	0	1	GMA13+(GMA12–GMA13)x41/64
AA	1	0	1	0	1	0	1	0	GMA13+(GMA12–GMA13)x42/64
AB	1	0	1	0	1	0	1	1	GMA13+(GMA12–GMA13)x43/64
AC	1	0	1	0	1	1	0	0	GMA13+(GMA12–GMA13)x44/64
AD	1	0	1	0	1	1	0	1	GMA13+(GMA12–GMA13)x45/64
AE	1	0	1	0	1	1	1	0	GMA13+(GMA12–GMA13)x46/64
AF	1	0	1	0	1	1	1	1	GMA13+(GMA12–GMA13)x47/64
B0	1	0	1	1	0	0	0	0	GMA13+(GMA12–GMA13)x48/64
B1	1	0	1	1	0	0	0	1	GMA13+(GMA12–GMA13)x49/64
B2	1	0	1	1	0	0	1	0	GMA13+(GMA12–GMA13)x50/64
B3	1	0	1	1	0	0	1	1	GMA13+(GMA12–GMA13)x51/64
B4	1	0	1	1	0	1	0	0	GMA13+(GMA12–GMA13)x52/64
B5	1	0	1	1	0	1	0	1	GMA13+(GMA12–GMA13)x53/64
B6	1	0	1	1	0	1	1	0	GMA13+(GMA12–GMA13)x54/64
B7	1	0	1	1	0	1	1	1	GMA13+(GMA12–GMA13)x55/64
B8	1	0	1	1	1	0	0	0	GMA13+(GMA12–GMA13)x56/64
B9	1	0	1	1	1	0	0	1	GMA13+(GMA12–GMA13)x57/64
BA	1	0	1	1	1	0	1	0	GMA13+(GMA12–GMA13)x58/64
BB	1	0	1	1	1	0	1	1	GMA13+(GMA12–GMA13)x59/64
BC	1	0	1	1	1	1	0	0	GMA13+(GMA12–GMA13)x60/64
BD	1	0	1	1	1	1	0	1	GMA13+(GMA12–GMA13)x61/64
BE	1	0	1	1	1	1	1	0	GMA13+(GMA12–GMA13)x62/64
BF	1	0	1	1	1	1	1	1	GMA13+(GMA12–GMA13)x63/64

relationship between input data and output voltage at negative polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
C0	1	1	0	0	0	0	0	0	GMA12
C1	1	1	0	0	0	0	0	1	GMA12+(GMA11–GMA12)x1/76
C2	1	1	0	0	0	0	1	0	GMA12+(GMA11–GMA12)x2/76
C3	1	1	0	0	0	0	1	1	GMA12+(GMA11–GMA12)x3/76
C4	1	1	0	0	0	1	0	0	GMA12+(GMA11–GMA12)x4/76
C5	1	1	0	0	0	1	0	1	GMA12+(GMA11–GMA12)x5/76
C6	1	1	0	0	0	1	1	0	GMA12+(GMA11–GMA12)x6/76
C7	1	1	0	0	0	1	1	1	GMA12+(GMA11–GMA12)x7/76
C8	1	1	0	0	1	0	0	0	GMA12+(GMA11–GMA12)x8/76
C9	1	1	0	0	1	0	0	1	GMA12+(GMA11–GMA12)x9/76
CA	1	1	0	0	1	0	1	0	GMA12+(GMA11–GMA12)x10/76
CB	1	1	0	0	1	0	1	1	GMA12+(GMA11–GMA12)x11/76
CC	1	1	0	0	1	1	0	0	GMA12+(GMA11–GMA12)x12/76
CD	1	1	0	0	1	1	0	1	GMA12+(GMA11–GMA12)x13/76
CE	1	1	0	0	1	1	1	0	GMA12+(GMA11–GMA12)x14/76
CF	1	1	0	0	1	1	1	1	GMA12+(GMA11–GMA12)x15/76
D0	1	1	0	1	0	0	0	0	GMA12+(GMA11–GMA12)x16/76
D1	1	1	0	1	0	0	0	1	GMA12+(GMA11–GMA12)x17/76
D2	1	1	0	1	0	0	1	0	GMA12+(GMA11–GMA12)x18/76
D3	1	1	0	1	0	0	1	1	GMA12+(GMA11–GMA12)x19/76
D4	1	1	0	1	0	1	0	0	GMA12+(GMA11–GMA12)x20/76
D5	1	1	0	1	0	1	0	1	GMA12+(GMA11–GMA12)x21/76
D6	1	1	0	1	0	1	1	0	GMA12+(GMA11–GMA12)x22/76
D7	1	1	0	1	0	1	1	1	GMA12+(GMA11–GMA12)x23/76
D8	1	1	0	1	1	0	0	0	GMA12+(GMA11–GMA12)x25/76
D9	1	1	0	1	1	0	0	1	GMA12+(GMA11–GMA12)x27/76
DA	1	1	0	1	1	0	1	0	GMA12+(GMA11–GMA12)x29/76
DB	1	1	0	1	1	0	1	1	GMA12+(GMA11–GMA12)x31/76
DC	1	1	0	1	1	1	0	0	GMA12+(GMA11–GMA12)x33/76
DD	1	1	0	1	1	1	0	1	GMA12+(GMA11–GMA12)x35/76
DE	1	1	0	1	1	1	1	0	GMA12+(GMA11–GMA12)x37/76
DF	1	1	0	1	1	1	1	1	GMA12+(GMA11–GMA12)x39/76
E0	1	1	1	0	0	0	0	0	GMA12+(GMA11–GMA12)x41/76
E1	1	1	1	0	0	0	0	1	GMA12+(GMA11–GMA12)x43/76
E2	1	1	1	0	0	0	1	0	GMA12+(GMA11–GMA12)x45/76
E3	1	1	1	0	0	0	1	1	GMA12+(GMA11–GMA12)x47/76
E4	1	1	1	0	0	1	0	0	GMA12+(GMA11–GMA12)x49/76
E5	1	1	1	0	0	1	0	1	GMA12+(GMA11–GMA12)x51/76
E6	1	1	1	0	0	1	1	0	GMA12+(GMA11–GMA12)x53/76
E7	1	1	1	0	0	1	1	1	GMA12+(GMA11–GMA12)x55/76
E8	1	1	1	0	1	0	0	0	GMA12+(GMA11–GMA12)x57/76
E9	1	1	1	0	1	0	0	1	GMA12+(GMA11–GMA12)x59/76
EA	1	1	1	0	1	0	1	0	GMA12+(GMA11–GMA12)x61/76
EB	1	1	1	0	1	0	1	1	GMA12+(GMA11–GMA12)x63/76
EC	1	1	1	0	1	1	0	0	GMA12+(GMA11–GMA12)x65/76
ED	1	1	1	0	1	1	0	1	GMA12+(GMA11–GMA12)x67/76
EE	1	1	1	0	1	1	1	0	GMA12+(GMA11–GMA12)x70/76
EF	1	1	1	0	1	1	1	1	GMA12+(GMA11–GMA12)x73/76

relationship between input data and output voltage at negative polarity (continued)

For 8x8 gamma correction reference potential:

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
F0	1	1	1	1	0	0	0	0	GMA11
F1	1	1	1	1	0	0	0	1	GMA11+(GMA10–GMA11)x3/87
F2	1	1	1	1	0	0	1	0	GMA11+(GMA10–GMA11)x6/87
F3	1	1	1	1	0	0	1	1	GMA11+(GMA10–GMA11)x9/87
F4	1	1	1	1	0	1	0	0	GMA11+(GMA10–GMA11)x12/87
F5	1	1	1	1	0	1	0	1	GMA11+(GMA10–GMA11)x15/87
F6	1	1	1	1	0	1	1	0	GMA11+(GMA10–GMA11)x19/87
F7	1	1	1	1	0	1	1	1	GMA11+(GMA10–GMA11)x23/87
F8	1	1	1	1	1	0	0	0	GMA11+(GMA10–GMA11)x27/87
F9	1	1	1	1	1	0	0	1	GMA11+(GMA10–GMA11)x32/87
FA	1	1	1	1	1	0	1	0	GMA11+(GMA10–GMA11)x37/87
FB	1	1	1	1	1	0	1	1	GMA11+(GMA10–GMA11)x45/87
FC	1	1	1	1	1	1	0	0	GMA11+(GMA10–GMA11)x55/87
FD	1	1	1	1	1	1	0	1	GMA11+(GMA10–GMA11)x68/87
FE	1	1	1	1	1	1	1	0	GMA10
FF	1	1	1	1	1	1	1	1	GMA9

For 7x7 gamma correction reference potential (only data (H) C0-FD change):

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
C0	1	1	0	0	0	0	0	0	GMA12
C1	1	1	0	0	0	0	0	1	GMA12+(GMA10–GMA12)x1/163
C2	1	1	0	0	0	0	1	0	GMA12+(GMA10–GMA12)x2/163
C3	1	1	0	0	0	0	1	1	GMA12+(GMA10–GMA12)x3/163
C4	1	1	0	0	0	1	0	0	GMA12+(GMA10–GMA12)x4/163
C5	1	1	0	0	0	1	0	1	GMA12+(GMA10–GMA12)x5/163
C6	1	1	0	0	0	1	1	0	GMA12+(GMA10–GMA12)x6/163
C7	1	1	0	0	0	1	1	1	GMA12+(GMA10–GMA12)x7/163
C8	1	1	0	0	1	0	0	0	GMA12+(GMA10–GMA12)x8/163
C9	1	1	0	0	1	0	0	1	GMA12+(GMA10–GMA12)x9/163
CA	1	1	0	0	1	0	1	0	GMA12+(GMA10–GMA12)x10/163
CB	1	1	0	0	1	0	1	1	GMA12+(GMA10–GMA12)x11/163
CC	1	1	0	0	1	1	0	0	GMA12+(GMA10–GMA12)x12/163
CD	1	1	0	0	1	1	0	1	GMA12+(GMA10–GMA12)x13/163
CE	1	1	0	0	1	1	1	0	GMA12+(GMA10–GMA12)x14/163
CF	1	1	0	0	1	1	1	1	GMA12+(GMA10–GMA12)x15/163
D0	1	1	0	1	0	0	0	0	GMA12+(GMA10–GMA12)x16/163
D1	1	1	0	1	0	0	0	1	GMA12+(GMA10–GMA12)x17/163
D2	1	1	0	1	0	0	1	0	GMA12+(GMA10–GMA12)x18/163
D3	1	1	0	1	0	0	1	1	GMA12+(GMA10–GMA12)x19/163
D4	1	1	0	1	0	1	0	0	GMA12+(GMA10–GMA12)x20/163
D5	1	1	0	1	0	1	0	1	GMA12+(GMA10–GMA12)x21/163
D6	1	1	0	1	0	1	1	0	GMA12+(GMA10–GMA12)x22/163
D7	1	1	0	1	0	1	1	1	GMA12+(GMA10–GMA12)x23/163
D8	1	1	0	1	1	0	0	0	GMA12+(GMA10–GMA12)x25/163
D9	1	1	0	1	1	0	0	1	GMA12+(GMA10–GMA12)x27/163
DA	1	1	0	1	1	0	1	0	GMA12+(GMA10–GMA12)x29/163
DB	1	1	0	1	1	0	1	1	GMA12+(GMA10–GMA12)x31/163
DC	1	1	0	1	1	1	0	0	GMA12+(GMA10–GMA12)x33/163
DD	1	1	0	1	1	1	0	1	GMA12+(GMA10–GMA12)x35/163
DE	1	1	0	1	1	1	1	0	GMA12+(GMA10–GMA12)x37/163
DF	1	1	0	1	1	1	1	1	GMA12+(GMA10–GMA12)x39/163

relationship between input data and output voltage at negative polarity (continued)

For 7x7 gamma correction reference potential (only data (H) C0-FD change):

DATA (H)	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	OUTPUT VOLTAGE
E0	1	1	1	0	0	0	0	0	GMA12+(GMA10–GMA12)x41/163
E1	1	1	1	0	0	0	0	1	GMA12+(GMA10–GMA12)x43/163
E2	1	1	1	0	0	0	1	0	GMA12+(GMA10–GMA12)x45/163
E3	1	1	1	0	0	0	1	1	GMA12+(GMA10–GMA12)x47/163
E4	1	1	1	0	0	1	0	0	GMA12+(GMA10–GMA12)x49/163
E5	1	1	1	0	0	1	0	1	GMA12+(GMA10–GMA12)x51/163
E6	1	1	1	0	0	1	1	0	GMA12+(GMA10–GMA12)x53/163
E7	1	1	1	0	0	1	1	1	GMA12+(GMA10–GMA12)x55/163
E8	1	1	1	0	1	0	0	0	GMA12+(GMA10–GMA12)x57/163
E9	1	1	1	0	1	0	0	1	GMA12+(GMA10–GMA12)x59/163
EA	1	1	1	0	1	0	1	0	GMA12+(GMA10–GMA12)x61/163
EB	1	1	1	0	1	0	1	1	GMA12+(GMA10–GMA12)x63/163
EC	1	1	1	0	1	1	0	0	GMA12+(GMA10–GMA12)x65/163
ED	1	1	1	0	1	1	0	1	GMA12+(GMA10–GMA12)x67/163
EE	1	1	1	0	1	1	1	0	GMA12+(GMA10–GMA12)x70/163
EF	1	1	1	0	1	1	1	1	GMA12+(GMA10–GMA12)x73/163
F0	1	1	1	1	0	0	0	0	GMA12+(GMA10–GMA12)x76/163
F1	1	1	1	1	0	0	0	1	GMA12+(GMA10–GMA12)x79/163
F2	1	1	1	1	0	0	1	0	GMA12+(GMA10–GMA12)x82/163
F3	1	1	1	1	0	0	1	1	GMA12+(GMA10–GMA12)x85/163
F4	1	1	1	1	0	1	0	0	GMA12+(GMA10–GMA12)x88/163
F5	1	1	1	1	0	1	0	1	GMA12+(GMA10–GMA12)x91/163
F6	1	1	1	1	0	1	1	0	GMA12+(GMA10–GMA12)x95/163
F7	1	1	1	1	0	1	1	1	GMA12+(GMA10–GMA12)x99/163
F8	1	1	1	1	1	0	0	0	GMA12+(GMA10–GMA12)x103/163
F9	1	1	1	1	1	0	0	1	GMA12+(GMA10–GMA12)x108/163
FA	1	1	1	1	1	0	1	0	GMA12+(GMA10–GMA12)x113/163
FB	1	1	1	1	1	0	1	1	GMA12+(GMA10–GMA12)x121/163
FC	1	1	1	1	1	1	0	0	GMA12+(GMA10–GMA12)x131/163
FD	1	1	1	1	1	1	0	1	GMA12+(GMA10–GMA12)x144/163
FE	1	1	1	1	1	1	1	0	GMA10
FF	1	1	1	1	1	1	1	1	GMA9

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD1} (see Notes 1 and 2) . . . . . –0.5 V to +14 V
Supply voltage, V_{DD2} . . . . . –0.5 V to +5 V
Input voltage, V_I (GMA1–GMA16) . . . . . –0.5 V to V_{DD1} + 0.5 V
Input voltage, V_I (analog inputs) . . . . . –0.5 V to V_{DD2} + 0.5 V
Output voltage, V_O (EIO1, EIO2) . . . . . –0.5 V to V_{DD2} + 0.5 V
Output voltage, V_O (OUT1–OUT384) . . . . . –0.5 V to V_{DD1} + 0.5 V
Storage temperature range, T_{stg} . . . . . –55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to $V_{SS1} = V_{SS2} = 0$ V.
2. Power up in the following order: V_{DD2}, control inputs, V_{DD1}, GAM1-16. Power down by reversing the sequence.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD1}	8.5		13.5	V
	V_{DD2}	2.5		3.6	
Gamma correction potential (see Note 3)	$V_{GMA(1-8)}$	1/2 V_{DD1}		V_{DD1} – 0.3	V
	$V_{GMA(9-16)}$	V_{SS1} + 0.3		1/2 V_{DD1}	
Clock frequency, f_{clk}	2.5 V ≤ V_{DD2} < 3.6 V			55	MHz
Load capacitance for outputs, C_L				100	pF
Operating free-air temperature, T_A		–55		125	°C

NOTE 3: The relative magnitudes of the reference potentials are as follows: [n = 1-15] V_{DD1} > GMA1, GMAn ≥ GMAn+1, GMA16 > V_{SS1}

electrical characteristics over recommended operating conditions (unless otherwise noted), V_{SS1}, V_{SS2} = 0 V

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High level input voltage	Dx0–Dx7, LK, TP1, LP, RS, EIO1, EIO2, L/R, REV1, REV2, POL, SHC		0.7 V_{DD2}			V
V_{IL}	Low level input voltage	Dx0–Dx7, LK, TP1, LP, RS, EIO1, EIO2, L/R, REV1, REV2, POL, SHC				0.25 V_{DD2}	V
I_{lkg}	Input leakage current	Dx0–Dx7, LK, TP1, LP, RS, EIO1, EIO2, L/R, REV1, REV2, POL, SHC		–1		1	µA
$I_{(CHG)}$	Output current (RS = L) (see Note 4)	OUT1–384	$V_{O(X)} = V_{DD1} – 0.3$ V, $V_O = V_{O(X)} – 1.0$ V		–100	–30	µA
$I_{(DIS)}$			$V_{O(X)} = V_{SS1} + 0.3$ V, $V_O = V_{O(X)} + 1.0$ V	30	100		
ΔV_O	Deviation between output voltage pins (see Note 5)	OUT1–384	$V_O = V_{DD1} – 0.3$ V to $V_{DD1} – 0.35$ V	–20	±10	20	mV
			$V_O = V_{SS1} + 0.3$ V to $V_{SS1} + 0.35$ V				
ΔV_{AV}	Average output variation (see Note 6)	OUT1–384	$V_O = V_{DD1} – 0.3$ V to $V_{DD1} – 2.0$ V	–15	±15	15	mV
			$V_O = V_{SS1} + 2.0$ V to $V_{SS1} + 0.3$ V				
$R_{(GMA)}$	Resistance between reference power supplies	GMA1–GMA8 GMA9–GMA16			5600		Ω
$I_{(DD1)}$	Supply current (during operation)	Analog section	TP1 interval = 20 µs, f_{CLK} = 36 MHz, No load, V_{DD1} = 13.5 V, Black raster test pattern, GMA1 = 13.2 V, GMA16 = 0.3 V		10	22	mA
$I_{(DD1)}$	Supply current (during standby)		No load, V_{DD1} = 13.5 V, Black raster test pattern, GMA1 = 13.2 V, GMA16 = 0.3 V, Clock and input signal are in the stopped state		9.6	18	
$I_{(DD2)}$	Supply current (during operation)	Digital section	TP1 interval = 20 µs, f_{CLK} = 36 MHz, Checkered dot test pattern		1.9	5	
$I_{(DD2)}$	Supply current (during standby)		Clock and input signal are in the stopped state.			100	µA

† All typical values are at V_{SS1}, V_{SS2} = 0 V and T_A = 25°C.

NOTES: 4. $V_{O(X)}$ is the output voltage of OUT1–OUT384. V_O is the voltage impressed at OUT1–OUT384.
5. This is the deviation between terminals with differences in positive and negative amplitudes, when all chip outputs display the same data.
6. This is the inter-chip variation in the average of the output voltage inter-pin deviation (ΔVo).
7. V_O is the output voltage of analog output terminals OUT1–OUT384.

timing requirements over recommended operating free-air temperature range, V_{DD2} = 2.5 V to < 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{c1}	CLK cycle time	See Figure 3	18			ns
t_{w1}	High-level CLK pulse width duration	See Figure 3	4			ns
t_{w2}	Low-level CLK pulse width duration	See Figure 3	4			ns
t_{su1}	Data/REV setup time	See Figure 3	4			ns
t_{h1}	Data/REV hold time	See Figure 3	0			ns
t_{su2}	Start pulse setup time	See Figure 3	4			ns
t_{h2}	Start pulse hold time	See Figure 3	0			ns
t_{d1}	Start pulse signal delay time	See Figure 3			10	ns
t_{d2}	LCD drive signal delay time	See Figure 3 and Notes 8 and 10			5	µs
t_{d3}		See Figure 3 and Notes 9 and 10			10	µs
t_{su3}	TP1 signal E10 (input) setup time	See Figure 3	70			ns
t_{h3}	TP1 low hold time from final data CLK	See Figure 3	1			CLK cycle
t_{w3}	High-level TP1 signal pulse width duration	See Figure 3	1.5			µs
t_{su4}	POL signal TP1 setup time	See Figure 3	–5			ns
t_{h4}	POL signal TP1 hold time	See Figure 3	6			ns
t_{h5}	SHC hold time	See Figure 4	4.5			µs
t_{su5}	SHC setup time	See Figure 4	4.5			µs

NOTES: 8. Specified as the value at which the driver's output voltage reaches the target output voltage ±(V_{DD1} x 0.1).
9. Specified as the value at which the driver's output voltage reaches the target output voltage (8-bit precision).
10. The load of the analog output terminal is the value shown in Figure 7.

PARAMETER MEASUREMENT INFORMATION

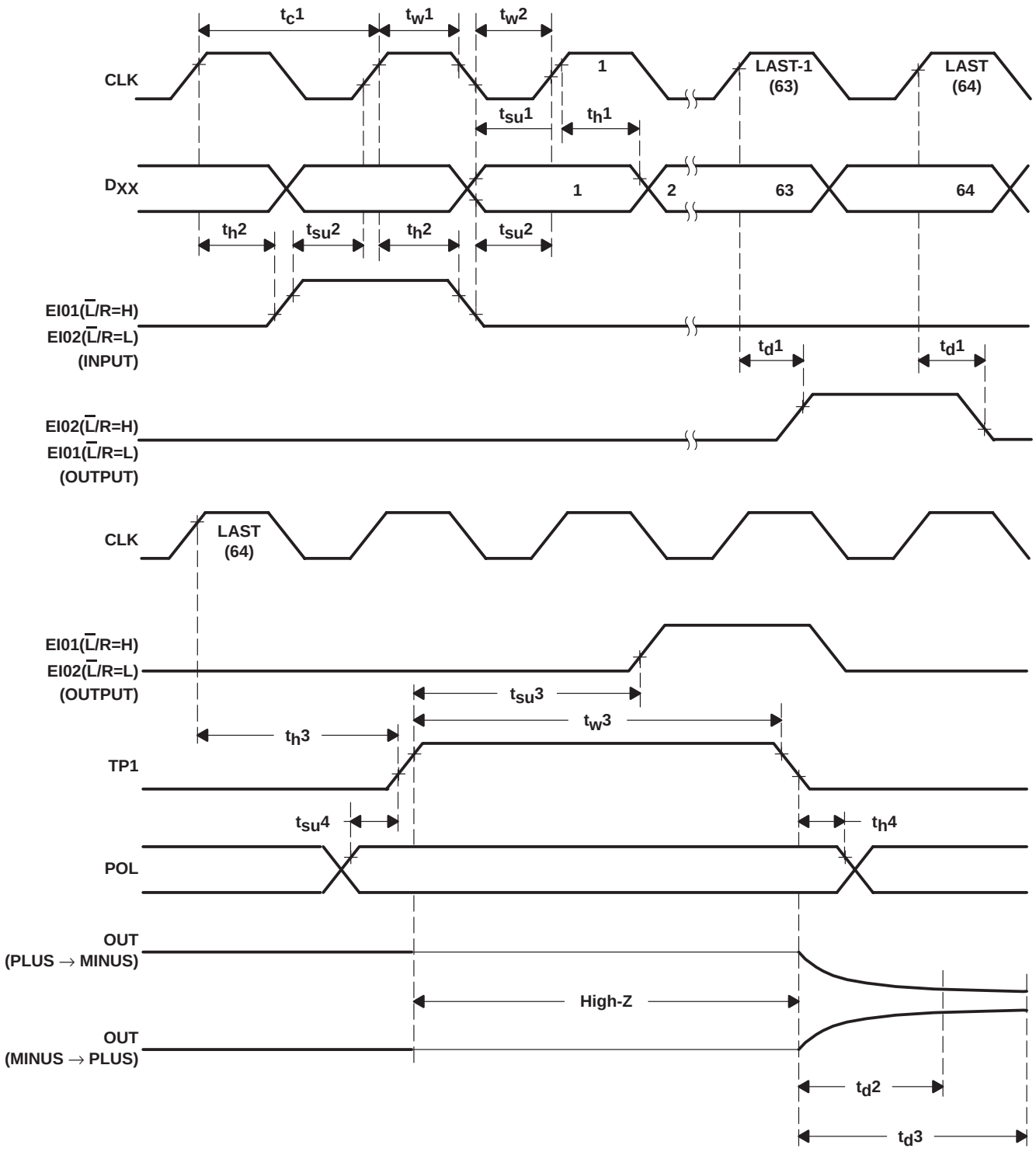


Figure 3. Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

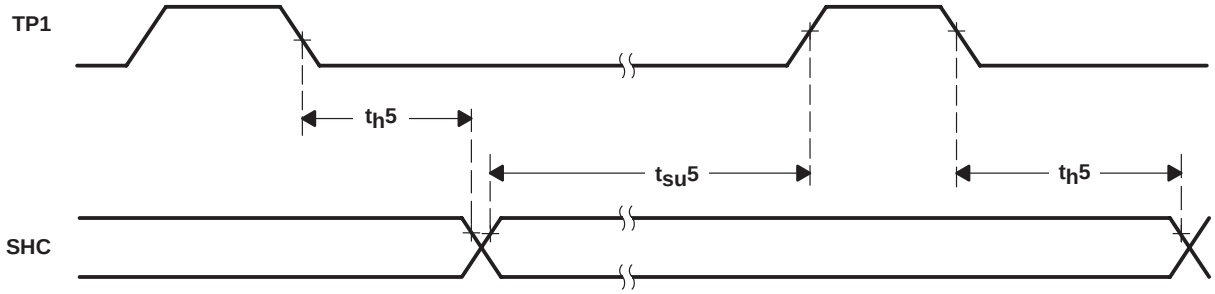


Figure 4. SHC Timing Waveforms

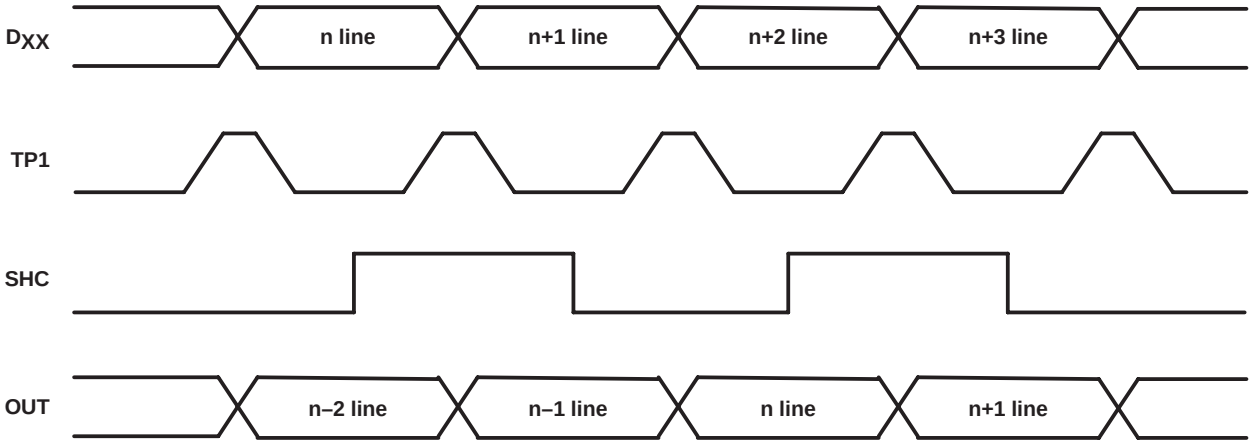


Figure 5. Relationship Between Input Data and Output

PARAMETER MEASUREMENT INFORMATION

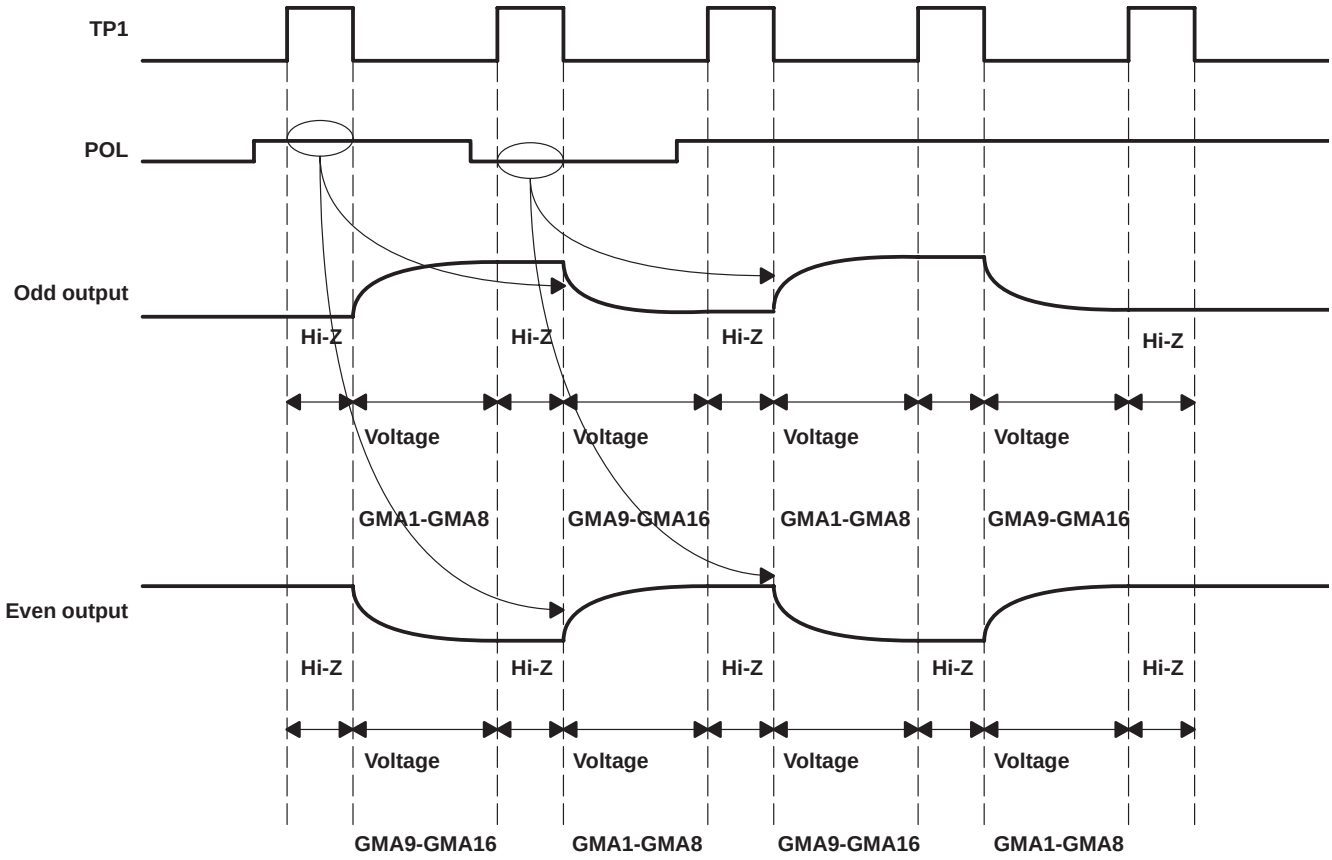
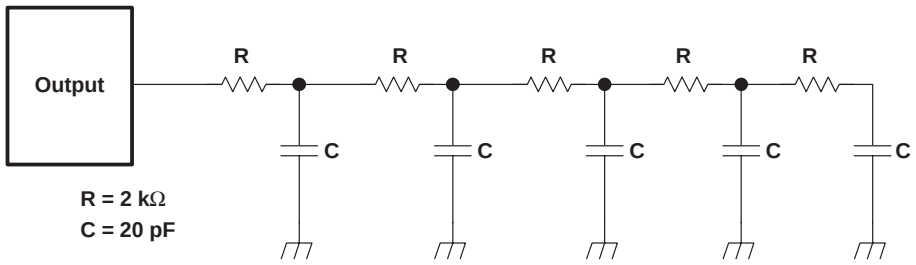


Figure 6. Relationship Between TP1 Signal (Latch Input Terminal), POL Signal (Polarity Reversal), and Outputs



NOTE: The loads of the analog output terminals (OUT1–OUT384) are per the above. However, the load circuit value may vary.

Figure 7. Load Circuit

APPLICATION INFORMATION

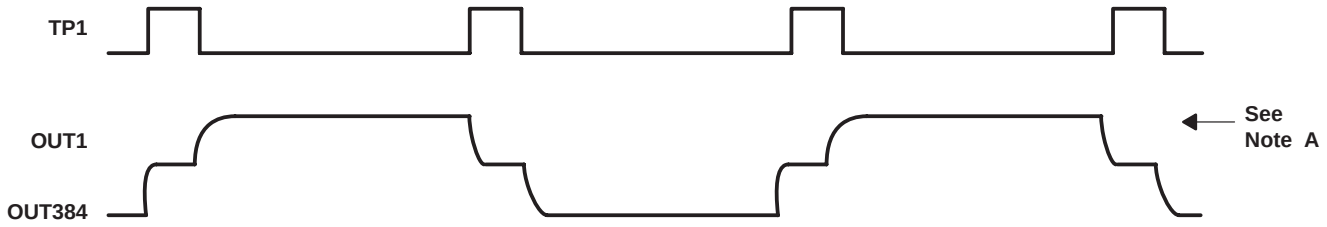
MPT57571 low power mode

The MPT57571 has a low power mode to reduce current consumption. This mode reduces charge and discharge currents to the load by redistributing the charge stored in the load. This makes efficient, low power consumption operation possible.

low power mode operation

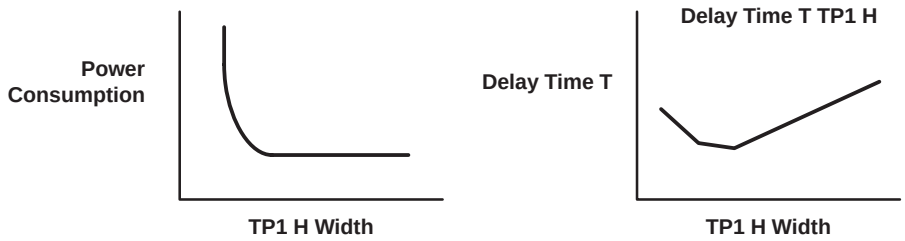
When the low power mode is selected and TP1 = H, all the outputs from OUT1 through OUT384 are shorted within the driver. In this case, each buffer amp that drives an output is in an isolated state.

low power mode output waveform

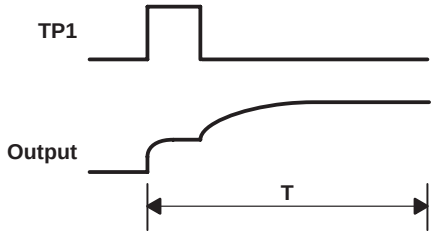


NOTE A: When TP1 = H, the electric potential becomes a fraction of the previous output potential immediately before it was averaged out by the output capacity. As an example, when a positive polarity output and a negative polarity output each have the same output channel, this is considered to be a symmetrical potential with a reference of 1/2 V_{DD1}, and all capacity values connected to the output are equal: when TP1 = H, all outputs are 1/2 V_{DD1}.

TP1 H width relationship with power and ac characteristics



Consumption power and delay time T change with the width of TP1 H, as shown in the previous figure; these characteristics also change with the load connected to the output. Therefore, with TP1 H width, it is necessary to select the optimal delay time for the load.



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