MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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by MRFIC1806/D

The MRFIC Line

1.8 GHz PA Driver/Ramp

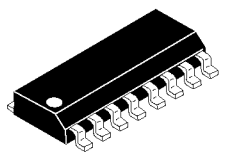
Designed primarily for use in DECT, Japan Personal Handy System (PHS), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1806 includes a two stage driver amplifier and transmit waveform shaping circuitry in a low–cost SOIC–16 package. The amplifier portion employs depletion mode power GaAs MESFETs to produce +21 dBm output with 0 dBm input. The ramping circuit controls the burst–mode transmit rise and fall time and is adjustable through external components. This circuitry also places the amplifier in standby during TDMA receive mode. The MRFIC1806 is sized to drive the MRFIC1807 PA/Switch.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2500 MHz
- 23 dB Typical Gain
- +21 dBm Typical 1.0 dB Compression
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 Volt Supply
- Low Cost Surface Mount Plastic Package
- Order MRFIC1806R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1806

MRFIC1806

1.8 GHz DRIVER AMPLIFIER AND RAMP CIRCUIT GaAs MONOLITHIC INTEGRATED CIRCUIT



**CASE 751B–05
(SO–16)**

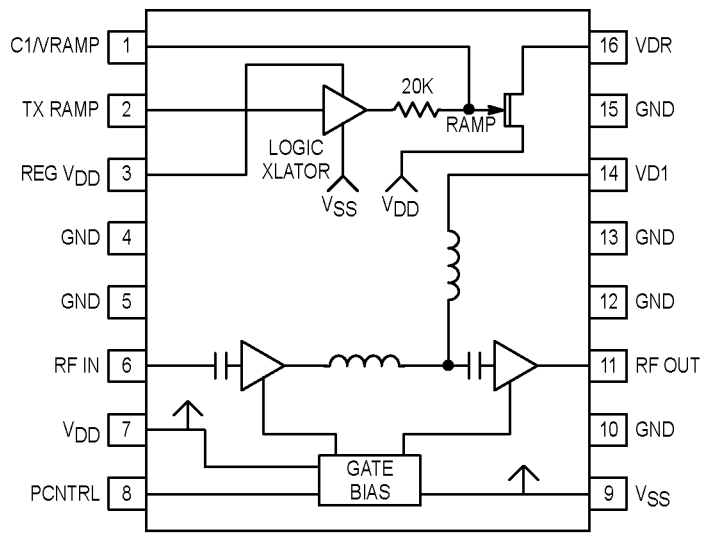


Figure 1. Pin Connections and Functional Block Diagram

REV 2

MOTOROLA

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Supply Voltage	V_{SS}	–4.0	Vdc
Supply Voltage	REG V_{DD}	4.5	Vdc
Bias Control Voltage	PCNTRL	3.0	Vdc
RF Input Power	P_{IN}	10	dBm
Ramp Circuit Input Voltage (High)	TX RAMP	6.0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Ambient Operating Temperature	T_A	–10 to +70	°C
Thermal Resistance, Junction to Case	θ_{JC}	100	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.5–2.5	GHz
Supply Voltage	V_{DD}	3.0 to 5.0	Vdc
Supply Voltage	V_{SS}	–2.75 to –2.25	Vdc
Supply Voltage	REG V_{DD}	2.9 to 3.1	Vdc
Bias Control Voltage	PCNTRL	0.5 to 1.5	Vdc
RF Input Power	P_{IN}	–20 to +5	dBm
Transmit Burst Enable Voltage (High)	TX RAMP	2.8 to 3.5	Vdc
Transmit Burst Enable Voltage (Low)	TX RAMP	–0.2 to +0.2	Vdc

ELECTRICAL CHARACTERISTICS

DECT Application with Internal Logic Translator (See Figure 2. V_{DD} = 3.5 V, REG V_{DD} = 3.0 V, T_A = 25°C, V_{SS} = –2.5 V, TX RAMP = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = –3.0 dBm @ 1.9 GHz unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = –7.0 dBm)	21	23	—	dB
Input Return Loss	—	12	—	dB
Reverse Isolation	—	36	—	dB
Output Power	18	19.5	—	dBm
Harmonic Output	—	–36	—	dBc
Output Third Order Intercept	—	33	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.35	0.6	mA
Supply Current, I_{DD} (Pin 7)	—	115	135	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.6	0.9	mA
Ramp Circuit Dynamic Range	40	44	—	dB

STANDBY MODE (TX RAMP = 0 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	–25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.25	0.4	mA

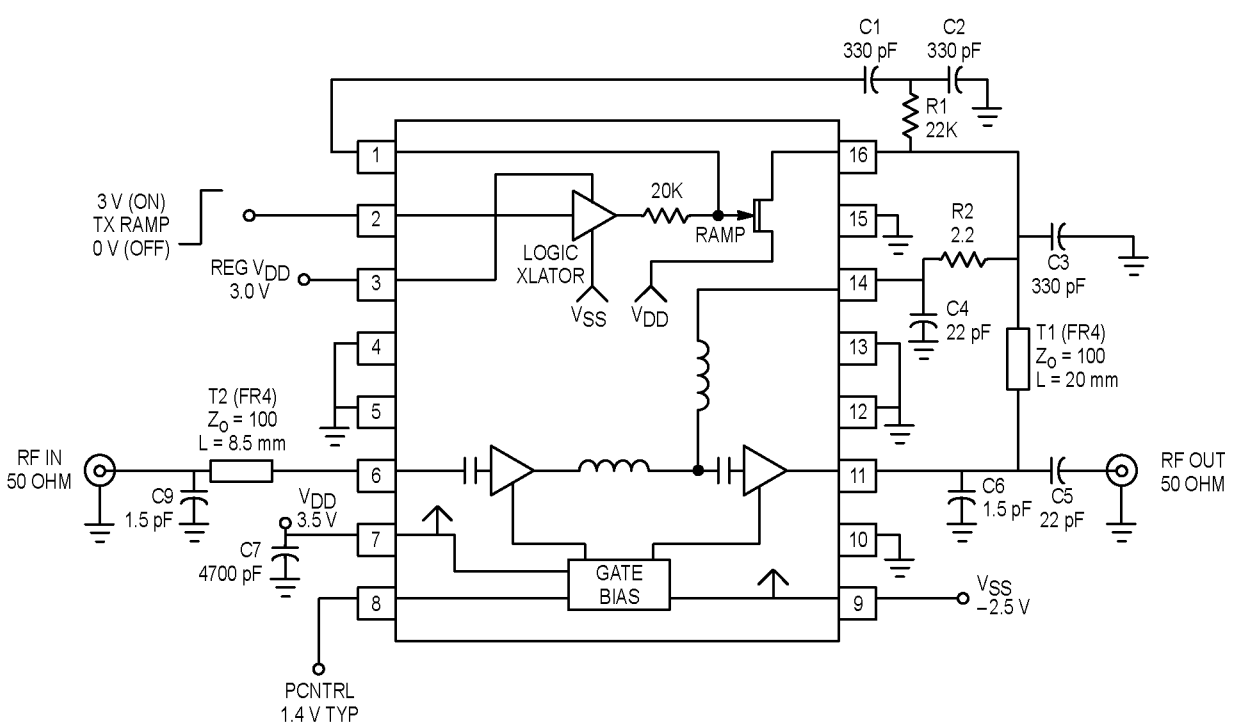


Figure 2. Applications Circuit Details for DECT using Internal Logic Translator

ELECTRICAL CHARACTERISTICS

General Application without Internal Logic Translator (See Figure 3. V_{DD} = 3.5 V, REG V_{DD} (Pin 2) open, V_{SS} = –2.5 V, TX RAMP (Pin 2) grounded, V_{RAMP} = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = 0 dBm @ 1.9 GHz, T_A = 25°C unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = –7.0 dBm)	21	23	—	dB
Output Power (P_{IN} = 0 dBm)	20	22	—	dBm
Output Power (P_{IN} = +4.0 dBm)	—	23	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.3	0.5	mA
Supply Current, I_{DD} (Pin 7)	—	130	145	mA

STANDBY MODE (V_{RAMP} = –2.4 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	–25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA

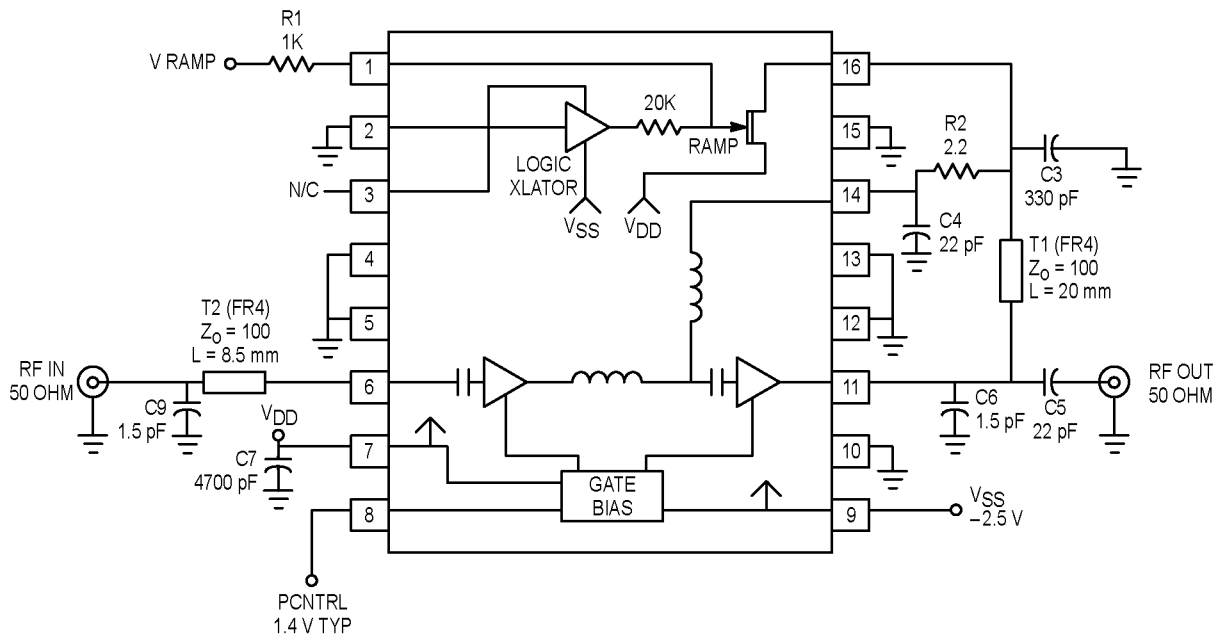


Figure 3. 1.9 GHz General Application Circuit Details (Internal Translator Disabled)

Table 1. Small Signal S–Parameters

(V_{DD} = 3.5 V, I_{DQ} = 120 mA, T_A = 25°C, no matching circuit, reference plane at pins 6 and 11.)

	S_{11}		S_{21}		S_{12}		S_{22}	
Freq (GHz)	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.734	–76.8	13.11	–87.9	0.009	–176	0.278	–98.9
1.6	0.654	–82.4	13.01	–109.4	0.012	178	0.326	–116.4
1.7	0.620	–72.6	11.17	–117.4	0.011	152	0.344	–109.8
1.8	0.636	–79.8	12.25	–137.0	0.014	170	0.423	–134.1
1.9	0.607	–80.6	10.77	–151.3	0.017	169	0.421	–147.7
2.0	0.592	–79.4	10.88	–165.1	0.019	163	0.427	–161.8
2.1	0.581	–79.4	9.64	–174.9	0.024	163	0.432	–172.3
2.2	0.571	–78.9	9.30	174.1	0.026	158	0.429	178.8
2.3	0.560	–79.1	7.95	166.9	0.029	157	0.432	171.1
2.4	0.541	–79.8	7.80	155.7	0.033	153	0.442	164.6
2.5	0.521	–80.1	6.90	147.2	0.042	154	0.445	161.7

DESIGN AND APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC1806 is designed to drive the MRFIC1807 Power Amplifier and Transmit/Receive Switch IC in Personal Communications System (PCS) applications such as Europe's DECT and Japan's Personal Handy System (PHS). The design incorporates not only a two–stage GaAs MESFET driver/exciter amplifier, but also externally controllable bias and ramping circuitry. The IC is designed to drive the MRFIC1807 with about +19 dBm which will, in turn, produce +26 dBm output, suitable for DECT. To reduce chip size (and cost) and to allow for flexibility of application, the amplifier has limited on–chip matching. The ramp circuitry is used to shape the drain voltage to the FETs for Time Domain Multiple Access (TDMA) applications and is comprised of a depletion mode pass device driven by a logic translator. Attack and release times are controllable through the use of external components. The IC is configured such that all, part or none of the ramping circuitry can be used, depending on the application.

AMPLIFIER CIRCUIT APPLICATION

As can be seen in Figures 2 and 3, the off–chip matching is straight forward. At frequencies near 1.9 GHz, the input requires 4.7 nH in series and 1.5 pF in shunt. The 4.7 nH series inductance may be implemented with a high–impedance transmission line as shown. The output, being close to 25 Ω, requires only a shunt 1.5 pF capacitor. Drain voltage for stage 1 is supplied through pin 14 and for stage 2 through pin 11, the RF output. Pin 8, PCNTRL is used to set the quiescent bias point for both stages. While nominal I_{DDQ} is 120 mA, it can be set as high as 180 mA for better linearity or lower for better efficiency. 120 mA is a good compromise for DECT and PHS. DECT, which employs GMSK constant envelope modulation can use RF amplifiers close to or in saturation without experiencing spectral regrowth of the signal. PHS, on the other hand, employs π/4 DQPSK modulation which has some residual AM associated with the encoding. With AM present, RF amplifiers must be backed off from saturation so as not to regrow the filtered sidebands. The MRFIC1806 has plenty of backoff capability for PHS where the MRFIC1807 PA/switch must only produce about +21 dBm. With the 8.0 dB gain of the MRFIC1807, the MRFIC1806 need only produce +13 dBm output so the bias point can be reduced below the 120 mA suggested for DECT.

As with all RF circuits, board layout and grounding are important. All RF signal paths must be controlled impedance structures. RF chip components must be high quality. Bypassing capacitors must be close to the IC and to ground vias. Pins which are designated as ground connections must be as close as possible to ground vias.

RAMPING CIRCUIT OPTIONS

The on–chip ramp circuit can be used to control the amplifier attack and release time for DECT applications through the use of a few external components as shown in Figure 2. This ramping is required to control the burst signal rise and fall time to avoid adjacent channel interference. At the same time, system specifications require the transmitter to reach full power in a minimum time. For DECT, it has been shown that a rise time of not greater than 2 microseconds will produce acceptable adjacent channel performance. The system requires full power in not greater than 10 microseconds. A good compromise, and the timing implemented in Figure 2, is 7 microseconds.

The on–chip logic translator can be bypassed as shown in Figure 3 by applying a ramp voltage to Pin 1 through a 1.0 kΩ resistor. This configuration allows flexibility in ramping the amplifier. The regulated V_{DD} voltage is not required so current consumption can be reduced. –2.3 V at Pin 1 turns the pass transistor, and the amplifier, off while a positive voltage will turn the pass transistor on. For full on state it is recommended that V_{RAMP} be close to V_{DD}. V_{RAMP} can also be used to on–off key the amplifier for simple telemetry applications or as transmit/receive control.

For more complex modulation schemes such as π/4 DQPSK used in PHS, burst ramping can be implemented with the burst mode logic. Referring to Figure 3, the V_{RAMP} voltage should be set to V_{DD} to leave the pass transistor on. The on–chip pass transistor can also be bypassed and V_{DD} applied to Pins 11 and 14.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

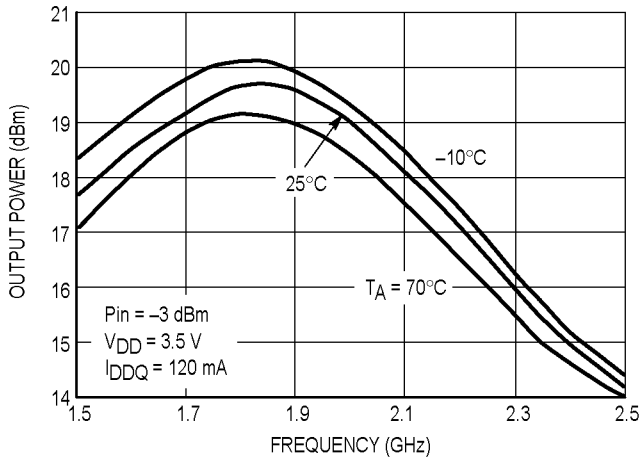


Figure 4. Output Power versus Frequency With Internal Logic Translator

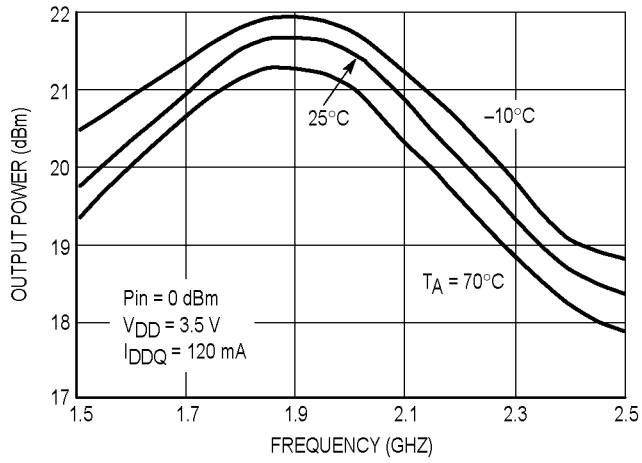


Figure 5. Output Power versus Frequency Without Internal Logic Translator

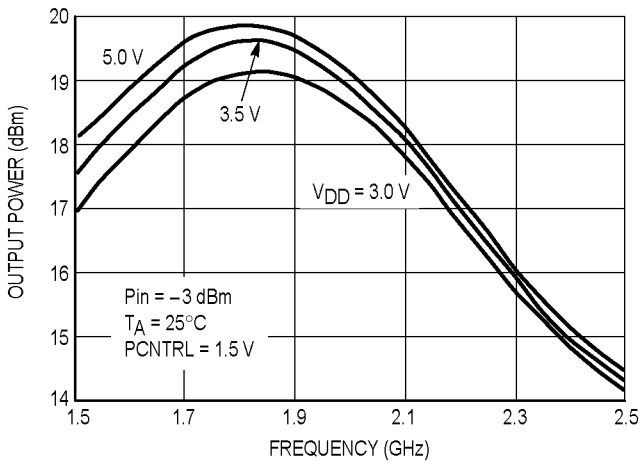


Figure 6. Output Power versus Frequency With Internal Logic Translator

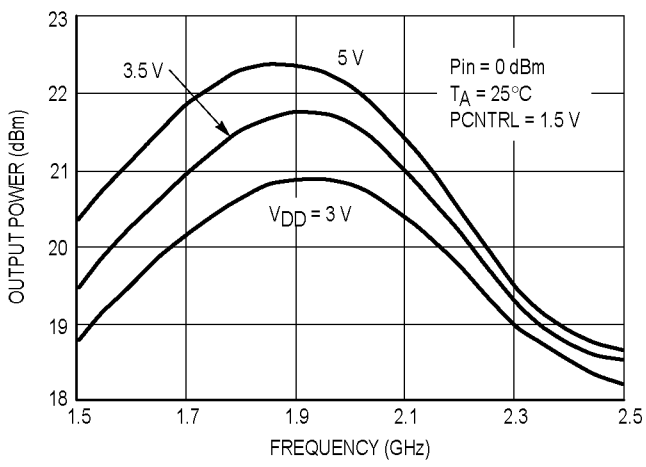


Figure 7. Output Power versus Frequency Without Internal Translator

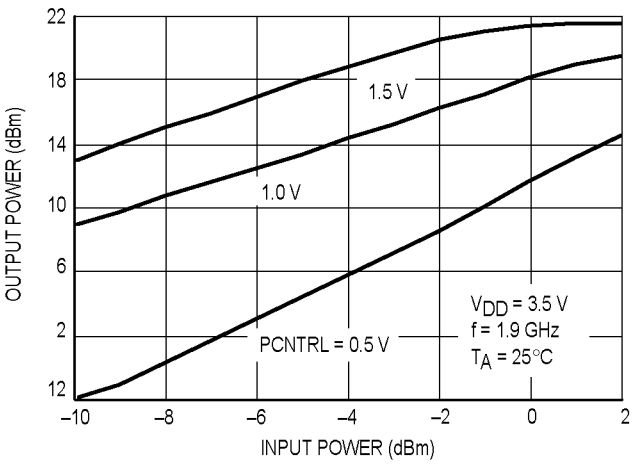


Figure 8. Output Power versus Input Power With Internal Logic Translator

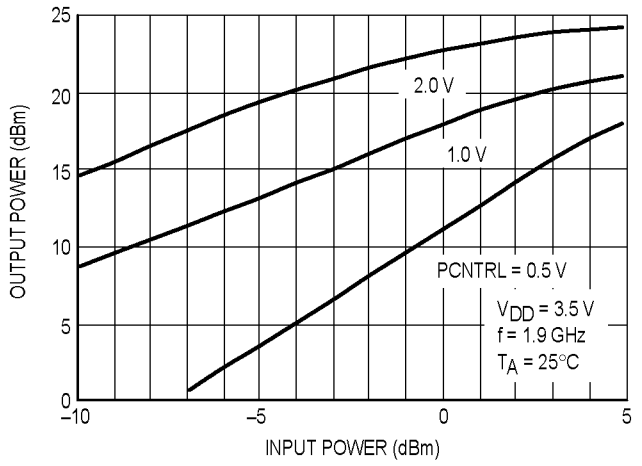


Figure 9. Output Power versus Input Power Without Internal Logic Translator

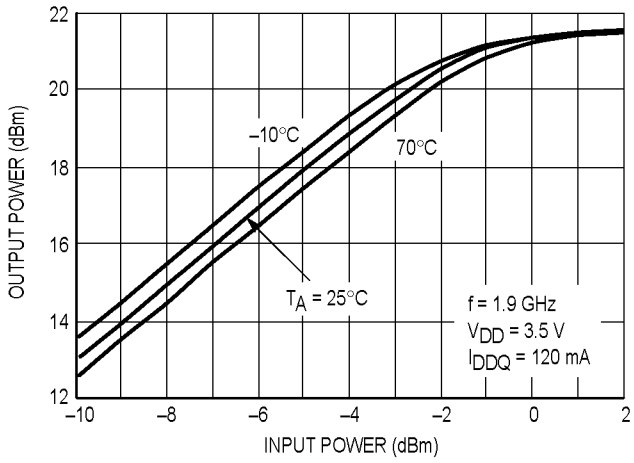


Figure 10. Output Power versus Input Power With Internal Logic Translator

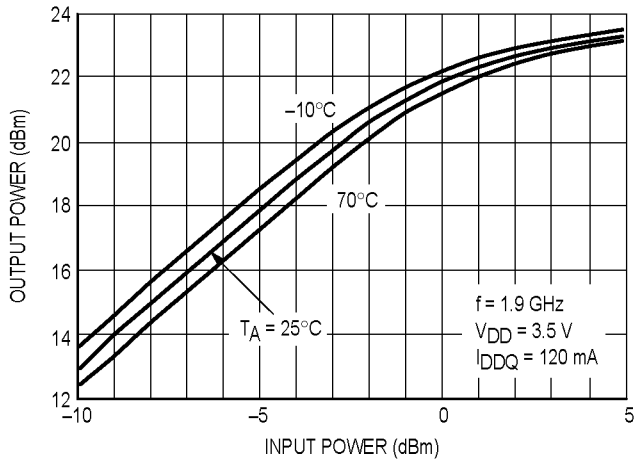


Figure 11. Output Power versus Input Power Without Internal Logic Translator

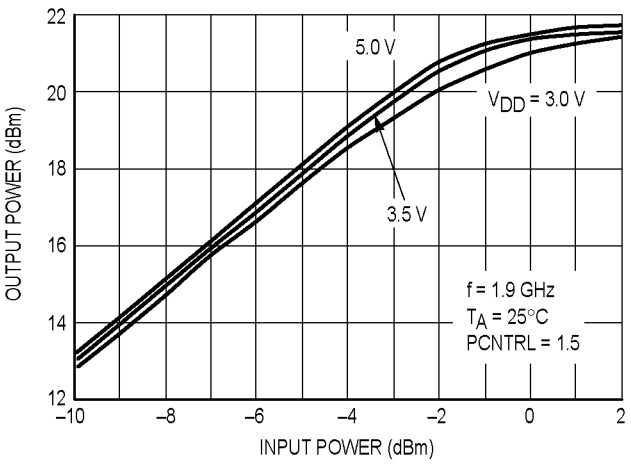


Figure 12. Output Power versus Input Power With Internal Logic Translator

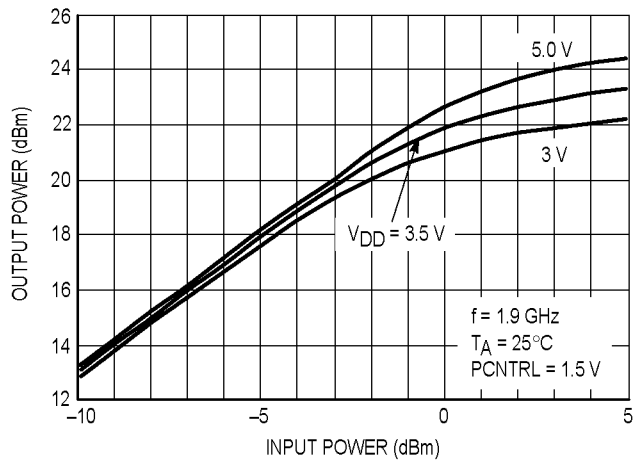


Figure 13. Output Power versus Input Power Without Internal Logic Translator

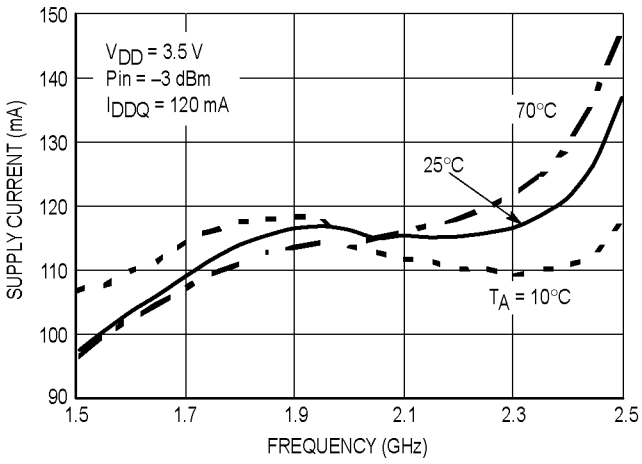


Figure 14. Supply Current versus Frequency With Internal Logic Translator

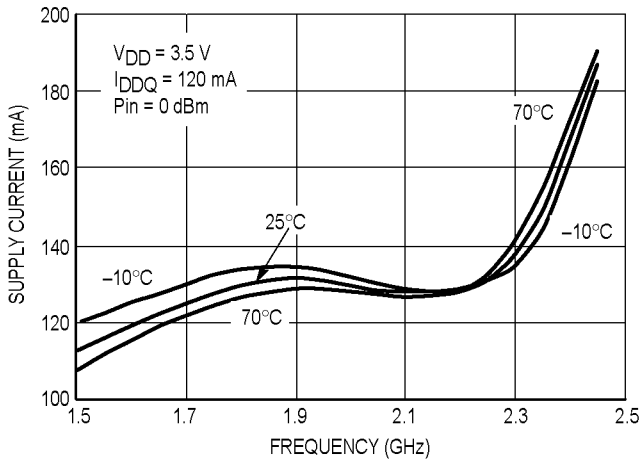


Figure 15. Supply Current versus Frequency Without Internal Logic Translator

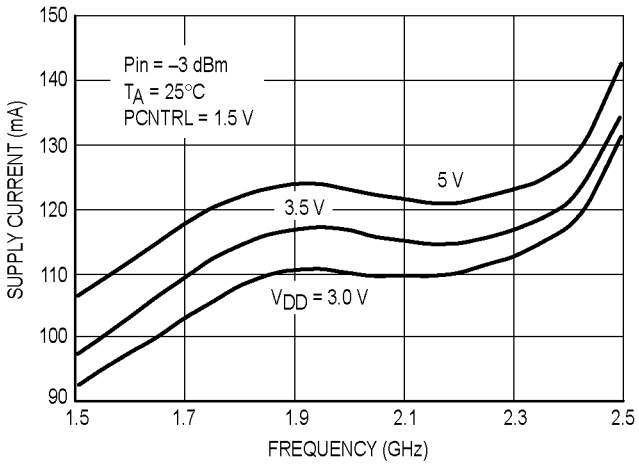


Figure 16. Supply Current versus Frequency With Internal Logic Translator

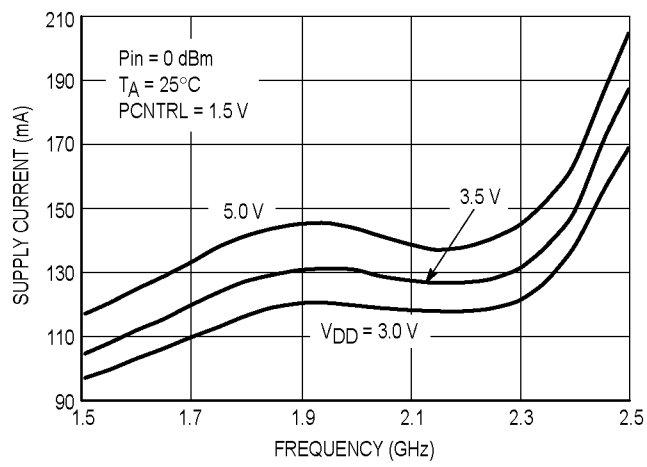


Figure 17. Supply Current versus Frequency Without Internal Logic Translator

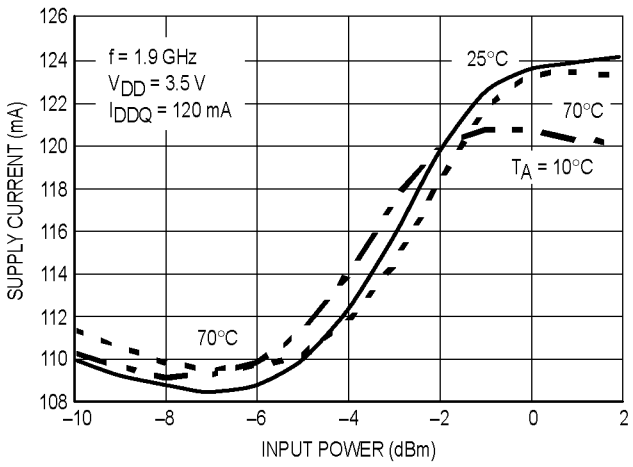


Figure 18. Supply Current versus Input Power With Internal Translator

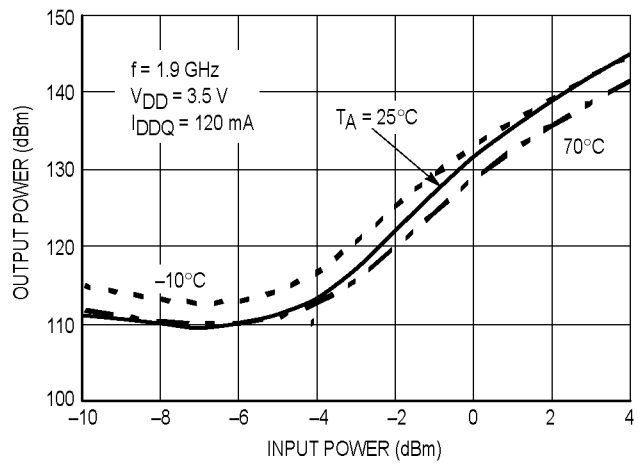


Figure 19. Supply Current versus Input Power Without Internal Translator

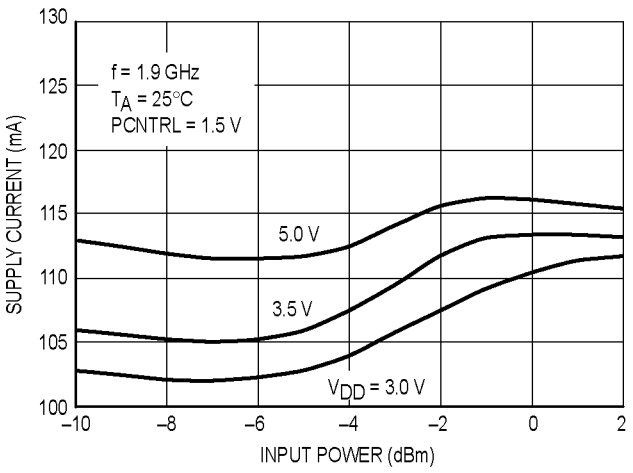


Figure 20. Supply Current versus Input Power With Internal Translator

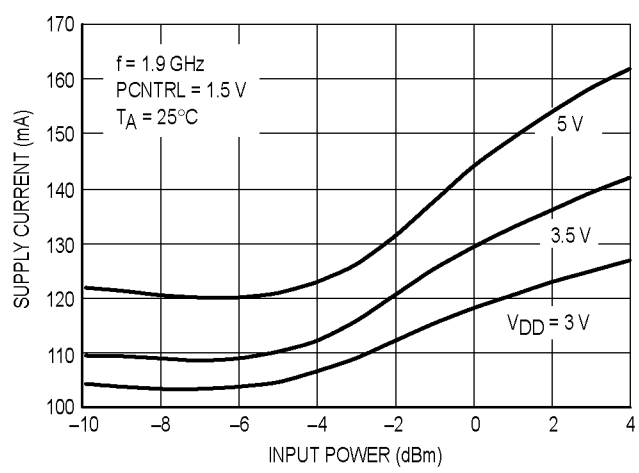


Figure 21. Supply Current versus Input Power Without Internal Logic Translator

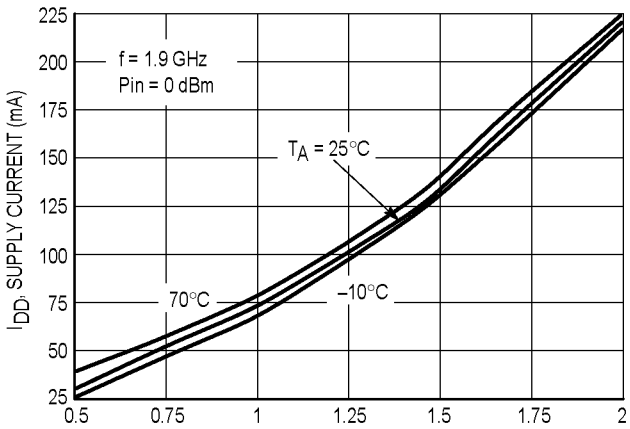


Figure 22. Supply Current versus PCNTRL Without Internal Logic Translator

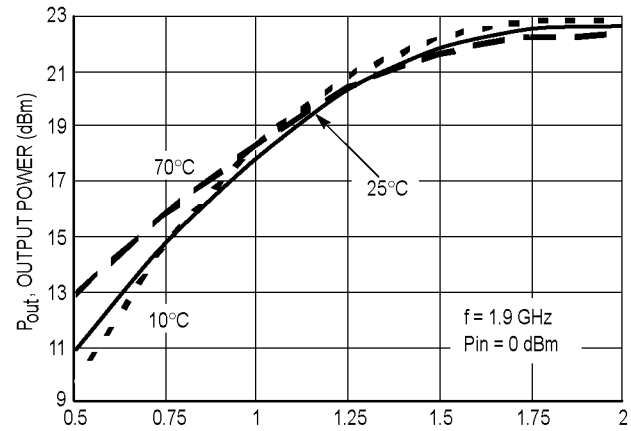


Figure 23. P_{out} versus PCNTRL Without Internal Logic Translator

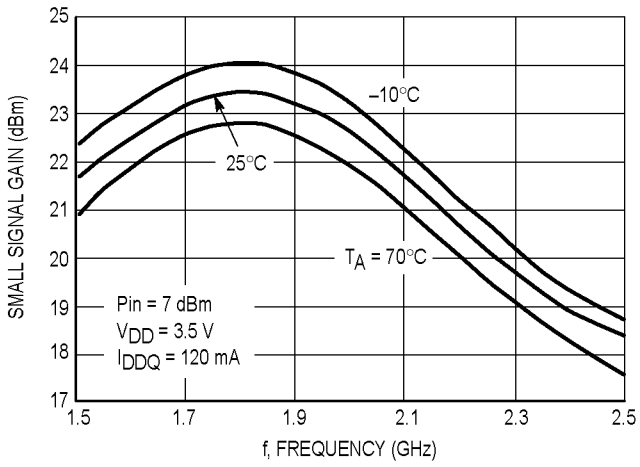


Figure 24. Small Signal Gain versus Frequency With Internal Logic Translator

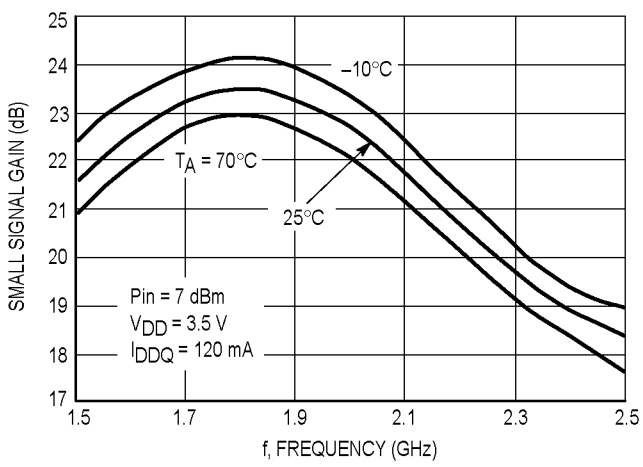


Figure 25. Small signal Gain versus Frequency Without Internal Logic Translator

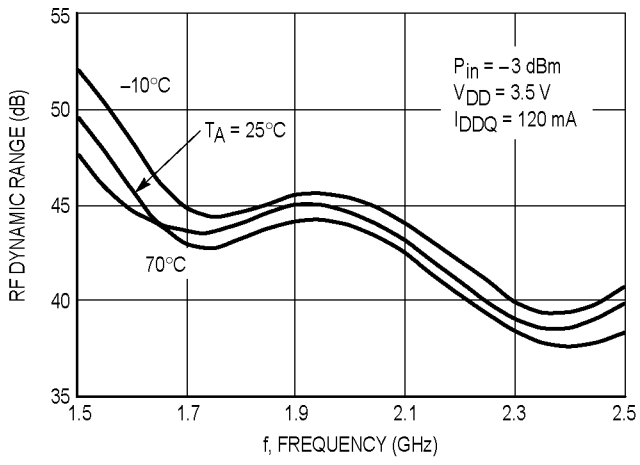


Figure 26. Dynamic Range versus Frequency With Internal Logic Translator

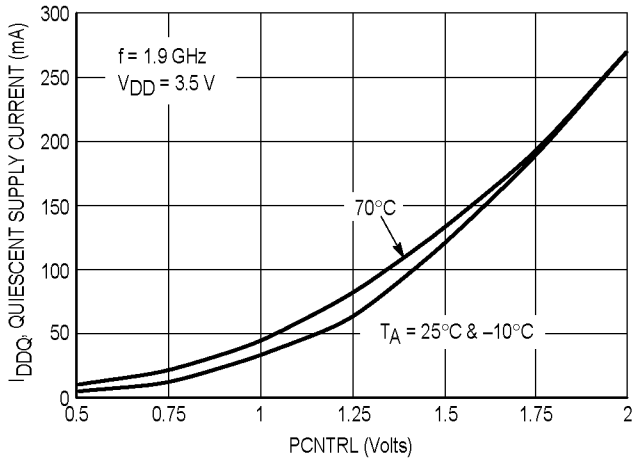


Figure 27. Quiescent Supply Current versus PCNTRL With Internal Logic Translator

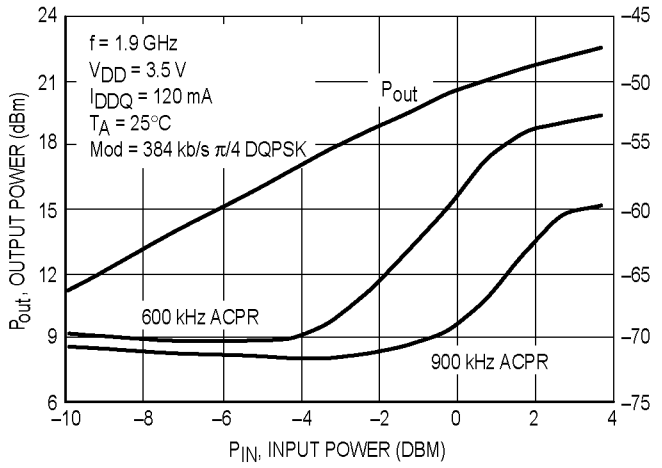


Figure 28. Output Power and Adjacent Channel Power Ratio versus Input Power Without Internal Logic Translator

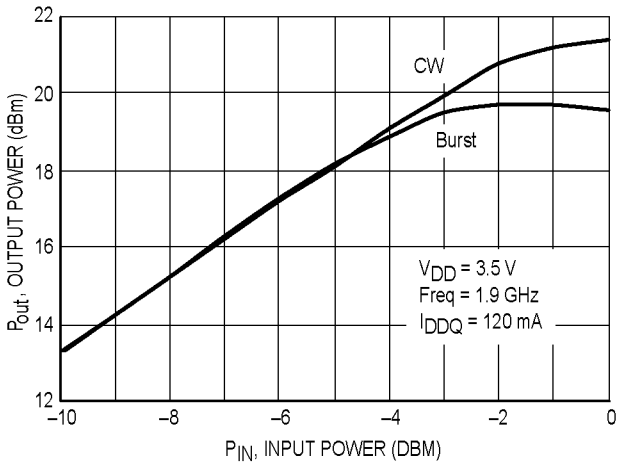
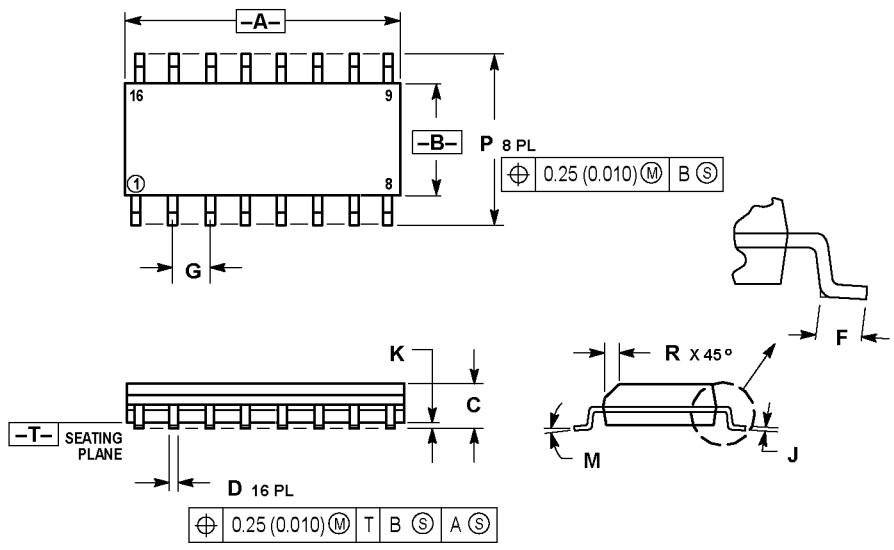


Figure 29. Continuous and Burst Mode Output Power versus Input Power With Internal Logic Translator

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
ISSUE J

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