

MSC2301YS9/KS9

65,536 BY 9 BIT DYNAMIC RAM MODULE

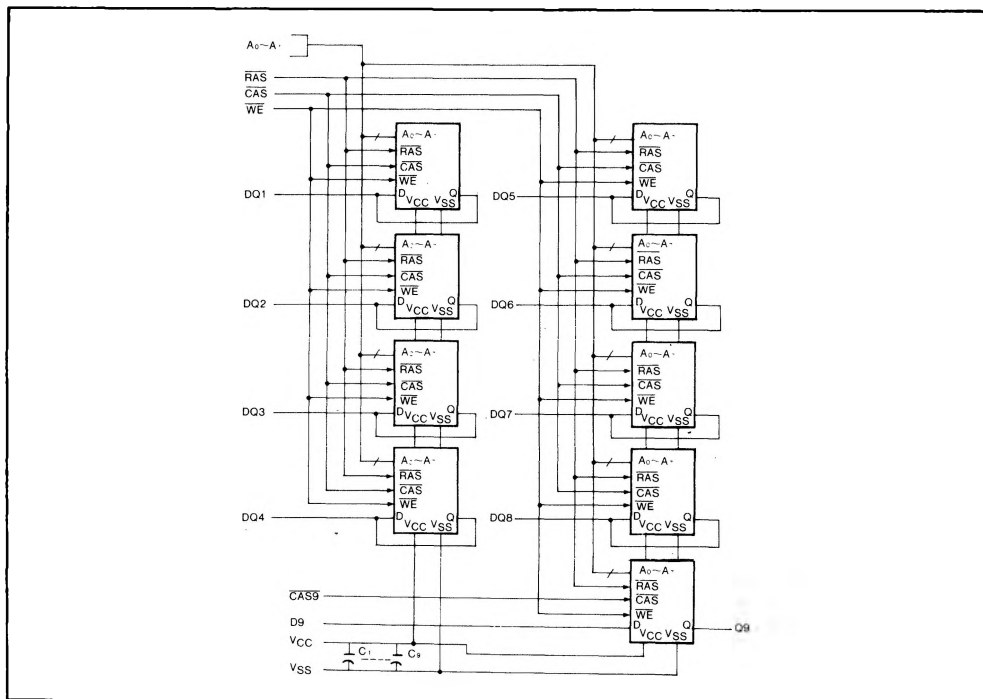
GENERAL DESCRIPTION

The Oki MSC2301YS9/KS9 is a fully decoded, 65,536 words \times 9 bit NMOS dynamic random access memory composed of nine 64K DRAMs in plastic leaded chip carrier. The mounting of nine PLCCs together with nine $0.2\mu\text{F}$ decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2301YS9/KS9 are quite same as the original MSM3764A; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

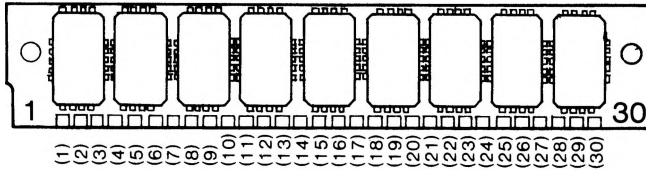
- 65,536 word \times 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 2ms (128 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common CAS Control for Eight Common Data-In and Data-Out Lines
- Separate CAS Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
 - 120ns max. (MSC2301-12YS9/KS9)
 - 150ns max. (MSC2301-15YS9/KS9)
- Low Power Dissipation;
 - 2970mW max. (MSC2301-12YS9/KS9)
 - 2725mW max. (MSC2301-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

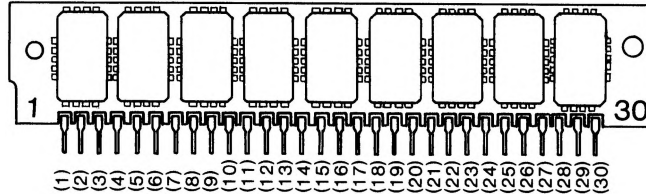


PIN ASSIGNMENT

MSC2301YS9



MSC2301KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V _{CC}	11	A4	21	$\overline{\text{WE}}$
2	CAS	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	$\overline{\text{Q9}}$
7	A2	17	NC	27	$\overline{\text{RAS}}$
8	A3	18	NC	28	CAS9
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V _{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to +7	V
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-40 to +125	°C
Power dissipation	P _D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	
Operating Current* Average power supply current (RAS, CAS cycling; $t_{RC} = \min.$)	I_{CC1}		540		495	mA
Standby Current* Power supply current (RAS = CAS = V_{IH})	I_{CC2}		45		45	mA
Refresh Current* Average power supply current (RAS cycling, CAS = V_{IH} ; $t_{RC} = \min.$)	I_{CC3}		360		360	mA
Page Mode Current* Average power supply current (RAS = V_{IL} , CAS cycling; $t_{PC} = \min.$)	I_{CC4}		450		405	mA
Input Leakage Current Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V)	I_{L1}	-90	90	-90	90	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{L0}	-10	10	-10	10	μA
Output Levels Output high voltage ($I_{OH} = -5mA$) Output low voltage ($I_{OL} = 4.2mA$)	V_{OH} V_{OL}	2.4	0.4	2.4	0.4	V V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A ₀ ~ A ₇)	C _{IN1}	40	70	pF
Input Capacitance ($\overline{\text{RAS}}$, CAS, $\overline{\text{WE}}$)	C _{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C _{DQ}	7	20	pF
Input Capacitance ($\overline{\text{CAS9}}$)	C _{IN3}	5	10	pF
Input Capacitance (D9)	C _{IN4}	4	10	pF
Output Capacitance (Q9)	C _{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Note 1, 2, 3

Parameter	Symbol	Units	MSC2301-12YS/KS		MSC2301-15YS/KS		Note
			Min.	Max.	Min.	Max.	
Refresh period	t _{REF}	ms		2		2	
Random read or write cycle time	t _{RC}	ns	220		260		
Page mode cycle time	t _{PC}	ns	120		145		
Access time from $\overline{\text{RAS}}$	t _{RAC}	ns		120		150	4, 6
Access time from $\overline{\text{CAS}}$	t _{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t _{OFF}	ns	0	35	0	40	
Transition time	t _T	ns	3	35	3	35	
$\overline{\text{RAS}}$ precharge time	t _{RP}	ns	90		100		
$\overline{\text{RAS}}$ pulse width	t _{RAS}	ns	120	10,000	150	10,000	
$\overline{\text{RAS}}$ hold time	t _{RSH}	ns	60		75		
$\overline{\text{CAS}}$ precharge time	t _{CP}	ns	50		60		
$\overline{\text{CAS}}$ pulse width	t _{CAS}	ns	60	10,000	75	10,000	
$\overline{\text{CAS}}$ hold time	t _{CSH}	ns	120		150		

AC CHARACTERISTICS (Continued)

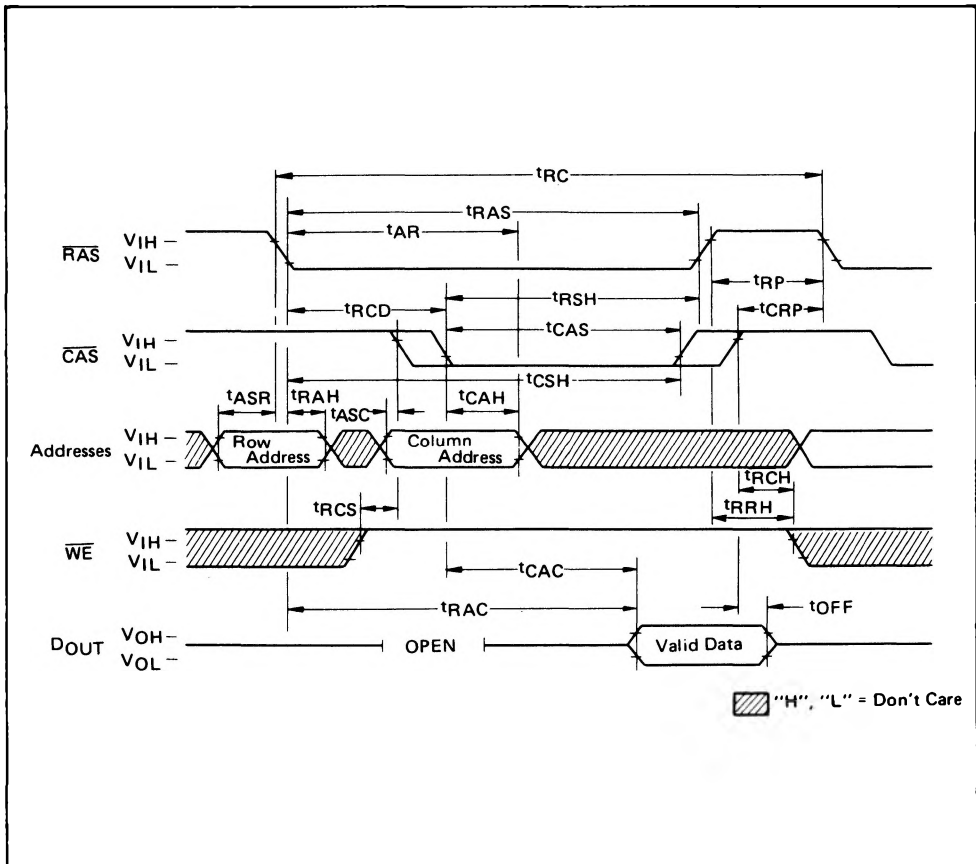
(Recommended operating conditions unless otherwise noted.)

Note 1, 2, 3

Parameter	Symbol	Units	MSC2301-12YS/KS		MSC2301-15YS/KS		Note
			Min.	Max.	Min.	Max.	
RAS to CAS delay time	t _{RCD}	ns	25	60	25	75	7
CAS to RAS precharge time	t _{CRP}	ns	0		0		
Row Address set-up time	t _{ASR}	ns	0		0		
Row Address hold time	t _{RAH}	ns	15		15		
Column Address set-up time	t _{ASC}	ns	0		0		
Column Address hold time	t _{CAH}	ns	20		20		
Column Address hold time reference to RAS	t _{AR}	ns	80		95		
Read command set-up time	t _{RCS}	ns	0		0		
Read command hold time	t _{RCH}	ns	0		0		
Write command set-up time	t _{WCS}	ns	-10		-10		
Write command hold time	t _{WCH}	ns	40		45		
Write command hold time referenced to RAS	t _{WCR}	ns	100		120		
Write command pulse width	t _{WP}	ns	40		45		
Write command to RAS lead time	t _{RWL}	ns	40		45		
Write command to CAS lead time	t _{CWL}	ns	40		45		
Data-in set-up time	t _{DS}	ns	0		0		
Data-in hold time	t _{DH}	ns	40		45		
Data-in hold time referenced to RAS	t _{DHR}	ns	100		120		

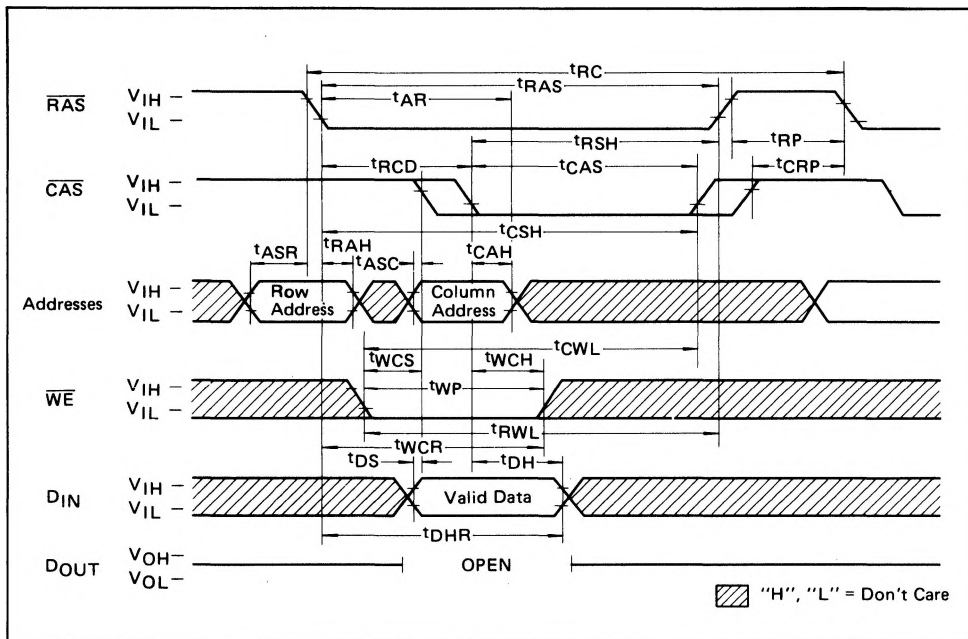
- Notes:**
- 1 An initial pause of 100 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles (Example: $\overline{\text{RAS}}$ only) before proper device operation is achieved.
 - 2 AC measurements assume at $t_T = 5$ ns
 - 3 V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL} .
 - 4 Assumes that $t_{\text{RCD}} < t_{\text{RCD}} (\text{Max.})$
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
 - 5 Assumes that $t_{\text{RCD}} < t_{\text{RCD}} (\text{Max.})$.
 - 6 Measured with a load circuit equivalent to 2TTL loads and 100 pF.
 - 7 Operation within the $t_{\text{RCD}} (\text{Max.})$ limit insures that $t_{\text{RAC}} (\text{Max.})$ can be met. $t_{\text{RCD}} (\text{Max.})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}} (\text{Max.})$ limit, then access time is controlled exclusively by t_{CAC} .

READ CYCLE TIMING



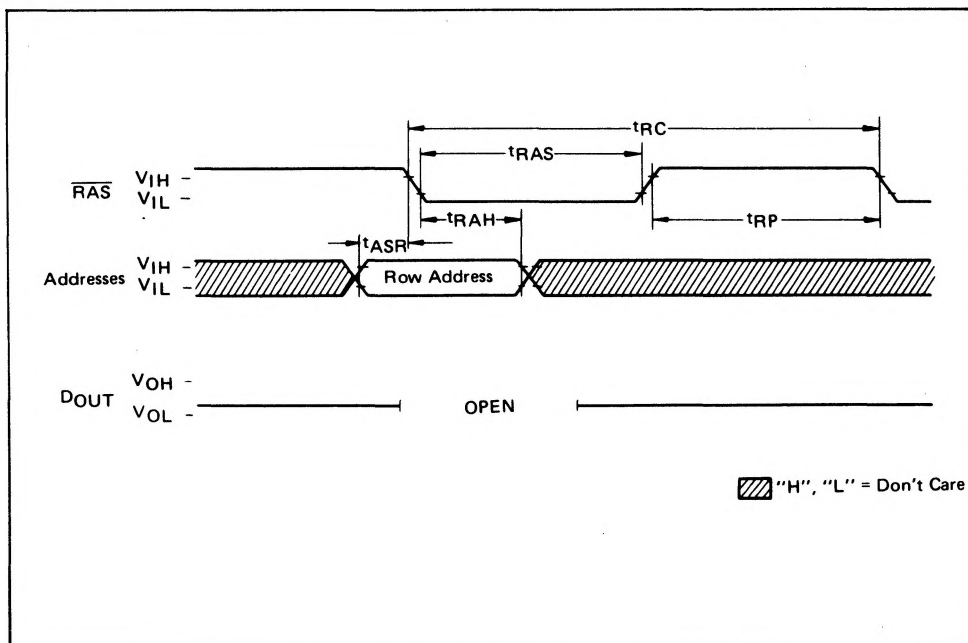
WRITE CYCLE TIMING

(EARLY WRITE)

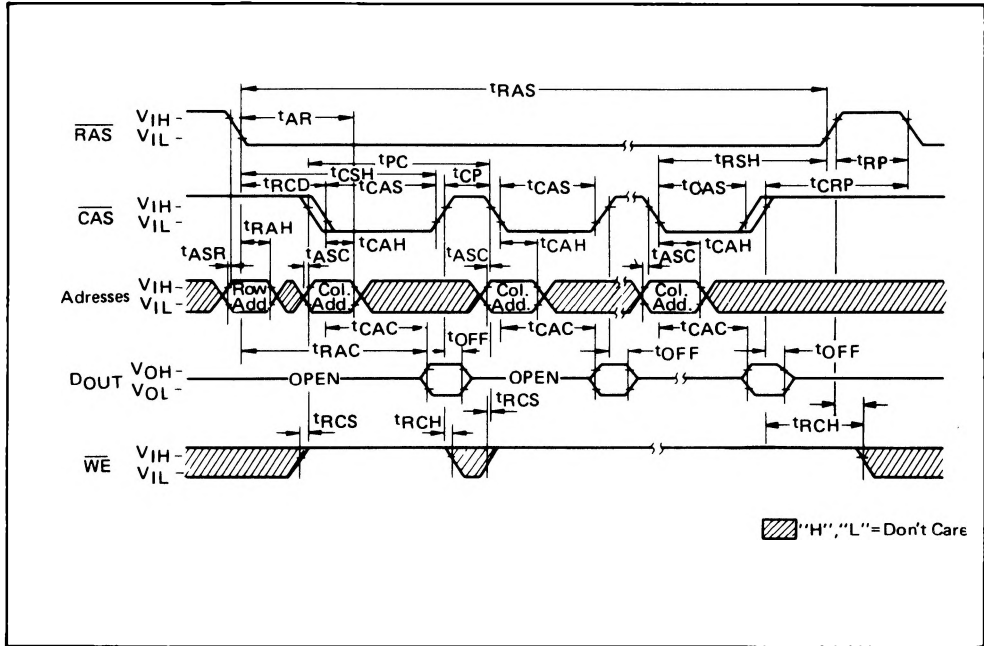


RAS ONLY REFRESH TIMING

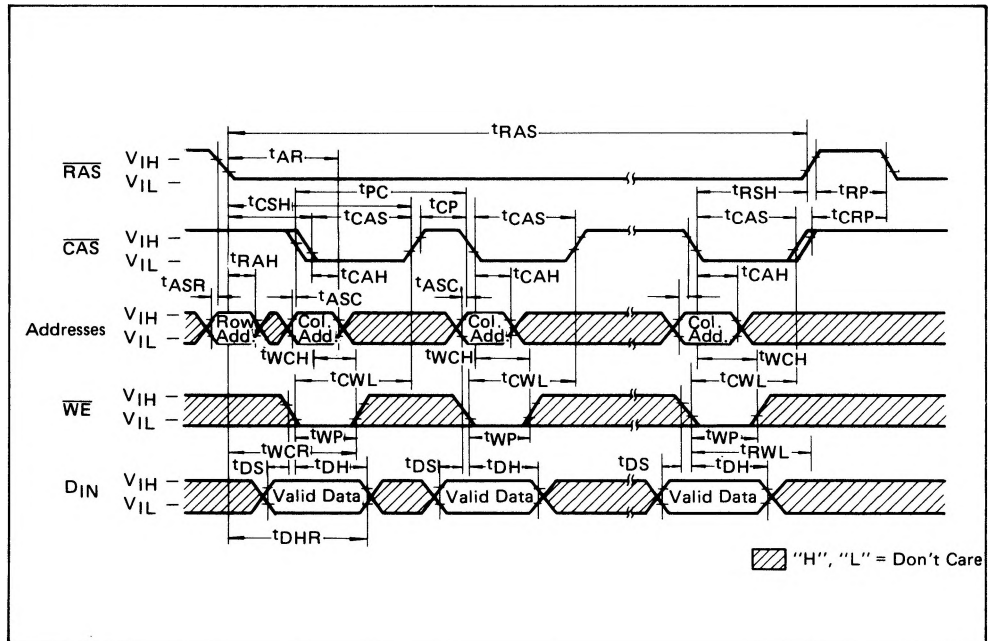
(CAS: V_{IH} , WE & DIN: Don't care)



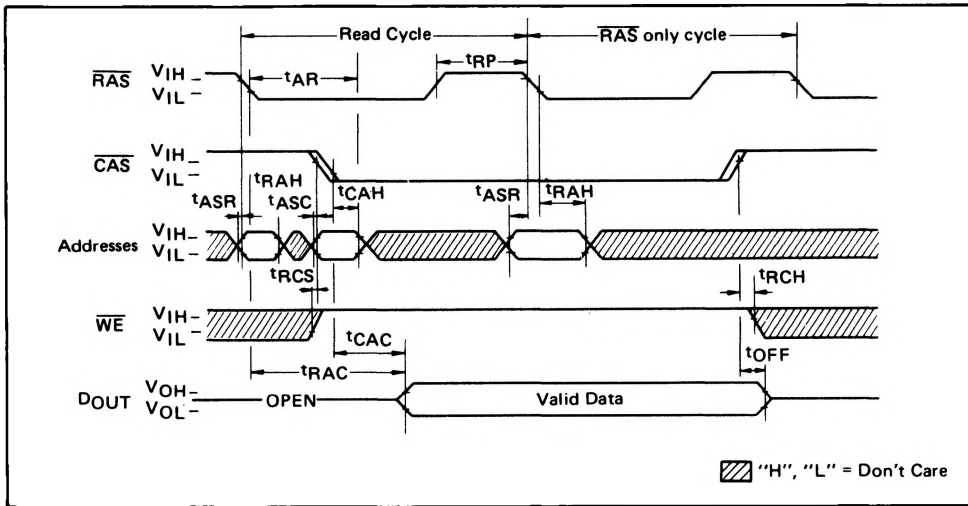
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HIDDEN REFRESH



FUNCTIONAL DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSC2301. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe (RAS). The eight column-address bits are established on the input pins and latched with the Column Address Strobe (CAS). All input addresses must be stable on or before the falling edge of RAS, CAS is internally inhibited (or "gated") by RAS to permit triggering of CAS as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the \overline{WE} input. A logic high (1) on \overline{WE} dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2301 during a write cycle. The last falling edge of \overline{WE} or \overline{CAS} is a strobe for the Data In (D_{IN}) register. In a write cycle, if \overline{WE} is brought low (write mode) before \overline{CAS} , D_{IN} is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} .

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until \overline{CAS} is brought low. In a read cycle, the output is valid after t_{RAC} from transition of RAS when t_{RCD} (Max.) is satisfied, or after t_{CAC} from transition of \overline{CAS} when the transition occurs after t_{RCD} (Max.). Data remain valid until \overline{CAS} is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSC2301 while maintaining RAS at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of RAS is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7 . RAS only refresh avoids any output during refresh because the output buffer is in the high impedance state unless \overline{CAS} is brought low. Strobing each of 128 row-addresses with RAS will cause all bits in

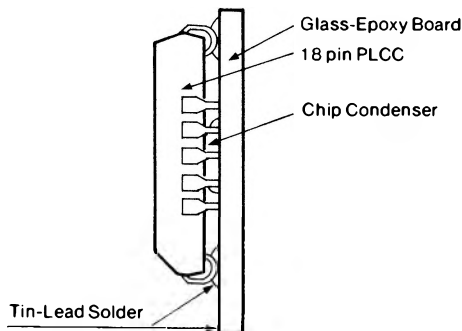
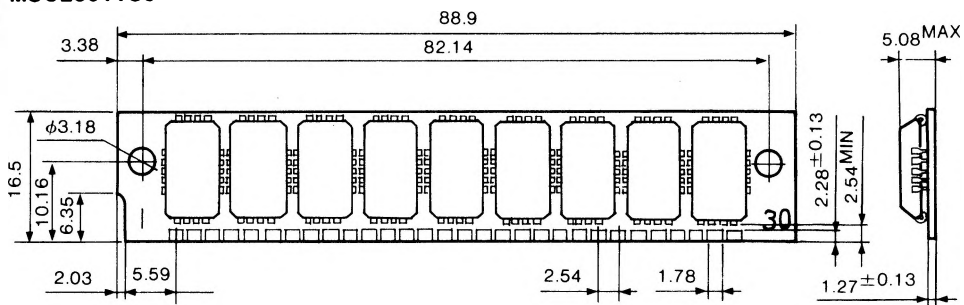
each row to be refreshed. Further $\overline{\text{RAS}}$ -only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

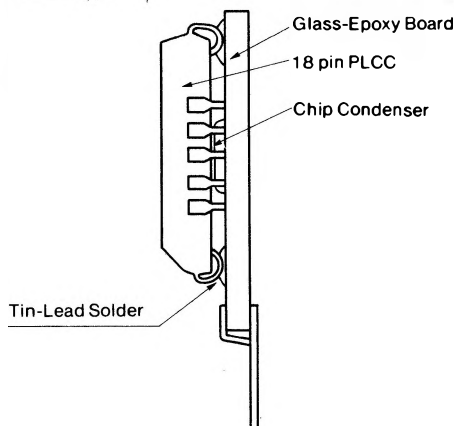
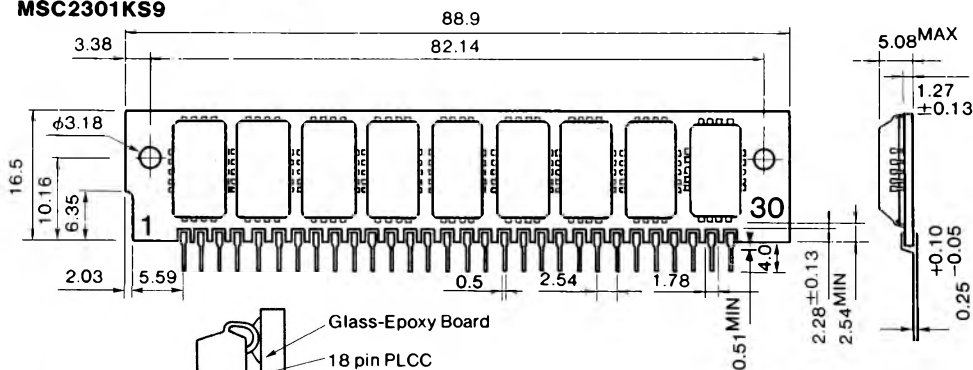
Hidden Refresh is performed by holding $\overline{\text{CAS}}$ as V_{IL} from a previous memory read cycle.

MSC2301YS9



1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18 μ m²)
4. Surface Coating: Photo Film Resist

MSC2301KS9



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