OKI semiconductor

MSM28101AAS

JAPANESE-CHARACTER GENERATING 1M BIT MASK ROM (E3-S-032-32)

GENERAL DESCRIPTION

The MSM 28101AAS is a 1M Bit Mask ROM using the N-channel silicon gate MOS process which stores 3,760 characters of numeric characters, Japanese cursive and square syllabarys, JIS 1st standard Japanese-characters, etc., in one chip.

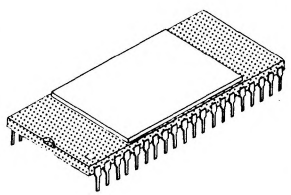
Because of its large capacity, Japanese-character pattern of 3,760 characters can be generated with only one chip. Furthermore, since the dot matrix character form of 18 lines x 16 strings is available from the data out pin by only inputting the JIS Japanese-character code into the address pin, the MSM28101AAS is efficient and optimum for constituting the Japanese-character terminal.

The power supply voltage is of 5 V single power supply, the input level is of TTL compatible, the data output is of 3-state output, the data valid is the output of the open collector and is packaged on the 40-pin DIP.

FEATURES

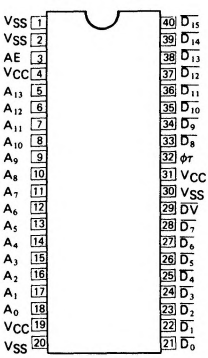
• Function	18 x 16 chinese-character font output
• Configuration	Duplex configuration of cell-array using the defect permissible technique
• Storage capacity	1082880 Bits
• Number of generating characters	3,418 characters
• Storage character range	Partition 0 ~ 7 and partition 16 ~ 47 of Japanese-character code system for JIS information processing
• Address input	14 Bits ($A_0 \sim A_{13}$)
• Data output	16 Bits ($\overline{D_0} \sim \overline{D_{15}}$, 3-state)
• Output mode	16 Bits x 18 times transfer
• Address enable	1 each (AE)
• Data valid	1 each ($\overline{DV}$, open collector output)
• Clock	1 each (ϕT) DC ~ 1.5MHz
• Used temperature	Ta = 0 ~ 70°C
• Access time	10 μs MAX
• Data transfer rate	22 μs/character
• Interface	TTL level
• Power supply voltage	5V single power supply (±5%)
• Power consumption	700 mW TYP
• Package	Side-brazed 40-pin DIP
• Memory cell	Multi-gate ROM

This specification is subject to change without notice



PIN CONFIGURATION

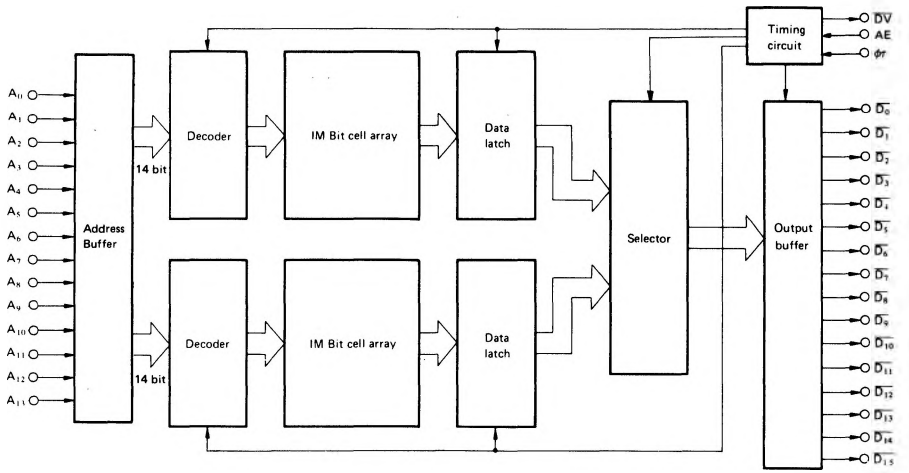
(Top View)



$A_0 \sim A_{13}$: Address input
$\overline{D_0} \sim \overline{D_{15}}$: Data output
AE: Address enable
$\overline{DV}$: Data valid output
ϕT: Clock input
V_{CC}: Power supply voltage (5V)
V_{SS}: GND (OV)

(Note) Connect all V_{CC} and V_{SS} terminals.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5 ~7	V
Input Terminal Voltage	V_{IN}	Respect to Vss	−0.5 ~7	V
Output Terminal Voltage	V_{OUT}	Respect to Vss	−0.5 ~7	V
Power Dissipation	P_D		2	W
Operating Temperature	T_{opr}		0 ~70	°C
Storage Temperature	T_{stg}		−35 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vcc	5V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
Input Signal Level	V_{IH}	Respect to Vss	2.0	5	6	V
	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Output Signal Level	V_{OH}	I_{OH}=−0.2 mA	2.4		Vcc	V
	V_{OL}	I_{OL} =1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_{IN}=0 ~Vcc	−10		10	μA
Output Leakage Current	I_{LO}	V_{OUT}=0 ~Vcc V_{AE}=0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC}=22μs t_C=650 ms t_{AR}=300 ns			170	mA
Steady State Power Supply Current	I_{CCS}	V_{AE}=0.8V			170	mA

AC CHARACTERISTICS

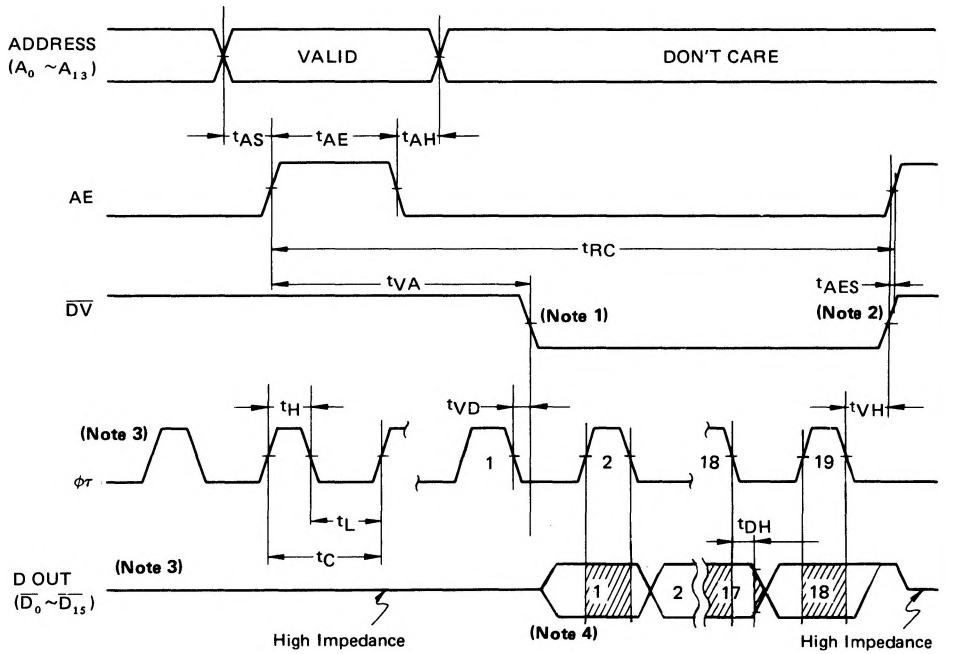
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.0V, V_{IL} = 0.8V
Input Rising, Falling Time	t_r = t_f = 15 ns
Input Timing Level	1.5V
Loading Condition	C_L = 50 pF, 1TTL Gate

READ CYCLE

(Vcc = 5V ±5%, T_a = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



(Note 1) $\overline{DV}$ is determined by the falling of ϕT.
(Note 2) $\overline{DV}$ changes with the falling of ϕT.
(Note 3) ϕT and Dn DATA are repeated 18 times during $\overline{DV}$ is Low.
(Note 4) The $\overline{Dn}$ timing levels are 2.0 V and 0.8 V.
(Note 5) Sometimes it will not normally operate unless input is made at least once with AE as the dummy after input of power supply.
(Note 6) $\overline{DV}$ is an open collector output and $\overline{Dn}$ is a 3-stage output.

INPUT/OUTPUT CAPACITANCE

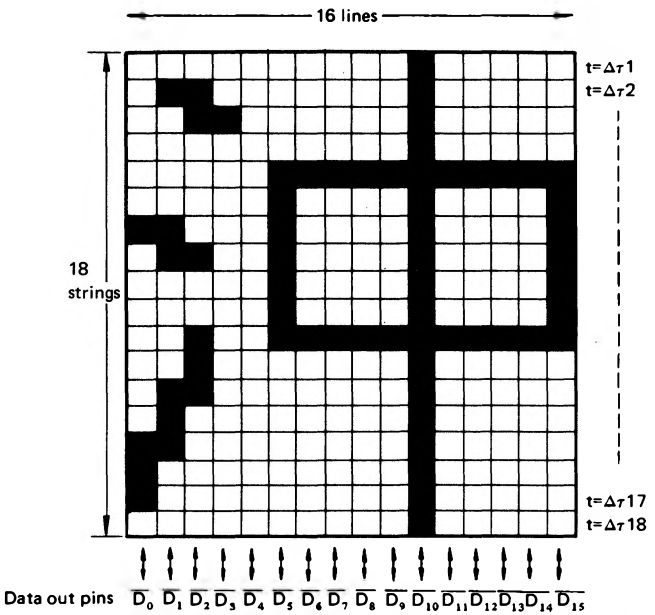
(Ta = 25°C, f = 1 MHz)

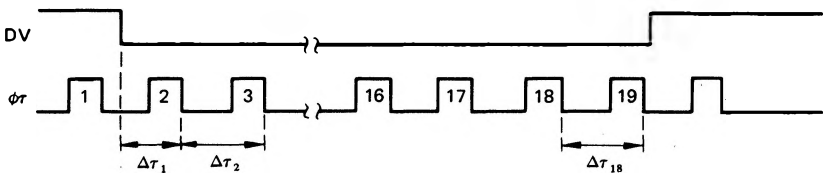
Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_{IN}	V_{IN} = OV			8	pF
Input Capacitance (AE terminal)	C_{IN}	V_{IN} = OV			15	pF
Output Capacitance	C_{OUT}	V_{OUT} = OV			8	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Specification	Unit	Remarks
Font Type	18 lines x 16 strings dot matrix		
Output Mode	16 bits x 18 times transfer		**(Note 1)**
Number of Generating characters	3418	Word	
Storage Character Range	0 ~ 7 (Non chinese-character area) 16 ~ 47 (JIS 1st standard)	Partition	**(Note 2)**

(Note 1) The correspondence of the 18 lines x 16 strings matrix and the data out pins are as shown in the diagram below.
Output for the character portion will be Low (V_{OL}) and the output for the background portion will be High (V_{OH}).





(Note 2) The correspondence of the 1st and 2nd bytes of JIS C 6226 and the address pins are as shown below.

JIS C 6226	Second byte							First byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0