OKI semiconductor

MSM28201AAS

1M BIT MASK ROM FOR JAPANESE-CHARACTER PATTERN (E3-S-033-32)

GENERAL DESCRIPTION

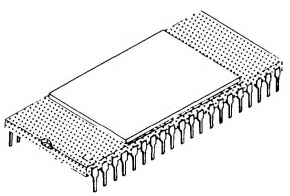
The MSM28201AAS is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 Japanese-characters (kanji conforming with JIS No. 2 standards) incorporated in single chip.

With this large capacity, 3760 Japanese-character patterns can be generated in a single chip. And by only a single input of JIS Japanese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile Japanese-character terminals.

The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

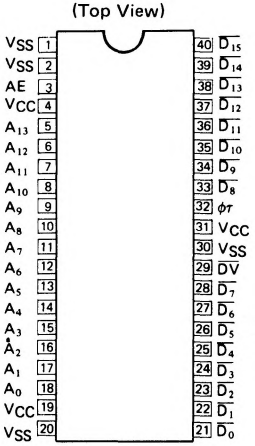
FEATURES

- Function . . . . . 18 x 16 chinese-character font output
- Configuration . . . . Duplex configuration employing defect permissible technique
- Storage capacity . . . 1082880 bits
- Number of generated characters . . . . . 3384 characters
- Accommodation character region . . . Japanese-character encoded partitions 48 to 87 for JIS data processing.
- Address input . . . . 14 bits (A_0 to A_{13})
- Data output . . . . . 16 bits ($\overline{D_0}$ to $\overline{D_{15}}$, tristate)
- Output mode . . . . 16 bit x 18 transfers
- Address enable . . . 1 (AE)
- Data valid . . . . . 1 ($\overline{DV}$, open collector output)
- Clock . . . . . 1 (ϕT) DC to 1.5MHz
- Operating temperature . . . . . Ta=0°C to 70°C
- Access time . . . . . 10 μs MAX.
- Data transfer rate . . 22 μs/character
- Interface . . . . . TTL level
- Power supply voltage 5V single (±5%)
- Power consumption . 700 mW TYP
- Package . . . . . Side-brazed 40-pin DIP
- Memory cell . . . . . Multi-gate ROM



PIN CONFIGURATION

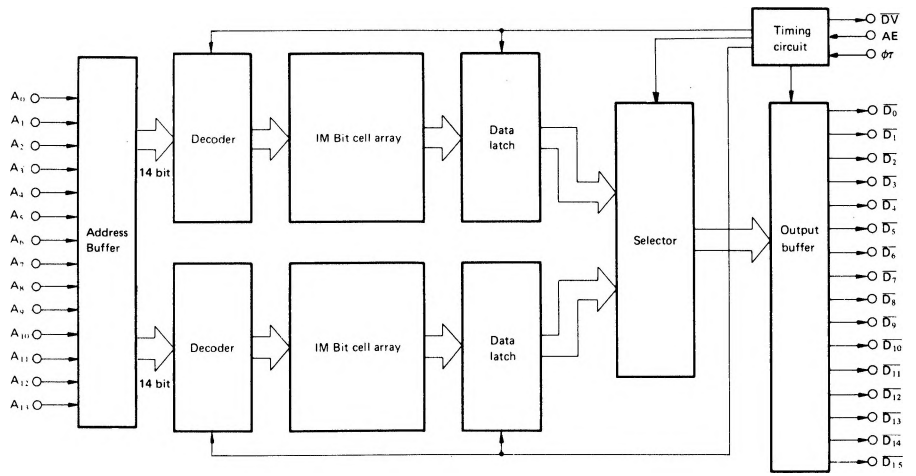
(Top View)



$A_0 \sim A_{13}$: Address inputs
$\overline{D_0} \sim \overline{D_{15}}$: Data outputs
AE : Address enable
$\overline{DV}$: Data valid output
ϕT : Clock input
Vcc : Power supply voltage (5 V)
Vss : GND (0 V)

Note: All Vss pins are to be connected

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5~7	V
Input Voltage	V_I	Respect to Vss	−0.5~7	V
Output Voltage	V_O	Respect to Vss	−0.5~7	V
Power Dissipation	P_D		2	W
Operating Temperature	Topr		0 ~ 70	°C
Storage Temperature	Tstg		−35~125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Range Value			Unit
			Min	Typ	Max	
Power Supply Voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
"H" Input Voltage	V_{IH}	Respect to Vss	2.0	5	6	V
"L" Input Voltage	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
"H" Output Voltage	V_{OH}	I_{OH} = −0.2 mA	2.4		V_{CC}	V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leakage Current	I_{LI}	V_I = 0 ~ V_{CC}	−10		10	μA
Output Leakage Current	I_{LO}	V_O = 0 ~ V_{CC} V_{AE} = 0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC} = 22μS, t_C = 650 ns t_{AE} = 300ns			170	mA
Rated Power Supply Current	I_{CCS}	V_{AE} = 0.8V			170	mA

AC CHARACTERISTICS

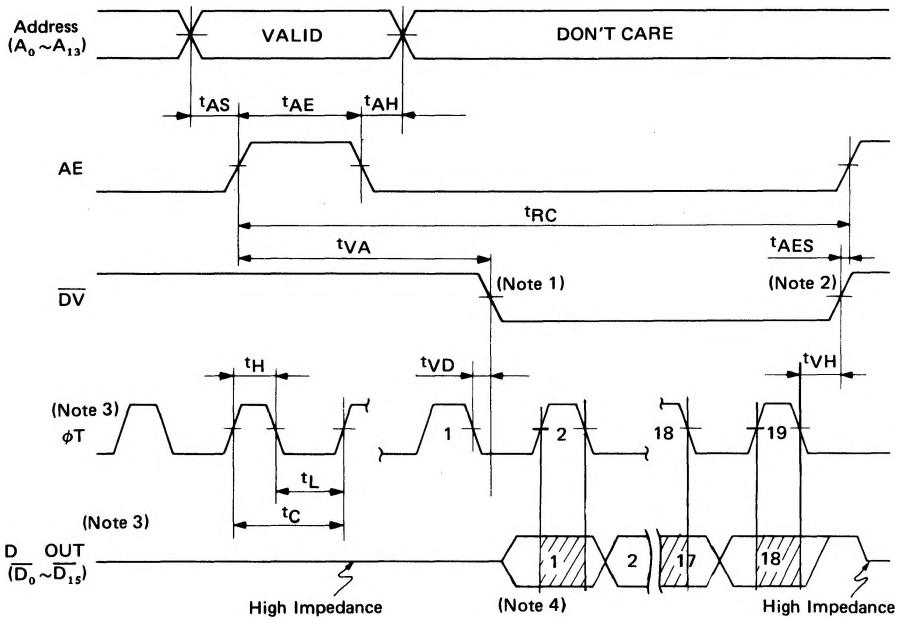
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0 V, V_{IL}=0.8 V
Input Rise/Fall Time	tr=tf=15ns
Input Timing Level	1.5V
Output Load	C_L=50pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



Notes:
1. $\overline{DV}$ is determined by the φT falling edge.
2. $\overline{DV}$ is changed by the φT falling edge.
3. φT and DnDATA are repeated 18 times when $\overline{DV}$ is low.
4. $\overline{Dn}$ timing levels of 2.0V and 0.8V.
5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
6. $\overline{DV}$ denotes open collector output, and $\overline{Dn}$ the tristate output.

INPUT/OUTPUT CAPACITANCE

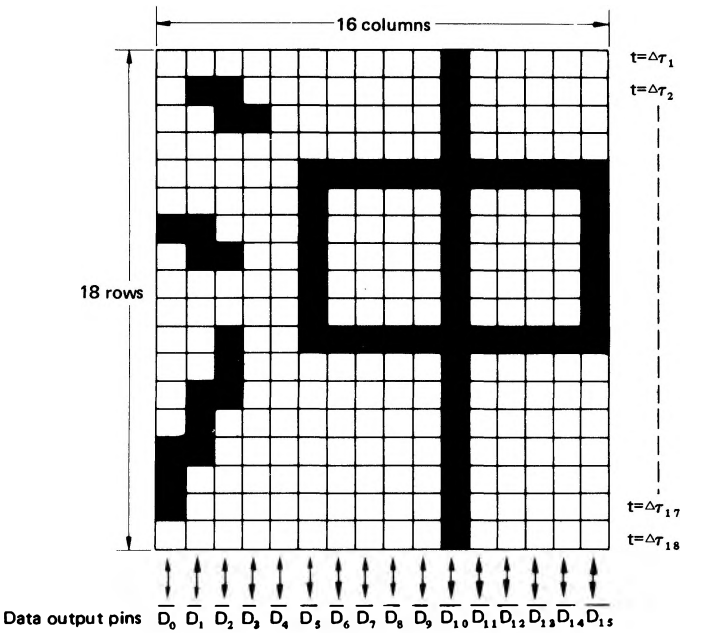
(Ta=25°C, f=1 MHz)

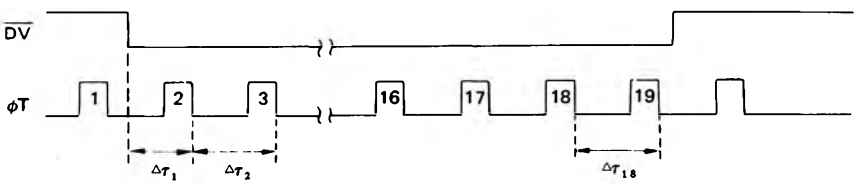
Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_I	V_I=0 V			15	pF
Input Capacitance (AE pin)	C_I	V_I=0 V			35	pF
Output Capacitance	C_O	V_O=0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Range	Unit	Remarks
Font Format	18-row x 16-column dot matrix		
Output Mode	16 bit x 18 transfers		(Note 1)
Number of Characters Generated	3384	Word	
Character Accommodation Region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (V_{OL}) for the character portion, and high (V_{OH}) for the background area.





Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

JIS C 6226	No.2 byte							No.1 byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0