OKI semiconductor

MSM2114LRS

4096-BIT (1024 x 4) STATIC RAM

GENERAL DESCRIPTION

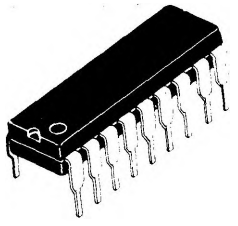
The Oki MSM2114L is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable N-channel Silicon Gate MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM2114L series is offered in an 18-pin dual-in-line plastic (RS Suffix) package. The series is guaranteed for operation from 0°C to 70°C.

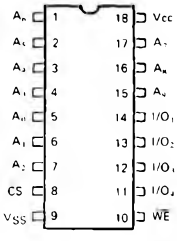
FEATURES

- Low Power Dissipation
- Single +5V Supply (±10% Tolerance)
- High Density 300-mil 18-Pin Package
- Fully Static Operation
- Common I/O Capability using Three-State Outputs
- Directly TTL Compatible
- N-channel Silicon Gate MOS Technology
- Interchangeable with Intel 2114L Devices

	2114L-2	2114L-3	2114L
Max. Access Time (NS)	200	300	450
Max. Power Dissipation (MW)	370	370	370

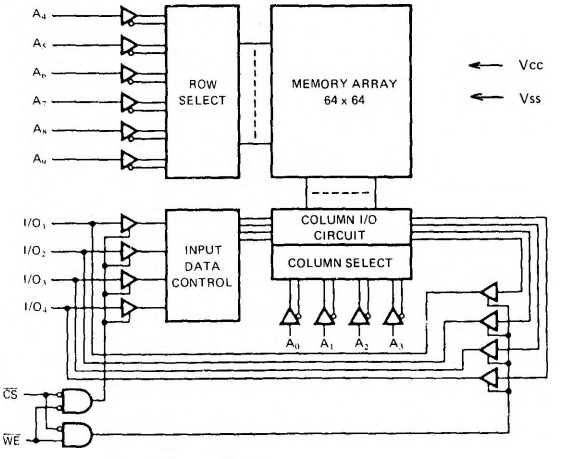


PIN CONFIGURATION



A_0 ~ A_9: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
I/O_1-I/O_4: Data Input/Output
Vcc: +5V Supply
V_{SS} : Ground

FUNCTIONAL BLOCK DIAGRAM



$\overline{CS}$	$\overline{WE}$	I/O	Mode
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D-out	Read

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Temperature Under Bias	Topr	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +150	°C	
Supply Voltage	V_{CC}	−0.5 to +7	V	Respect to V_{SS}
Input Voltage	V_{IN}	−0.5 to +7	V	
Output Voltage	V_{OUT}	−0.5 to +7	V	
Power Dissipation	P_D	1.0	W	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ±10%
Input Signal Level	V_{IH}	2.0	5	5.5	V	Respect to V_{SS}
	V_{IL}	−0.5	0	0.8	V	
Operating Temperature	T_{opr}	0		+70	°C	

DC CHARACTERISTICS

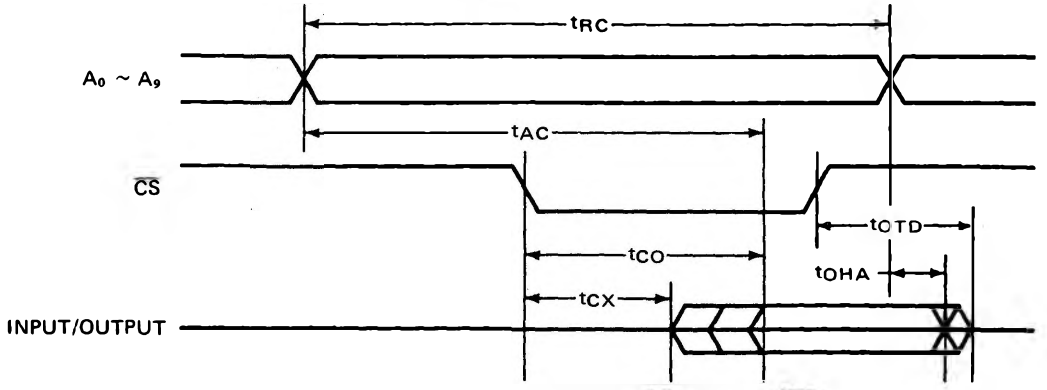
(V_{CC} = 5V ±10, T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}			10	μA	V_{IN} = 0 to +5.5V
I/O Leakage Current	I_{LOL}			−10	μA	$\overline{CS}$ = 2.4V $V_{I/O}$ = 0.4V
I/O Leakage Current	I_{LOH}			10	μA	$\overline{CS}$ = 2.4V $V_{I/O}$ = 5.5V
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −0.2mA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0mA
Power Supply Current	I_{CC}			70	mA	V_{CC} = 5.25V I/O = 0mA T_A = 0°C
Power Supply Current	I_{CC}			72	mA	V_{CC} 5.5V I/O = 0mA T_A = 0°C

AC CHARACTERISTICS
READ CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	2114L-2		2114L-3		2114L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		300		450		ns
Access Time	t_{AC}		200		300		450	ns
Chip Selection to Output Valid	t_{CO}		70		100		120	ns
Chip Selection to Output Active	t_{CX}	20		20		20		ns
Output 3-state from Deselection	t_{OTD}		60		80		100	ns
Output Hold from Address Change	t_{OHA}	10		10		10		ns



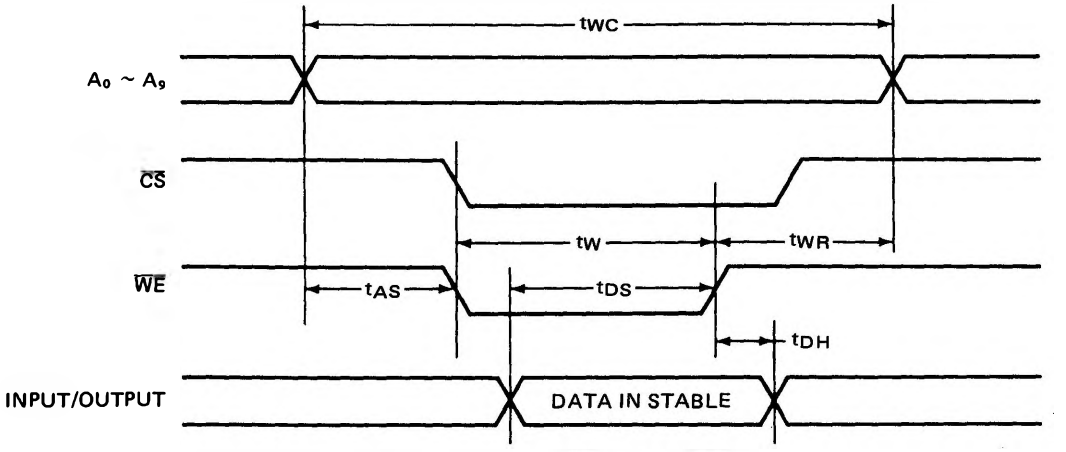
Notes:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.
3. Input Pulse Levels: 0.8V to +2.0V
4. Input Rise and Fall Time: 10ns
5. Timing Measurement Reference Levels: 1.5V
6. Output Load: 1 TTL Gate and C_L = 50pF

WRITE CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to 70°C)

Parameter	Symbol	2114L-2		2114L-3		2114L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		450		ns
Write Time	t_W	120		150		200		ns
Write Release Time	t_{WR}	20		30		50		ns
Address Setup Time	t_{AS}	0		0		0		ns
Data Setup Time	t_{DS}	120		150		200		ns
Data Hold From Write Time	t_{DH}	0		0		0		ns

WRITE CYCLE



Notes:
1. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. Input Pulse Levels: 0.8V to +2.0V
3. Input Rise and Fall Time: 10ns
4. Timing Measurement Reference Levels: 1.5V
5. t_W: Overlap time of a low $\overline{CS}$ and low $\overline{WE}$
6. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
7. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
8. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
9. When I/O pins are Data output mode, don't force inverse signal to those pins.

CAPACITANCE

($T_a = 25°C$, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	C_I/O		6	8	pF
Input Capacitance	C_{IN}		4	6	pF

Note: This parameter is periodically sampled and not 100% tested.