Preliminary

OKI semiconductor

MSM414256RS

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

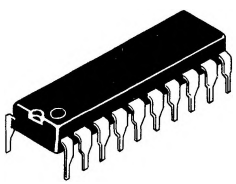
The MSM414256RS is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM414256RS is OKI's N channel silicon gate MOS process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

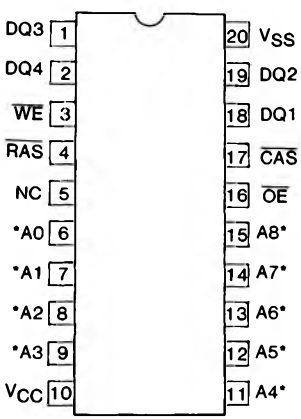
- Silicon gate, tripple polysilicon NMOS, 1-transistor memory cell
- 262,144 words by 4 bits
- Standard 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Stand By (MAX)
MSM414256-10RS	100 ns	200 ns	413 mW	28 mW
MSM414256-12RS	120 ns	230 ns	385 mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and OE operations
- Page mode, read modify write capability
- CAS before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit



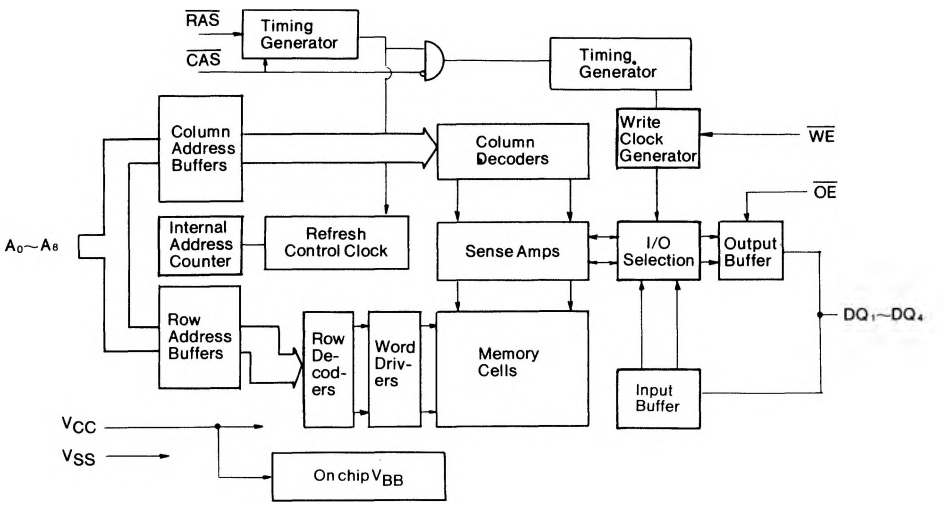
PIN CONFIGURATION (TOP VIEW)



*Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 414256-10		MSM 414256-12		Unit	Note
			MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	–	2.4	–	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	–	−0.4	–	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	75	–	70	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH}	–	5	–	5	mA	
Average power supply current* ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min	–	65	–	60	mA	
Average power supply current* (Page mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	–	70	–	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	70	–	65	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	10	pF
I/O capacitance (DQ1 to DQ4)	C	–	–	7	pF

AC CHARACTERISTICS

Note 1, 2, 3 (V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read/write cycle time	t_{RC}	200	–	230	–	ns	
Read/write cycle time	t_{RWC}	275	–	305	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	5, 6
Output buffer turn-off delay	t_{OFF}	0	25	0	25	ns	
Transition time	t_T	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90	–	100	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	7, 8
$\overline{CAS}$ and $\overline{RAS}$ set-up time	t_{CRS}	15	–	20	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$,	t_{AR}	70	–	80	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	10
Write command hold time from $\overline{RAS}$	t_{WCR}	80	–	95	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	9
Write command hold time	t_{WCH}	30	–	35	–	ns	

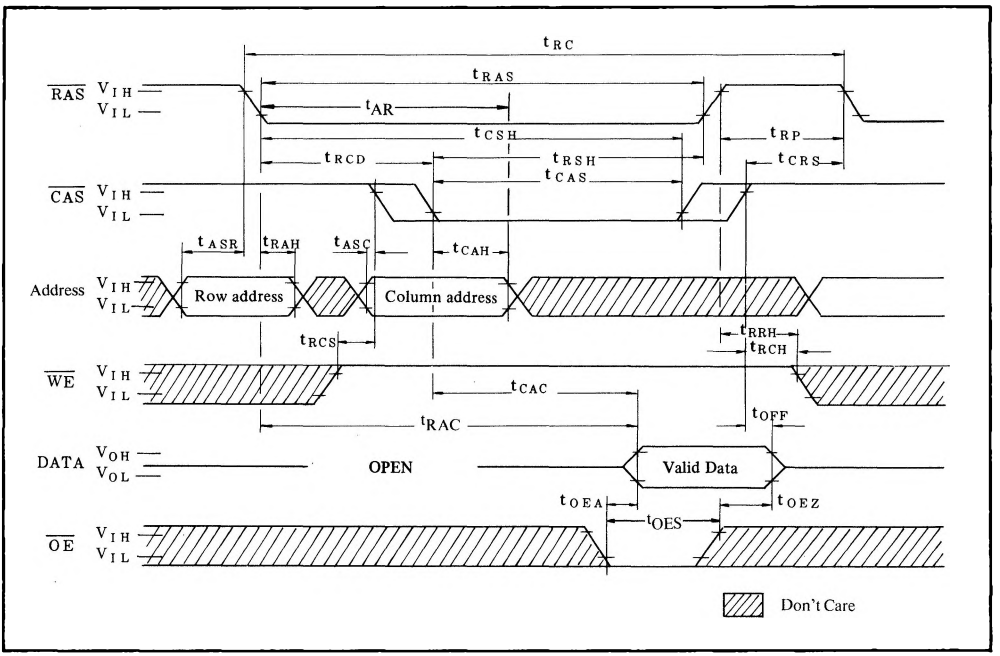
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM414256-10		MSM414256-12		Unit	Note
		MIN	MAX	MIN	MAX		
Write command pulse width	t_{WP}	30	–	35	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40	–	40	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40	–	40	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	30	–	35	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	80	–	95	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80	–	90	–	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130	–	150	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	10
Access time from $\overline{OE}$	t_{OEA}	–	30	–	30	ns	
$\overline{OE}$ data delay time	t_{OED}	25	–	25	–	ns	
$\overline{OE}$ hold time	t_{OEH}	0	–	0	–	ns	11
Turn-off delay time from $\overline{OE}$	t_{OEZ}	0	25	0	25	ns	
$\overline{OE}$ set-up time	t_{OES}	30	–	30	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
Read/write cycle (Refresh counter test)	t_{RTC}	385	–	435	–	ns	11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	285	10000	325	10000	ns	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	50	–	60	–	ns	11
Read/write cycle time (Page mode)	t_{PRWC}	175	–	195	–	ns	

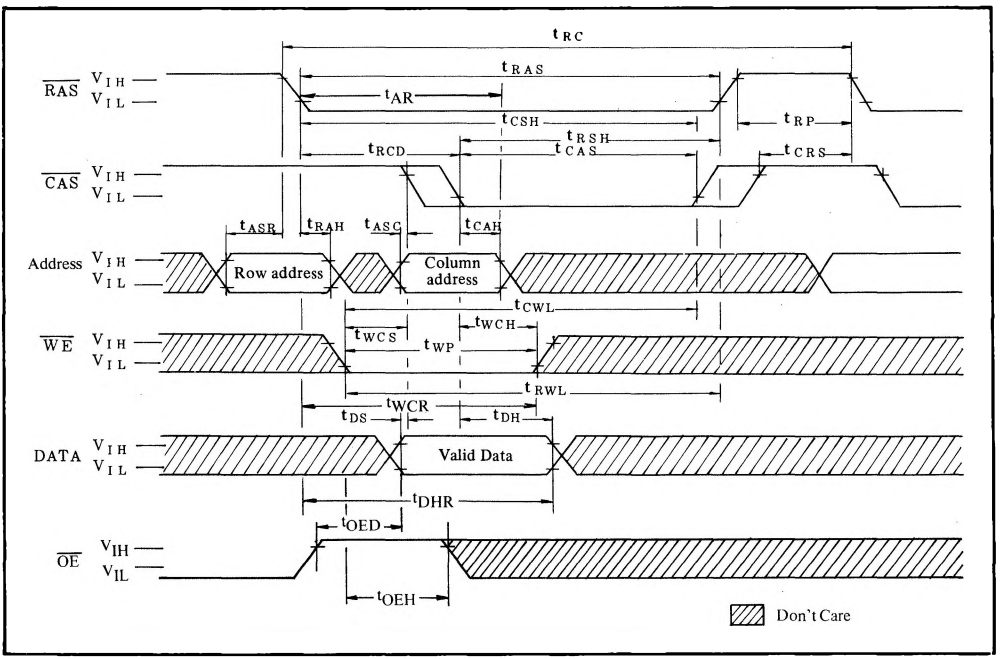
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL + 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geqq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

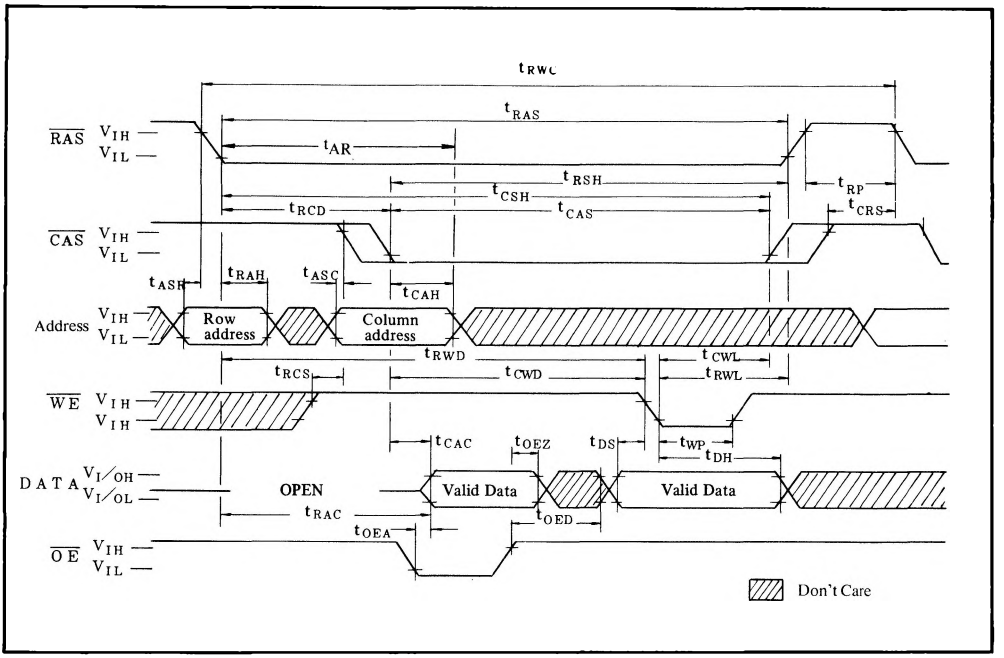
READ CYCLE



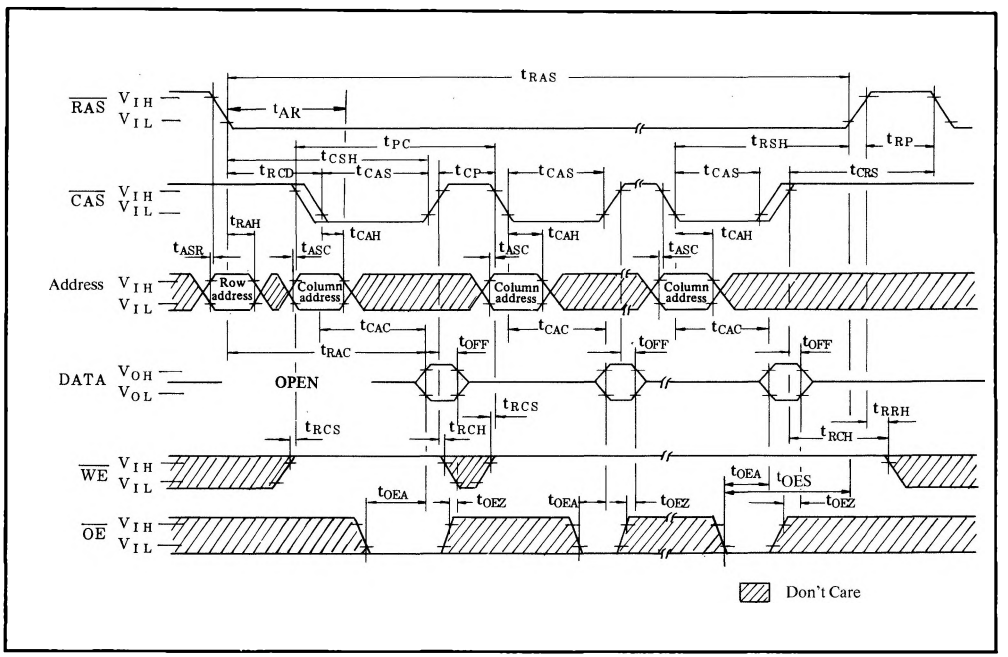
WRITE CYCLE (EARLY WRITE)



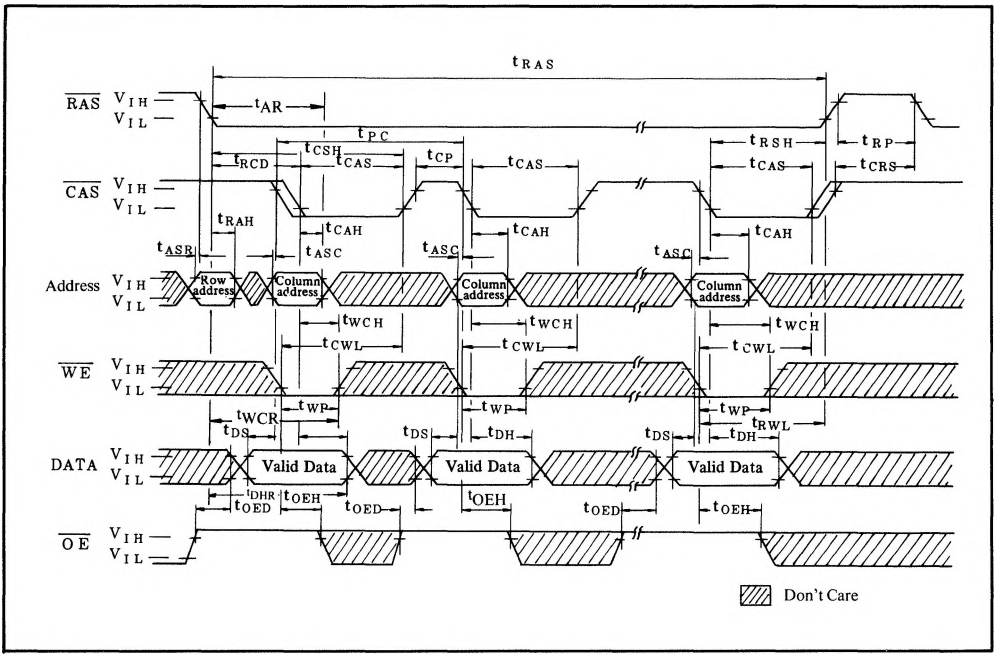
READ/WRITE AND READ MODIFY WRITE CYCLE



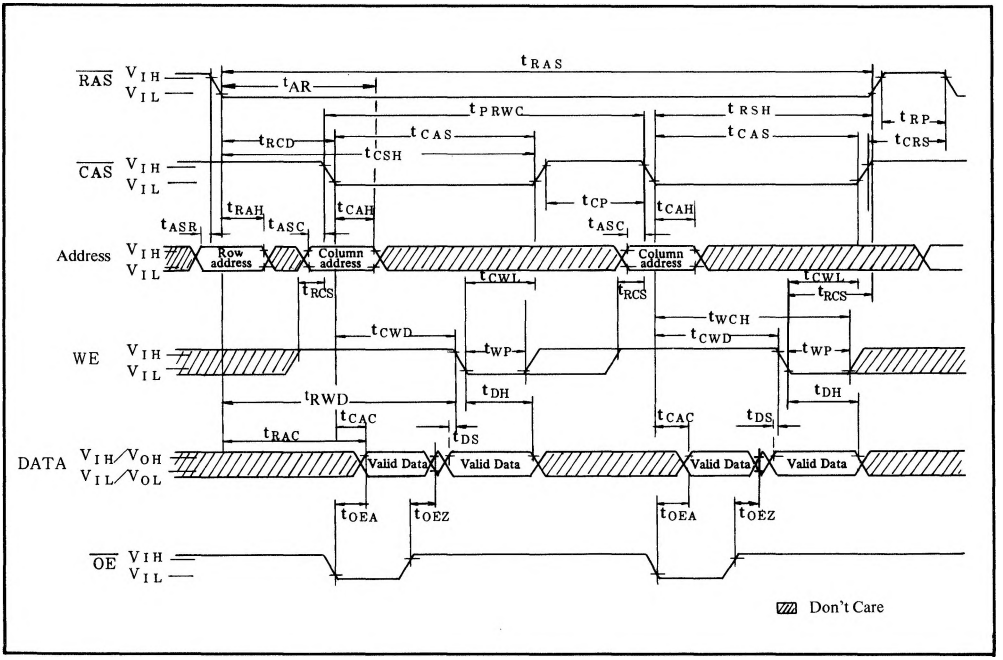
PAGE MODE READ CYCLE



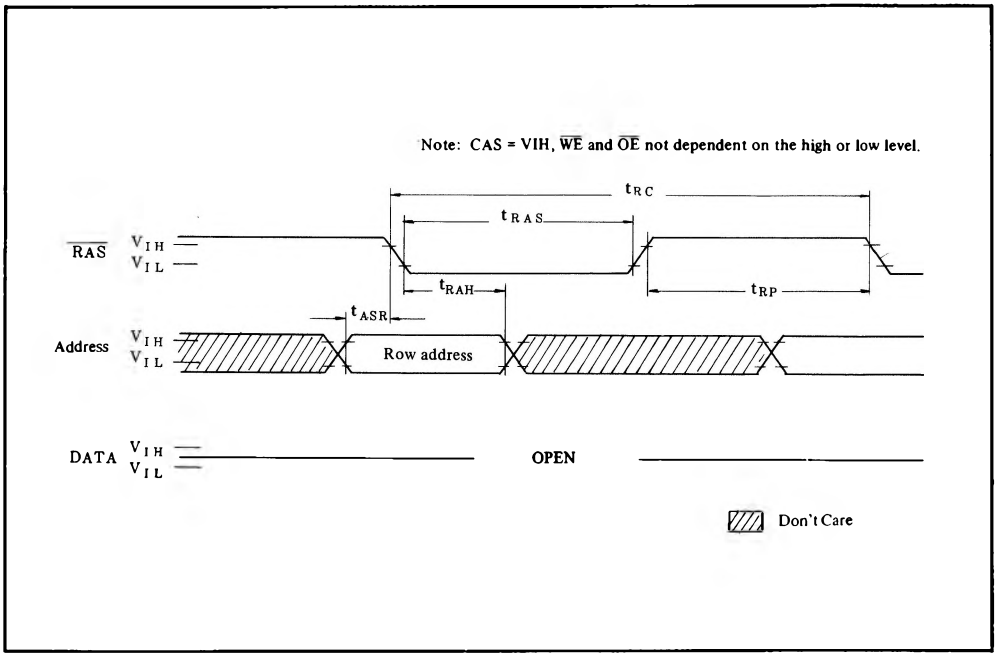
PAGE MODE WRITE CYCLE



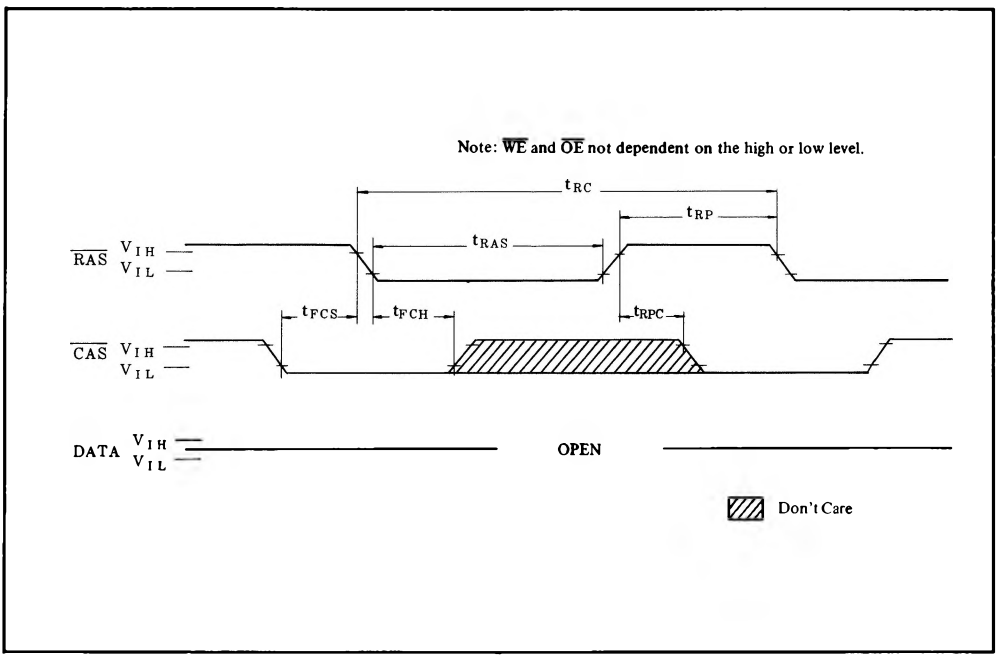
PAGE MODE READ/WRITE CYCLE



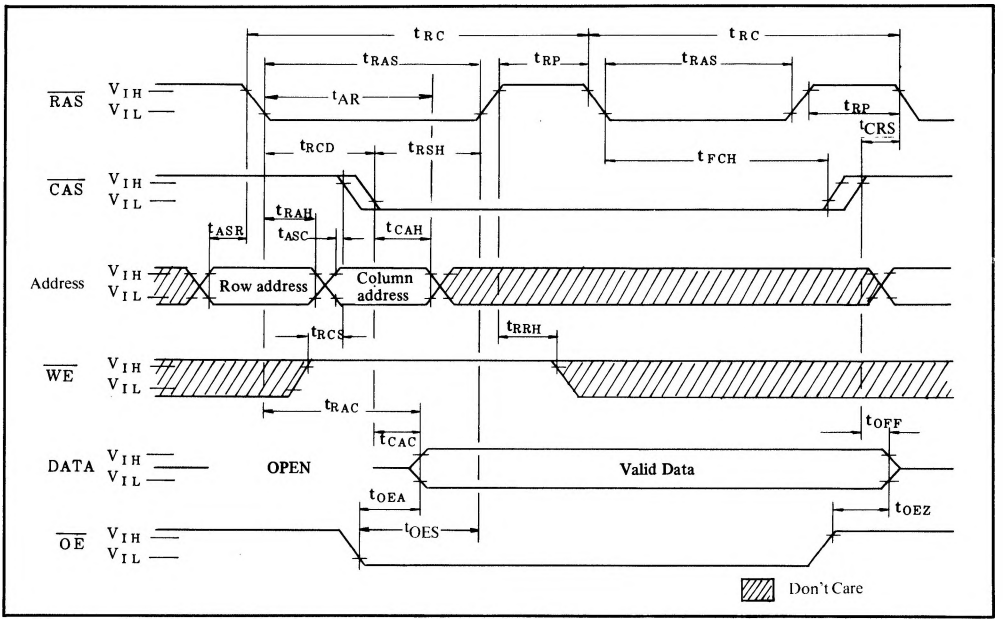
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



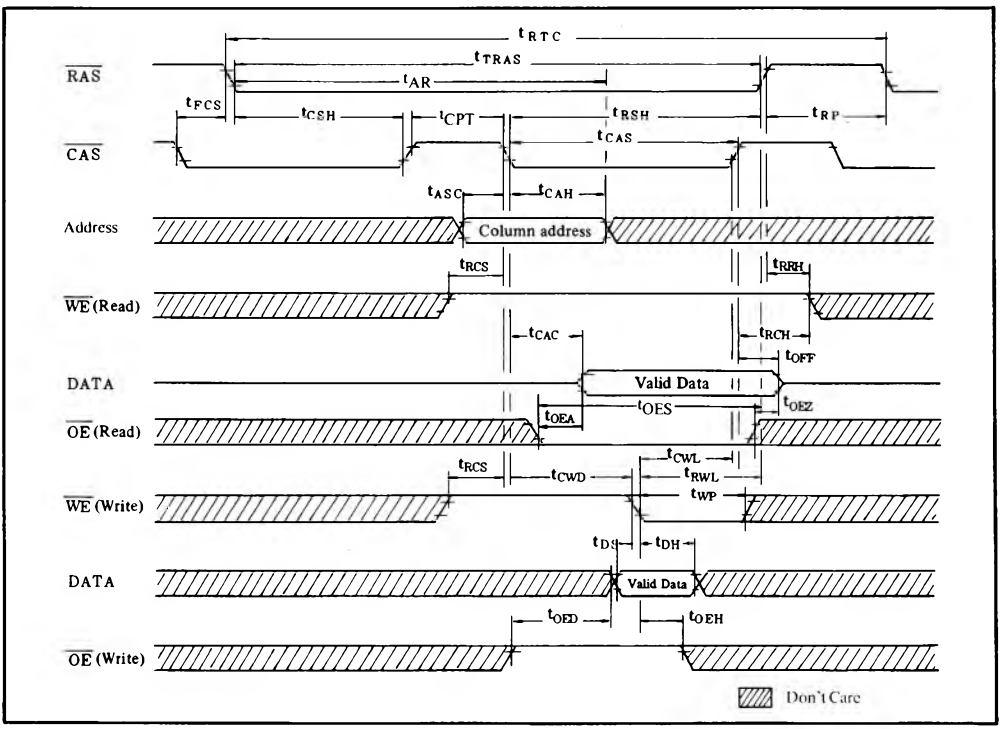
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

18 bits of binary address input are required to decode any one of the 262,144 words by 4 bits storage cell locations.

9 row-address bits are set up on address input pins A0 through A8 and latched onto the chip by the row address strobe ($\overline{RAS}$). Then 9 column-address bits are set up on pins A0 through A8 and latched onto the chip by the column address strobe ($\overline{CAS}$).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ is low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{CAS}$ or $\overline{OE}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses (A_0 to A_8) at least every eight milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 512 (A_0 to A_8) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  – Bits A_0 through A_8 are defined by the refresh counter.
* A COLUMN ADDRESS
  – All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 512 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 512 times, and highs are written into the 512 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).