OKI semiconductor

MSM41464RS

65,536-WORD × 4-BITS DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM41464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

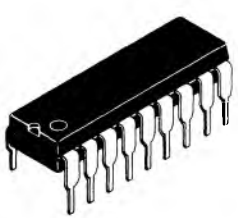
Multiplexed row and column address inputs permit the MSM41464 to be housed in a standard 18 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh provides an on-chip refresh capability.

The MSM41464 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

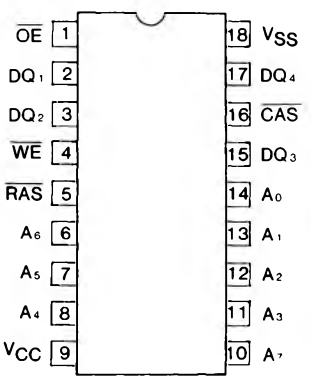
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 65,536 × 4 RAM, 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41464-10RS)
  - 120 ns max (MSM41464-12RS)
  - 150 ns max (MSM41464-15RS)
- Cycle time:
  - 200 ns min (MSM41464-10RS)
  - 230 ns min (MSM41464-12RS)
  - 260 ns min (MSM41464-15RS)
- Low power:
  - 385 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{\text{CAS}}$
- 256 refresh cycles/4 ms
- Output impedance controllable through early write and $\overline{\text{OE}}$ operations
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- "Page Mode" capability

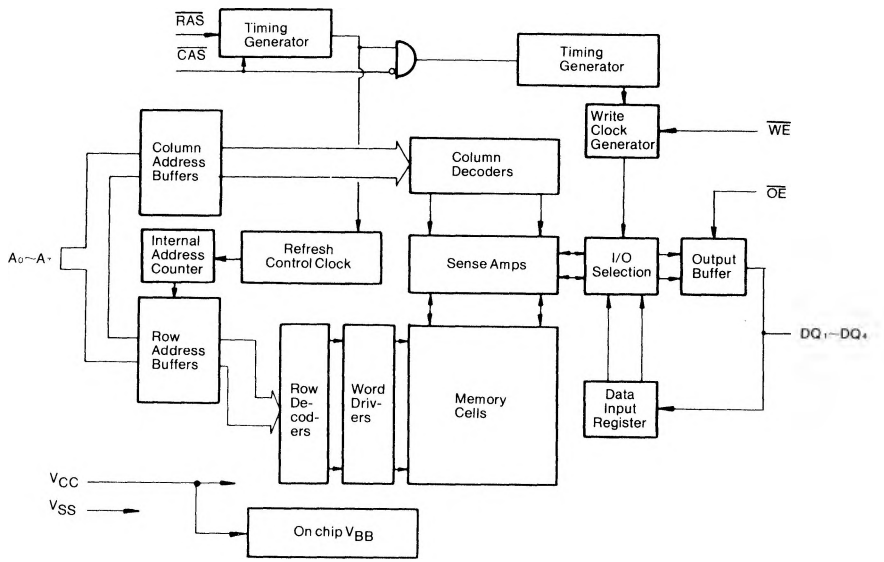


PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 - A_7$	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$DQ_1 - DQ_4$	Data In/Data Out
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		70	mA	
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		55	mA	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		60	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_7$)	C_{IN1}	–	7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	10	pF
Data I/O capacitance ($DQ_1 \sim DQ_4$)	C_D	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		230		260		
Read-write cycle time	t_{RWC}	ns	275		320		360		
Page mode cycle time	t_{PC}	ns	100		120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	35	0	40	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	ns	40		50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	22	50	22	60	25	75	7, 8
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	12		12		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	15		15		20		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		10
Write command set-up time	t_{WCS}	ns	−5		−5		−5		9

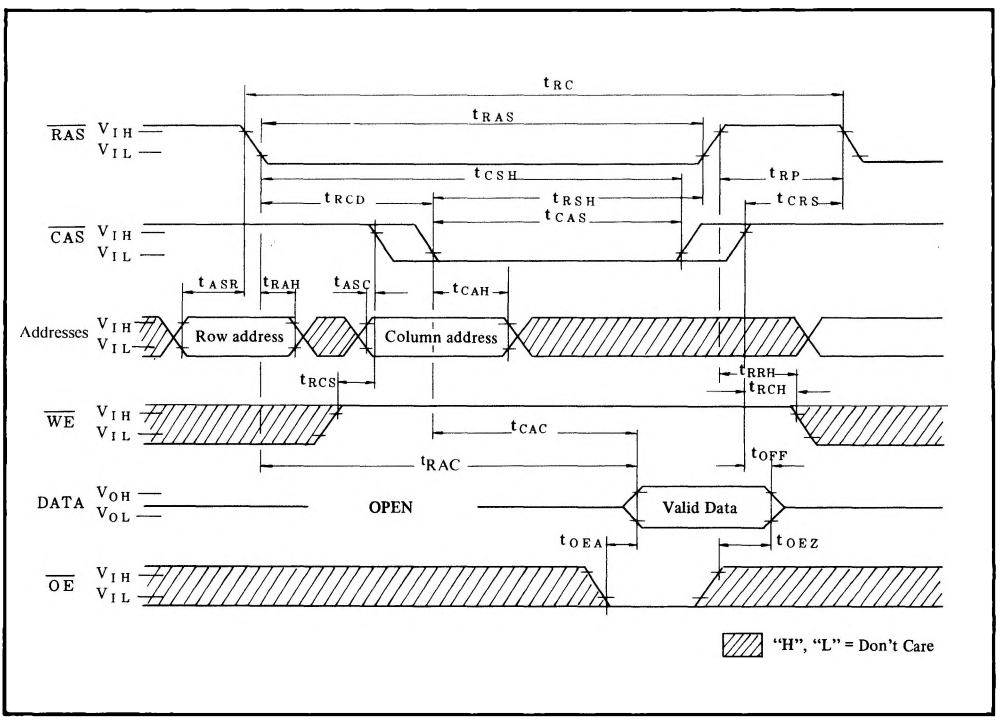
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41464-10		MSM41454-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	20		25		30		
Write command hold time	t_{WCH}	ns	20		25		30		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		45		50		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		45		50		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		25		30		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	85		100		120		9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	135		160		195		9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		20		25		10
Access time from $\overline{OE}$	t_{OEA}	ns		25		30		40	
$\overline{OE}$ data delay time	t_{OED}	ns	30		35		40		
$\overline{OE}$ hold time	t_{OEH}	ns	0		0		0		
Turn-off delay time from $\overline{OE}$	t_{OEZ}	ns	0	30	0	35	0	40	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	ns	20		25		30		
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	ns	20		20		20		
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	ns	20		25		30		
Read/write cycle (Refresh counter test)	t_{RTC}	ns	385		450		515		11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	ns	285	10μs	340	10μs	405	10μs	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	ns	50		60		70		11
Read/write cycle time (Page mode)	t_{PRWC}	ns	175		210		245		

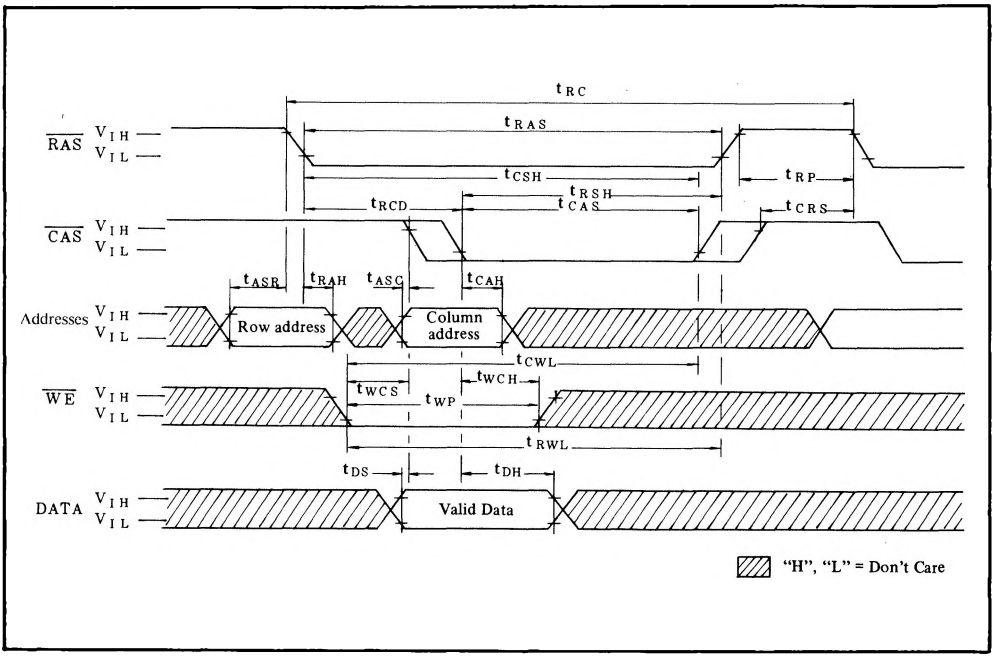
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.) If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle and the data in/data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data in/data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

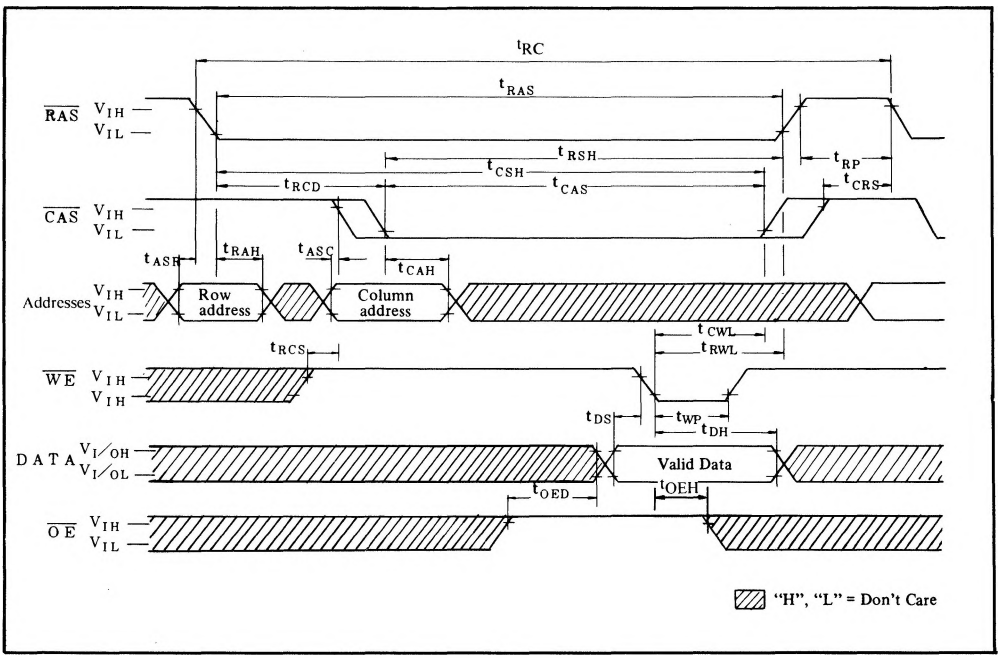
READ CYCLE



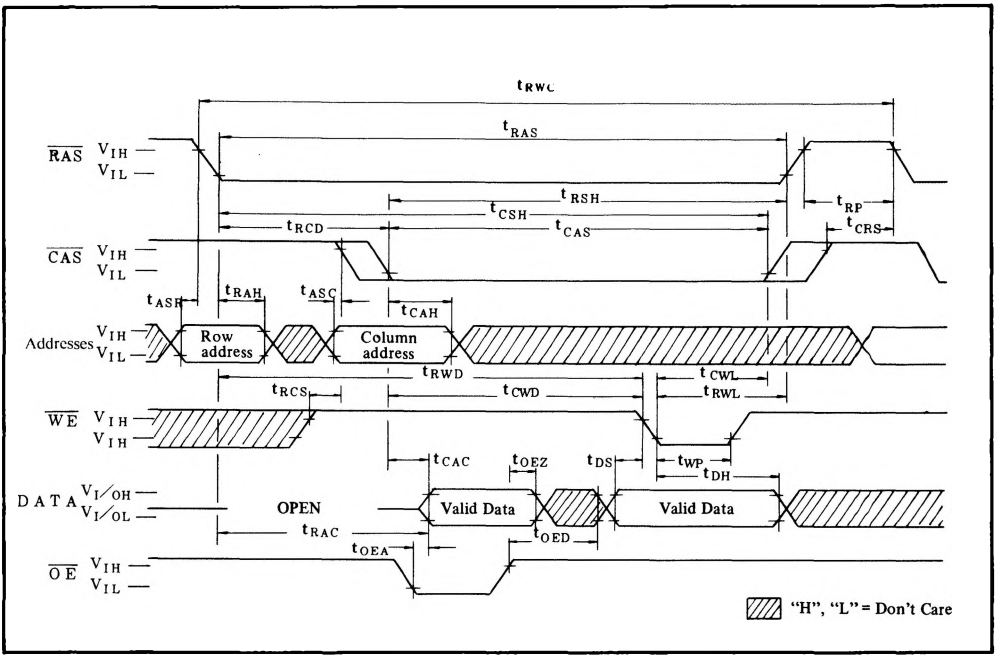
WRITE CYCLE (EARLY WRITE)



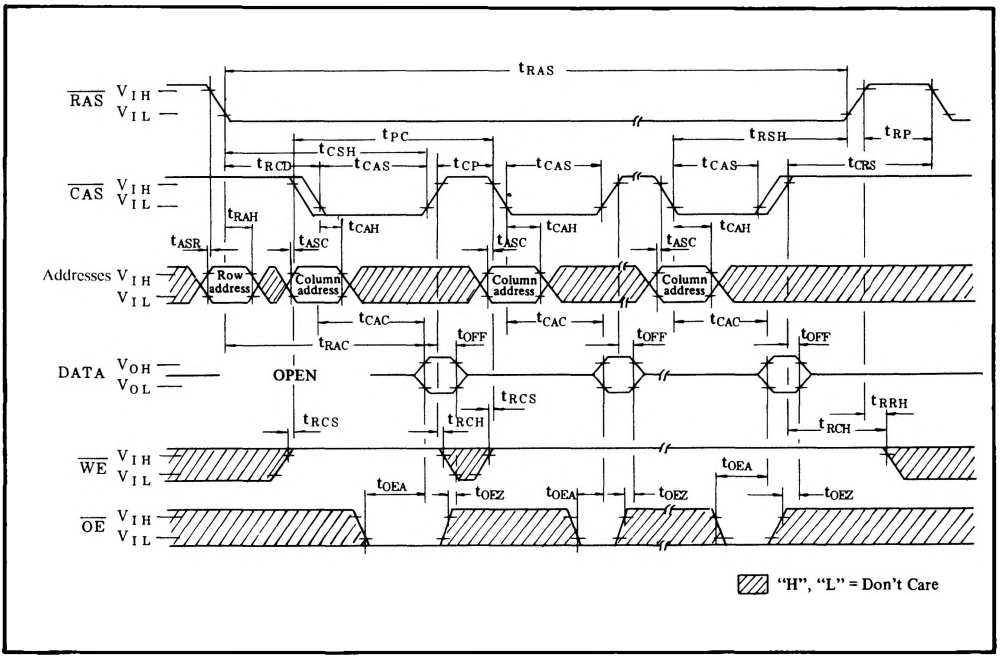
$\overline{OE}$ WRITE CYCLE



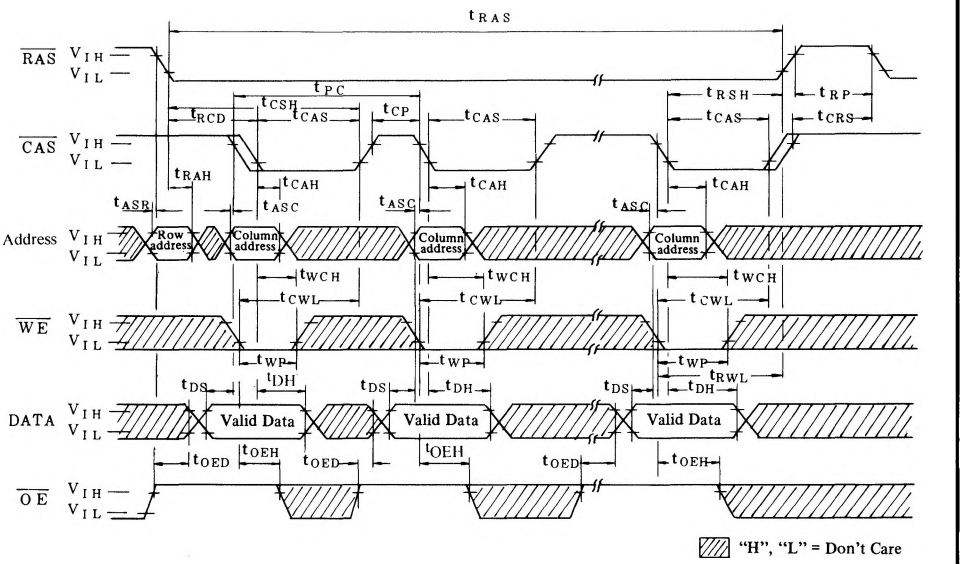
READ/WRITE AND READ MODIFY WRITE CYCLE



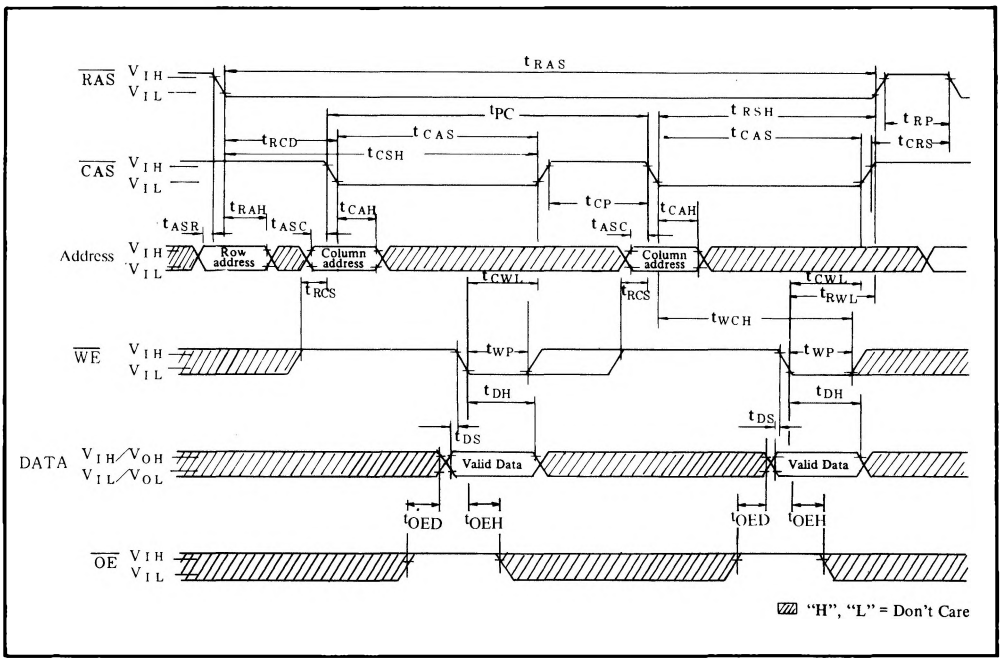
PAGE MODE READ CYCLE



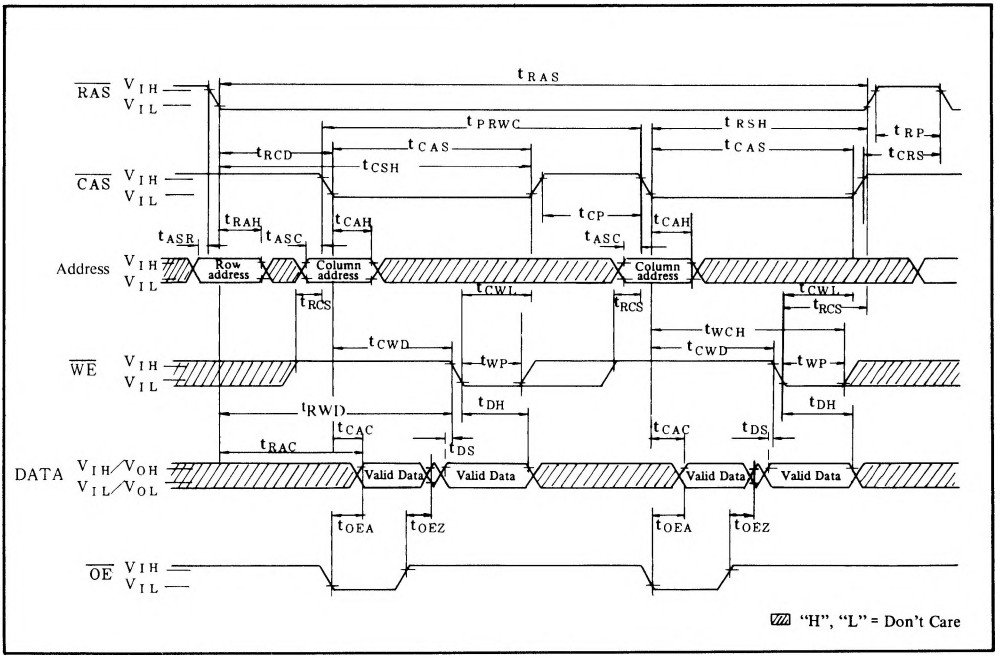
PAGE MODE WRITE CYCLE



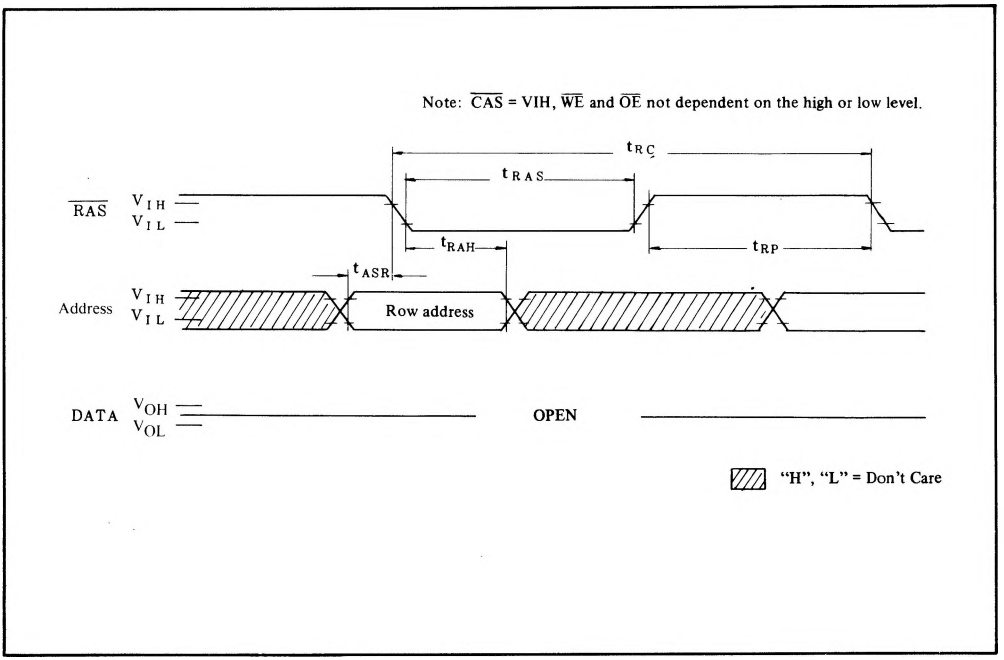
PAGE MODE $\overline{OE}$ WRITE CYCLE



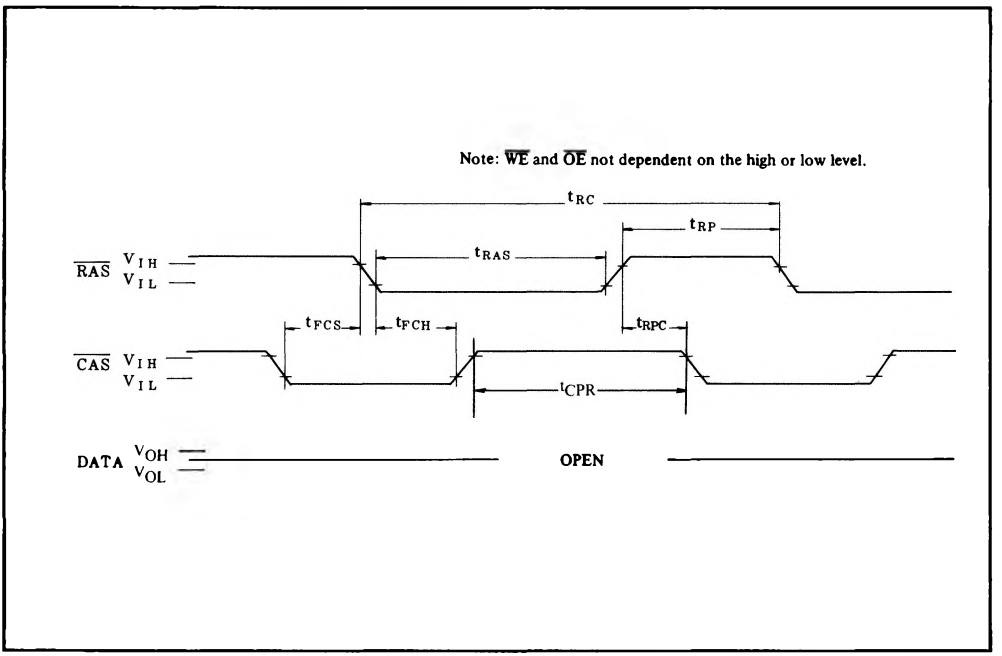
PAGE MODE READ/WRITE CYCLE



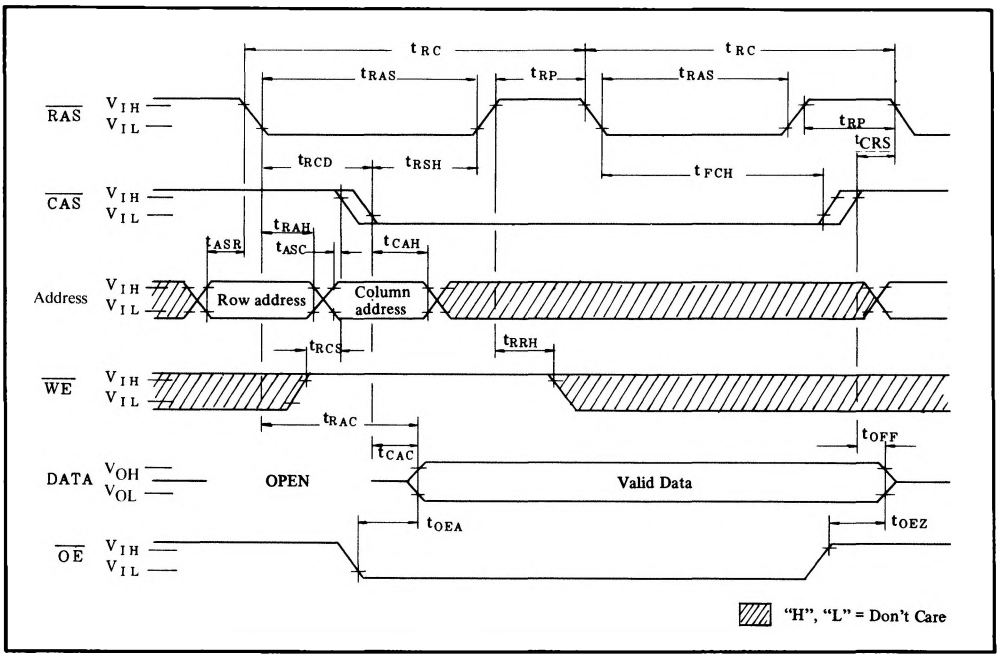
RAS ONLY REFRESH CYCLE



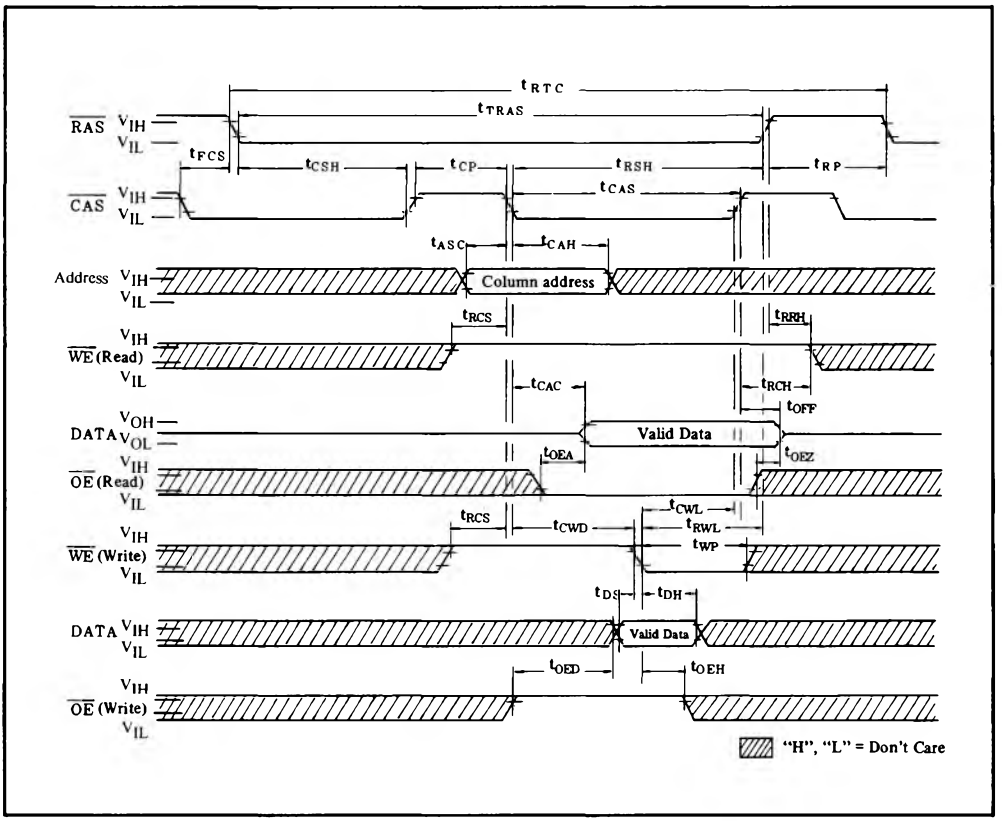
CAS BEFORE RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

16 bits of binary address input are required to decode any one of the 65,536 words by 4 bit storage cell locations.

8 row-address bits are set up on address input pins A_0 through A_7 and latched onto the chip by the row address strobe (RAS). Then 8 column-address bits are set up on pins A_0 through A_7 and latched onto the chip by the column address strobe (CAS).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ or $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every four milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 (A_0 to A_7) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  – Bits A_0 through A_7 are defined by the refresh counter.
* A COLUMN ADDRESS
  – All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41464 Bit Map (Physical-Decimal)

□ Pin 18

DQ1 DQ2 DQ3 DQ4

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253	253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
253	253	253	253	253	253	253	253	253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128

COLUMN DECODER

REFRESH ADDRESS (0 – 255)

REFRESH ADDRESS (0 – 255)

□ Pin 9

A
B

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)