OKI semiconductor

MSM5055

CMOS 4 BIT SINGLE CHIP VERY LOW POWER MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

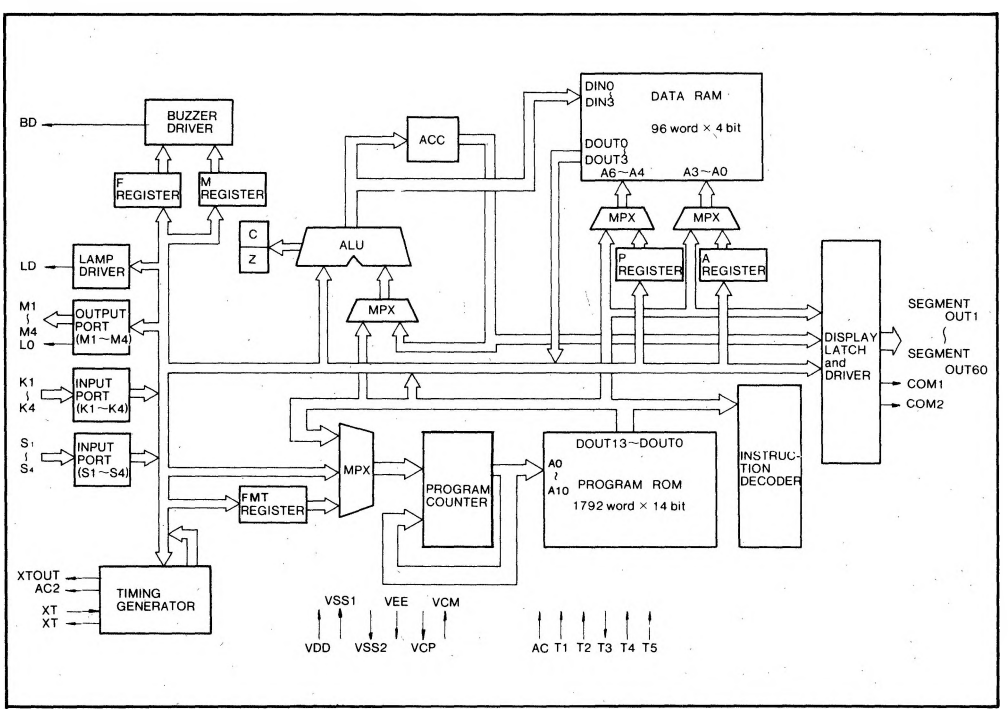
The OKI MSM5055 is a low-power, high-performance single-chip microcontroller employing complementary metal oxide semiconductor technology. Integrated onto a single chip are 4 bits of ALU, 25K bits of mask programmable ROM, 384 bits of data RAM, crystal oscillator, voltage doubler, timer, LCD driver, input port, output port and interface circuit for voice LSI (MSM6212).

The MSM5055 is widely used in electronic products requiring low power operation, for example, multi-functioned watches, voice synthesizer watches and games.

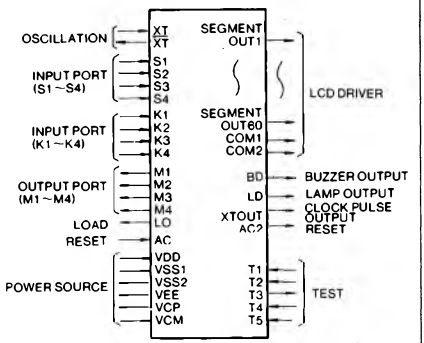
FEATURES

- Low Power Consumption 3 μA Typical
- 1792 × 14 Internal ROM
- 96 × 4 Internal RAM
- 4 × 2 Input Port
- 4 × 1 Output Port
- 4 × 4 Key Matrix Input (K1~K4, M1~M4)
- 60 LCD Driver
  (1/2 Duty, 1/2 Bias, 120 Segment)
- 42 Instructions
- 1.5 V or 3 V Operating Voltage
  (Masking Option)
- 32.768 kHz Crystal Oscillator
- 122.1 μS Instruction Cycle
- −20 to 75°C Operating Temperature
- 94 pad die

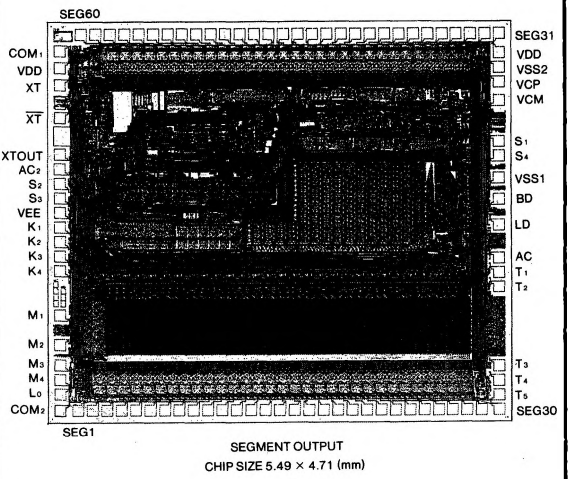
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



CHIP PAD LAYOUT



SEGMENT OUTPUT
CHIP SIZE 5.49 × 4.71 (mm)

PIN DESCRIPTION

Designation	Function
V_{DD}	Circuit ground potential
V_{SS_1}	Power source (−1.5 V)
V_{SS_2}	Power source for LCD driver (−3.0 V) This terminal is connected to V_{DD} terminal through a 0.1 μF capacitor.
V_{EE}	Power source for internal logic (−1.5 to −3.0 V) This terminal is connected to V_{DD} terminal through a 0.1 μF capacitor.
V_{CP}, V_{CM}	Booster capacitor connection terminals V_{CP} terminal is connected to V_{CM} terminal through a 0.1 μF capacitor.
XT, $\overline{XT}$	Input and output terminals of oscillator inverter, 32.768 kHz crystal is connected to these terminals.
T1 ～ T5	Terminals to test internal logic, T1 ～ T3 and T5 are pulled down to V_{SS_1}. T4 is output. Test pins must be normally open.
AC	Terminal to clear internal logic pulled down to V_{SS_1}. After power is turned on, the MSM5055 must be reset by this terminal.
BD	Buzzer output
LD	Lamp output
LO	Load data terminal of M_1 to M_4
AC2	Reset terminal for external circuit
XT OUT	Clock output for external circuit

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5055 is given on page 104. Each block of logic will be briefly discussed. For more information, please refer to the MSM5055 user's manual.

Program ROM

The MSM5055 addresses up to 1 K word of internal mask programmable ROM. Each word consists of 14 bits, and all instructions are one word. The instructions are routed to a programmed logic array which generates the signals necessary for control of logic.

Data RAM

Data is organized in 4-bit nibbles. Internal data RAM consists of 62 nibbles.

The RAM is addressed by page address and column address. Normally page address is specified by the page register, but direct addressing is available in Page 0.

Column address is directly addressed by the operand of various instructions.

ALU

The ALU performs 4-bit parallel operation of RAM and ACC contents, or RAM contents and an immediate digit. It sets or resets the flags (Z, C) depending on the condition.

Program Counter (PC)

The program counter is 10 bits wide and specifies the address of the program ROM.

The PC is incremented by one at every execution of the instruction, and then specifies the next instruction to be executed. However, the contents of the PC are rewritten by the execution of the Jump or Branch instruction.

There is no boundary in the ROM, so the Jump or Branch instruction can be put anywhere in the ROM.

Input/Output Port

Input Port (S1 ~ S4)

The input port (S1 ~ S4) is a 4-bit parallel input port. Each pin of the port is pulled down to V_{SS1} by an internal resistor, and the status of the port is fetched by the SWITCH instruction.

Input Port (K1 ~ K4)

The input port (K1 ~ K2) is a 2-bit parallel input port. Each pin of the port is pulled down to V_{SS1} by an internal resistor, and the status of the port is fetched by the KSWITCH instruction.

Output Port (M1 ~ M4)

The output port (M1 ~ M4) is a 4-bit parallel output port. This port consists of data latches and buffers, and the contents of the data latches are rewritten by a matrix instruction.

Display Function

The MSM5055 is provided with a segment output terminal which can directly drive a 1/2 bias, 1/2 duty LCD, and the common drive output terminal COM1 and COM2. The segment drive circuit consists of the display data latch, multiplexer and driver. If the data is sent to the display data latch with a display instruction, the LCD drive waveform is output to the segment drive output terminal.

Time Base

The time base of the CPU is provided by connecting a 32.768 kHz crystal to the XT and $\overline{XT}$ pins. One machine cycle is 122.1 μs.

A hardware divider of up to 1 Hz is provided, enabling programs to implement a clock function by counting signals between 32 and 1 Hz.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage 1	$V_{DD} - V_{SS_1}$	Ta = 25°C	−0.3 to +2.0	V
Supply Voltage 2	$V_{DD} - V_{SS_2}$	Ta = 25°C	−0.3 to +4.0	V
Supply Voltage 3	$V_{DD} - V_{EE}$	Ta = 25°C	−0.3 to +4.0	V
Input Voltage	V_{IN_1}	Ta = 25°C	V_{SS_1} −0.3 to +0.3	V
Storage Temperature	Tstg		−55 to 125	°C

OPERATING CONDITIONS

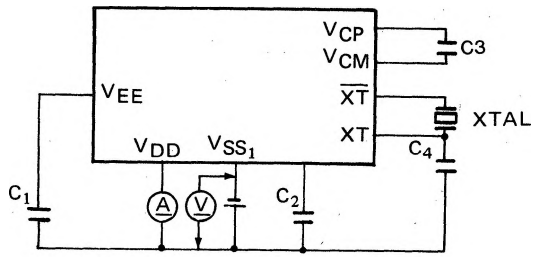
Parameter	Symbol	Limits	Unit
Operating Voltage	$V_{DD} - V_{SS_1}$	1.25 to 1.65	V
Operating Temperature	Topr	−20 to 75	°C

DC CHARACTERISTICS

(VDD =0V, V_{SS_1}, V_{EE} = −1.55V, V_{SS_2} = −3.0V, C_l = 30kΩ, Ta = 25°C)

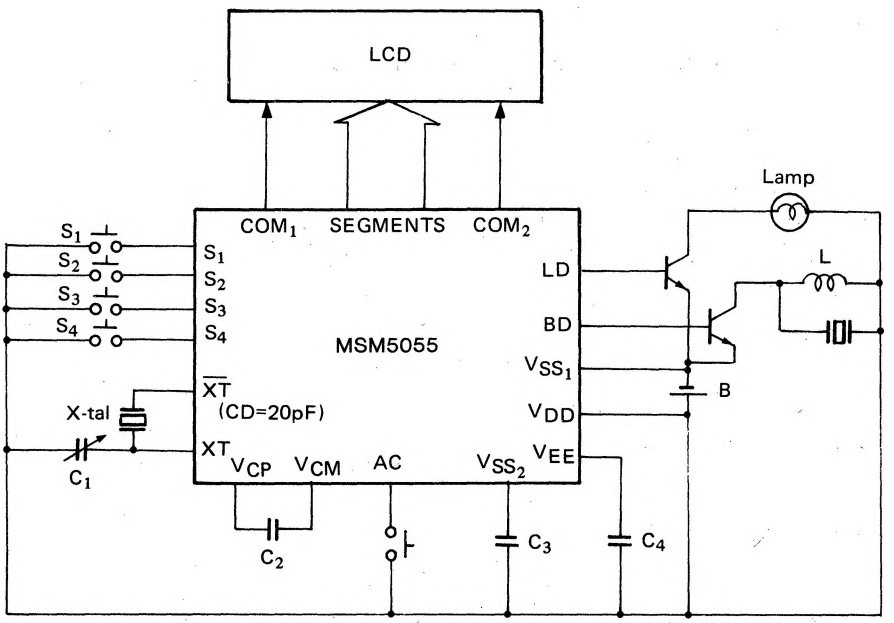
Parameter	Symbol	Conditions		Limits			Unit
				Min.	Typ.	Max.	
Power supply current	I_{DD}			−	3.0	−	μA
Oscillation start voltage	$-V_{OSC}$	Within 5 seconds V_{SS_1} terminal		1.45	−	−	V
Output current 1 COM	I_{OH_1}	V_{OH_1} = −0.2V		−4	−	−	μA
	I_{OM_1}	$V_{OM_1} = V_{SS_1} \pm 0.2V$		4/−4	−	−	
	I_{OL_1}	V_{OL_1} = −2.8V		4	−	−	
Output current 2 SEGMENT	I_{OH_2}	V_{OH_2} = −0.2V		−0.4	−	−	μA
	I_{OL_2}	V_{OL_2} = −2.8V		0.4	−	−	
Output current 3 AC2 LOAD, XTOUT	I_{OH_3}	V_{OH_3} = −0.5V		−10	−	−	μA
	I_{OL_3}	V_{OL_3} = −1.05V		10	−	−	
Output current 4 M1～M4	I_{OH_4}	V_{OH_4} = −0.5V		−100	−	−	μA
	I_{OL_4}	V_{OL_4} = −1.0V		1.5	−	12.7	
Output current 5 LD	I_{OH_5}	V_{OH_5} = −0.55V	V_{SS_1} = −1.25V, V_{EE} = −2.4V, V_{SS_2} = −2.4V	−21.6	−	−83	μA
	I_{OL_5}	V_{OL_5} = −1.15V		1	−	−	
Output current 5 BD	I_{OH_6}	V_{OH_6} = −0.4V	V_{SS_1} = VEE = −1.25V, V_{SS_2} = −2.4V	−50	−	−	μA
	I_{OH_6}	V_{OL_6} = −0.8V		−	5	−	
Input current 1 S_1 ～ S_4	I_{IH_1}	V_{IH_1} = 0V		1	10	50	μA
	I_{IL_1}	V_{IL_1} = −1.55V		−	−	−0.2	
Input current 2 K_1～K_4	I_{IH_2}	V_{IH_2} = 0V		2.5	6	12	μA
	I_{IL_2}	V_{IL_2} = −1.55V		−	−	−0.2	
Oscillator built-in capacitor	CD			−	20	−	pF

MEASURING CIRCUIT



C1 . C2 . C3 : 0.1 μF
C4 : 30 pF
X-tal : 32.768 kHz

TYPICAL APPLICATION



C1 : 5 ~ 35pF
C2, C3, C4 : 0.1μF
B : 1.5V
L : 20mH

DESCRIPTION OF INSTRUCTIONS

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Arithmetic operation	ADD ACC, AP	0	0	0	0	0	P	0	1	0	0		A			AP ← (AP) + (ACC)
	ADD #D, AP	0	1	1	0	0	P		D				A			AP ← (AP) + D
	SUB ACC, AP	0	0	0	0	1	P	0	1	0	0		A			AP ← (AP) − (ACC)
	SUB #D, AP	0	1	1	0	1	P		D				A			AP ← (AP) − D
	ADJUST N, AP	1	1	0	0	0	P		$\overline{N}+1$				A			AP ← N adjust {(AP)}
	CMP ACC, AP	0	0	0	0	1	P	1	1	1	0		A			(AP) − (ACC)
	CMP #D, AP	0	1	0	1	1	P		D				A			(AP) − D
	INC AP	0	1	1	0	0	P	0	0	0	1		A			AP ← (AP) + 1
	DEC AP	0	1	1	0	1	P	0	0	0	1		A			A ← (AP) − 1
	XOR ACC, AP	0	0	0	0	0	P	0	1	1	1		A			AP ← (AP) $\forall$ (ACC)
	XOR #D, AP	0	1	1	1	1	P		D				A			AP ← (AP) $\forall$ D
Bit operation	BIT ACC, AP	0	0	0	0	0	P	1	1	1	0		A			(AP) V $\overline{(ACC)}$
	BIT #D, AP	0	1	0	1	0	P		D				A			(AP) V $\overline{D}$
	BIS ACC, AP	0	0	0	0	0	P	0	1	1	0		A			AP V (ACC)
	BIS #D, AP	0	1	0	0	0	P		D				A			(AP) V D
	BIC ACC, AP	0	0	0	0	1	P	0	1	1	0		A			AP $\wedge$ $\overline{(ACC)}$
	BIC #D, AP	0	1	0	0	1	P		D				A			AP $\wedge$ $\overline{D}$
Shift	ASR AP	0	0	0	0	0	P	0	0	1	1		A			↳(C) 0 → (AP)┘
	ASL AP	0	0	0	0	1	P	0	0	1	1		A			(C) ← (AP) ← 0
Flag operation	CLZ	0	0	0	0	0	0	1	0	1	0	0	0	0	0	Z ← 0
	CLC	0	0	0	0	0	0	1	0	0	1	0	0	0	0	C ← 0
	CLA	0	0	0	0	0	0	1	0	1	1	0	0	0	0	Z ← 0, C ← 0
	SEZ	0	0	0	0	1	0	1	0	1	0	0	0	0	0	Z ← 1
	SEC	0	0	0	0	1	0	1	0	0	1	0	0	0	0	C ← 1
	SEA	0	0	0	0	1	0	1	0	1	1	0	0	0	0	Z ← 1, C ← 1
Data transfer	MOV ACC, AP	1	1	1	1	0	P	0	0	0	0		A			AP ← (ACC)
	MOV ACC, AX	1	1	1	1	0	0	0		X			A			AX ← (ACC)
	MOV #D, AP	0	1	1	1	0	P		D				A			AP ← D
	MOV AP, ACC	1	1	1	1	1	P	0	0	0	0		A			ACC ← (AP)
	MOV AX, ACC	1	1	1	1	1	0	0		X			A			ACC ← (AX)
Jump	JMP adrs	1	0	0	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	PC ← adrs
	JMP @AP	0	0	0	0	0	P	1	1	0	1		A			PC ← (PC) + (AP) + 1
	JMPIO @AP	0	0	0	0	1	P	1	1	0	1		A			PC ← (PC) + {(AP) $\wedge$ 7H} +1
	BEQ +n BZE +n	0	0	0	1	1	0	0	1	0	n_4	n_3	n_2	n_1	n_0	PC ← (PC)+n+1, if Z=1

DESCRIPTION OF INSTRUCTIONS (CONT.)

	Mnemonic	Instruction Code 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Operation
Jump	BNE +n BNZ +n	0 0 0 1 1 0 1 1 0 n_4 n_3 n_2 n_1 n_0	PC ← (PC)+n+1, if Z=0
	BCS +n	0 0 0 1 1 0 0 0 0 n_4 n_3 n_2 n_1 n_0	PC ← (PC)+n+1, if C=1
	BCC +n	0 0 0 1 1 0 1 0 0 n_4 n_3 n_2 n_1 n_0	PC ← (PC)+n+1, if C=0
Input/Output	SWITCH AP	1 1 0 1 0 P 0 0 0 1 A	AP ← INPUT PORT (S1 ~ S4)
	KSWITCH AP	1 1 0 1 0 P 0 0 1 0 A	AP ← INPUT PORT (K1 ~ K4)
	MATRIX AP	1 1 0 1 1 P 0 0 1 0 A	OUTPUT PORT (M1 ~ M4) ←(AP)
	MATRIX Mn	0 0 0 1 0 0 0 0 1 0 M_4 M_3 M_2 M_1	OUTPUT PORT (M1~M4) ← Mn (n=1, 2, 3, 4)
	XTCP ON/OFF	0 0 0 1 0 0 1 0 0 0 0 0 b_1 b_0	XTOUT ON/OFF
	FREQ N	0 0 0 1 0 0 1 1 0 1 N	Freq ← N
	BUZZER sound	0 0 0 1 0 0 1 1 0 0 b_3 b_2 1 0	Mreg ← sound, Buzzer start
	BSO	0 0 0 1 0 0 1 1 0 0 0 0 0 0	Buzzer stop
	LAMP ON/OFF	0 0 0 1 0 0 0 0 0 1 0 0 b_1 b_0	LD ON/OFF
Display	DSP digit, AP	0 0 1 0 0 P digit A	Digit (Low part) ← (AP), (ACC)
	DSPH digit, AP	0 0 1 0 1 P digit A	Digit (High part) ← (AP), (ACC)
	FORMAT AP	1 1 0 1 1 P 0 0 1 1 A	FMT reg. ← (AP)
	FORMAT N	0 0 0 1 0 0 0 0 1 1 N	FMT reg. ← N
	DSPF digit, AP	0 0 1 1 0 P digit A	Digit (Low part) ← (AP) via table
	DSPFH digit, AP	0 0 1 1 1 P digit A	Digit (High part) ← (AP) via table
CPU Control & Others	HALT	0 0 0 1 0 0 0 0 0 0 0 0 0 0	Halt
	INTENAB 32/16	0 0 0 1 0 0 1 0 1 1 1 0 0 0	Enable timer
		0 0 0 1 0 0 0 1 0 0 0 0 1 0	
	INTDSAB 32/16	0 0 0 1 0 0 1 0 1 1 0 1 0 0	Disable timer
		0 0 0 1 0 0 0 1 0 0 0 0 0 1	
	INTMODE AP	1 1 0 1 0 P 0 1 0 0 A	AP ← Interrupt mode
	PAGE A0	1 1 0 1 1 0 0 1 0 1 A	Preg ← (A0)
	PAGE N	0 0 0 1 0 0 0 1 0 1 N	Preg ← N
	ADRS AP	1 1 0 1 1 P 0 1 1 0 A	Areg ← (AP)
	ADRS N	0 0 0 1 0 0 0 1 1 0 N	Areg ← N
	RATE AP	1 1 0 1 0 P 1 0 0 1 A	AP ← DIVIDER (8 Hz~1 Hz)
	RSTRATE	0 0 0 1 0 0 1 0 0 0 1 0 0 0	DIVIDER (8 Hz~1 Hz) ← 0
	BACKUP ON/OFF	0 0 0 1 0 0 0 0 0 1 b_3 b_2 0 0	Backup ON/OFF
	NOP	0 0 0 0 0 0 0 0 0 0 0 0 0 0	No operation