Preliminary

OKI semiconductor

MSM51257RS/JS

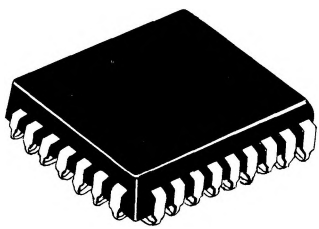
32,768-WORD x 8-BIT CMOS STATIC RAM

GENERAL DESCRIPTION

The MSM51257RS/JS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257RS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

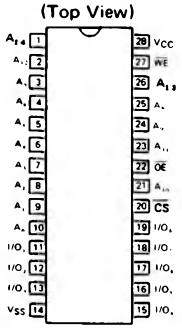
FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 5.5 mW MAX
  Operation; 385mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 32-pin PLCC



PIN CONFIGURATION

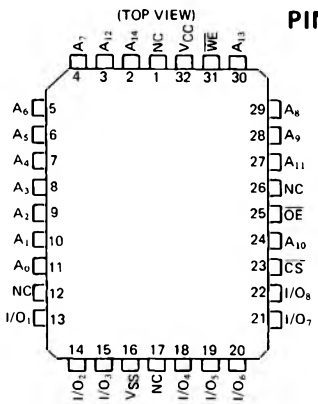
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION

(TOP VIEW)



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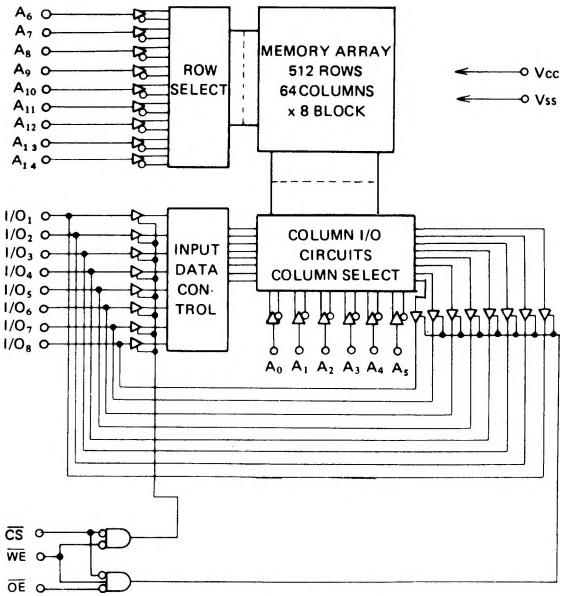
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Wreite	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		0.02	1	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE

AC CHARACTERISTICS

Test Condition

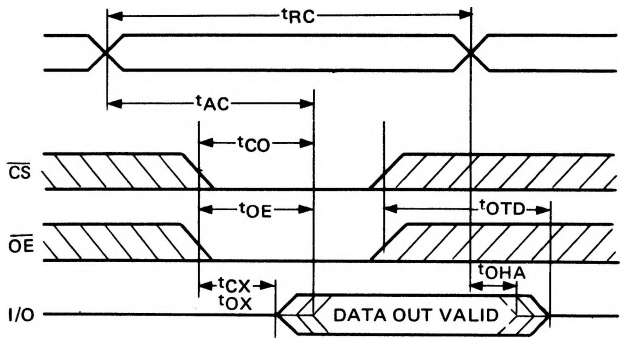
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Deselection	t_{OTD}	0	30	0	35	0	40	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and ahigh $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

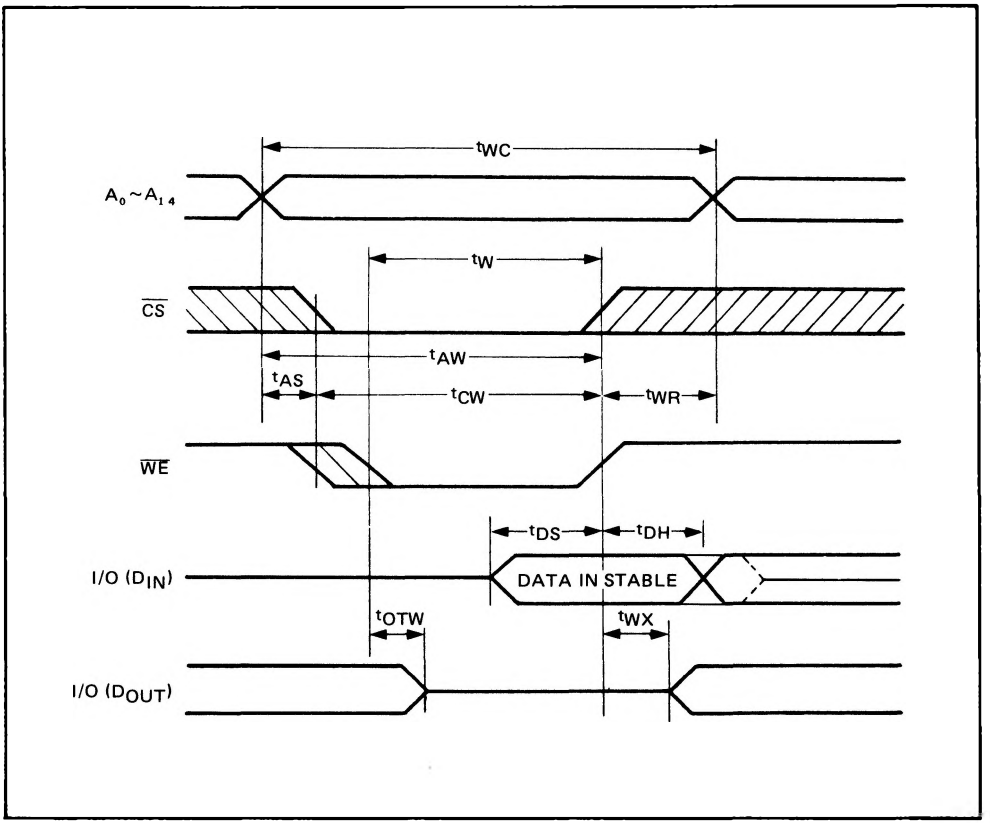
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257-85		MSM51257-10		MSM51257-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	65		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	35		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	35	0	40	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		15		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.