OKI semiconductor

MSM5126RS

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-014-32)

GENERAL DESCRIPTION

The MSM5126RS is a 2048-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5126RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 30μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

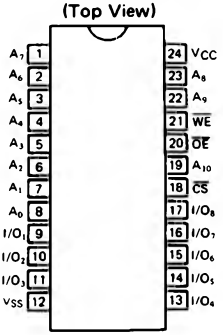
A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −30°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX T_a = 25°C
    5.0 μA MAX T_a = 60°C
    30 μA MAX T_a = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5126-20/25; 200 ns/250 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  16K EPROM (MSM2716)
  16K NMOS SRAM (MSM2128)

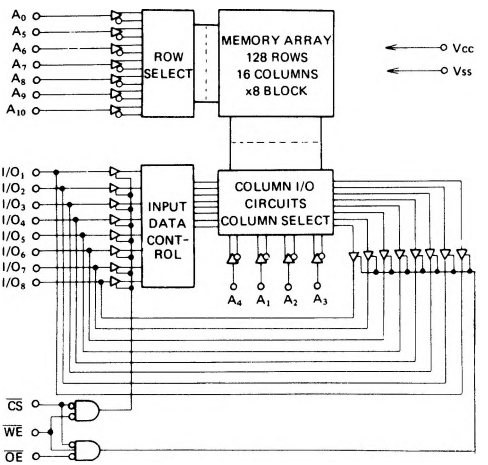
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−30 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ±10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	Test Condition		MSM5126-20/25			Unit
				Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}		−5		5	μA
Output Voltage	V_{OH}	I_{OH} = −1 mA		2.4			V
	V_{OL}	I_{OL} = 2.0 mA				0.4	V
Standby Supply Current	I_{CCS}	CS ≧ V_{CC} − 0.5V V_{CC} = 2V to 5.5V V_I = 0 to V_{CC}	Ta = 25°C		0.05	1.0	μA
			Ta = 60°C			5.0	
			Ta = 85°C			30	
	I_{CCS_1}	$\overline{CS}$ = V_{IH} t_{CYC} = Min. cycle			1	3	mA
Operating Supply Current	I_{CCA}	$\overline{CS}$ = 0V, V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0 mA			40	70	mA
		$\overline{CS}$ = 0V, V_{IN} = V_{CC}/G_{ND}, I_{OUT} = 0 mA			30	55	mA

AC CHARACTERISTICS

Test Condition

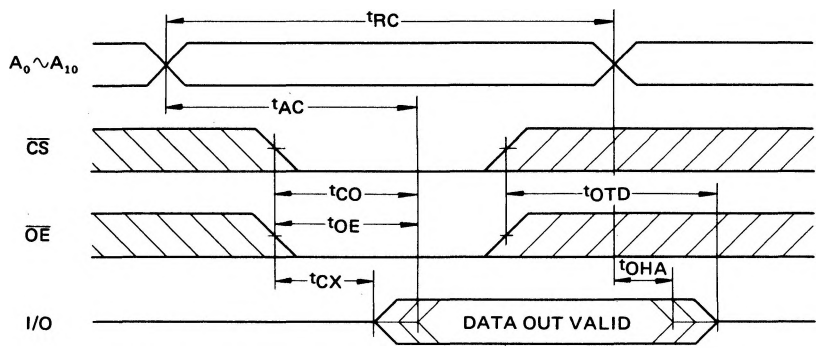
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	2.2V 0.8V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20		MSM5126-25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		250		ns
Address Access Time	t_{AC}		200		250	ns
Chip Select Access Time	t_{CO}		200		250	ns
Output Enable to Output Valid	t_{OE}		100		100	ns
Chip Selection to Output Active	t_{CX}	10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		10		ns
Output 3-state from Deselection	t_{OTD}	0	80	0	80	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

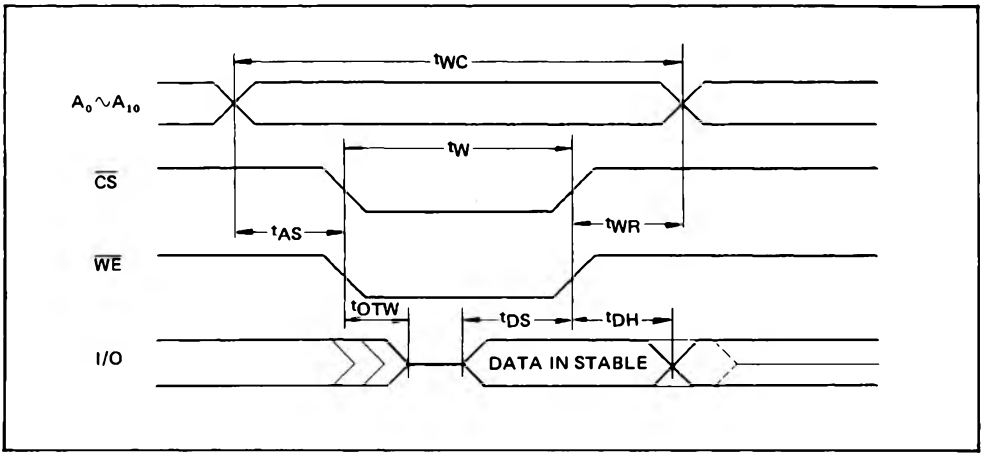
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20		MSM5126-25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		250		ns
Address to Write Setup Time	t_{AS}	0		0		ns
Write Time	t_W	160		200		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	80		120		ns
Data Hold from Write Time	t_{DH}	0		0		ns
Output 3-State from Write	t_{OTW}		80		80	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

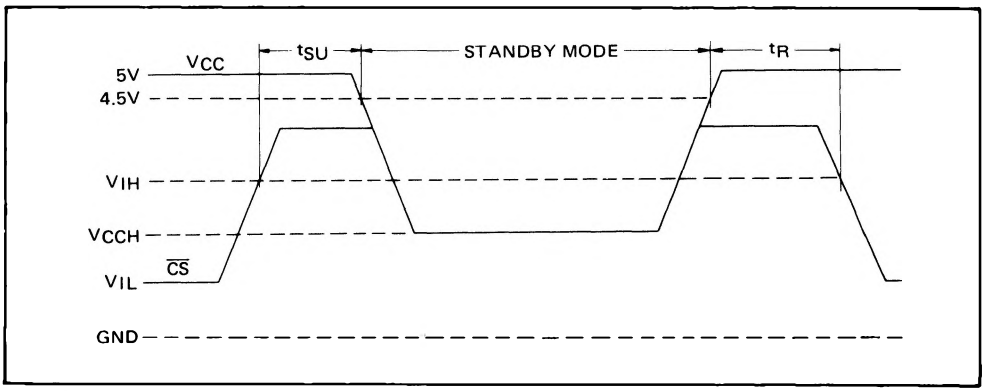
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −30°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}, CS = V_{CC}
Data Retention Current	I_{CCH}		0.05	30	μA	V_{CC} = 2V to 5.5V, V_I = 0V to V_{CC} CS ≧ = V_{CC} − 0.5V
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$		5	10	pF
Input Capacitance	C_{IN}		5	10	pF

Note: This parameter is periodically sampled and not 100% tested.