MSM514221B 632 296/302

262,263-Word × 4-Bit Field Memory

DESCRIRTION

The OKI MSM514221B is a high performance 1M-bit, 256K × 4-bit, Field Memory especially designed for high-speed serial access applications such as HDTVs, conventional NTSC TVs, VTRs, digital movies and Multi-media systems. MSM514221B is FRAM for wide or low end use as general commodity TVs and VTRs, exclusively. MSM514221B is not designed for the other use or high end use as medical systems, professional graphics systems require long time picture storage, data storage systems and others. The 1M-bit capacity fits for one field of conventional NTSC TV screen.

Each of the 4-bit planes has separate serial write and read ports that employ independent control clocks to support asynchronous read and write operations. Different clock rates are also supported that allow alternate data rates between write and read data streams.

The MSM514221B provides high speed FIFO, First-In First-Out, operation without external refreshing: MSM514221B refreshes its DRAM storage cells automatically, so that it appears fully static to the users.

Moreover, fully static type memory cells and decoders for serial access enable the serial access operation refresh free, so that serial read and/or write control clock can be halted high or low for any time as long as the power is on. Internal conflicts of any memory access and refreshing operation are prevented by special arbitration logic.

The MSM514221B's function is simple like that of a digital delay device whose delay-bit-length is easily set by reset timing. The delay length, number of read delay clocks between write and read, is determined by externally controlled write and read reset timings.

Additional SRAM serial registers, or line buffers, for the initial access of 256 × 4-bit enable high speed first-bit-access with no clock delay just after the write or read reset timings.

The MSM514221B is similar in operation and functionality to OKI 2M-bit Field memory MSM518221.

FEATURES

- 512 Rows × 512 Column × 4-bit
- Fast FIFO (First-in First-out)operation
- High speed asynchronous serial access

Read/Write cycle time	30ns/40ns/60ns
Access time	25ns/30ns/50ns

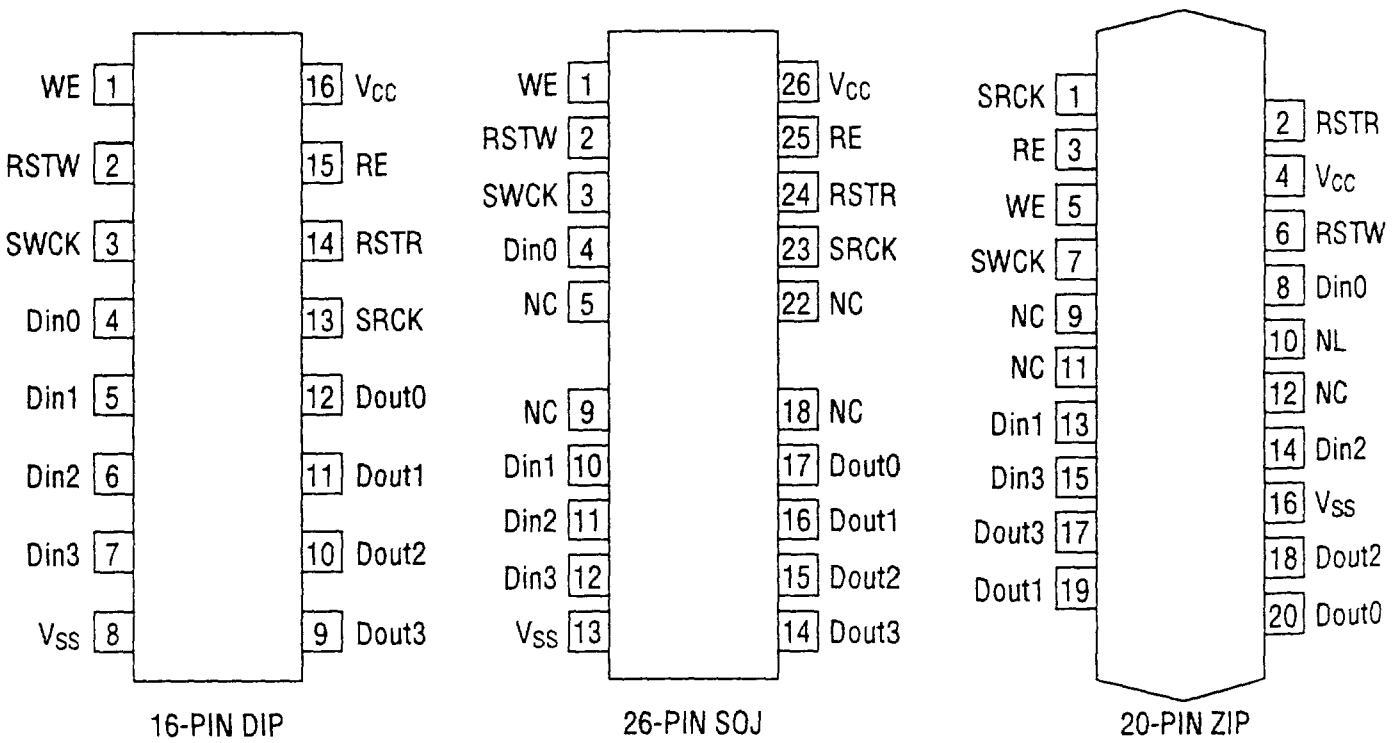
- Functional compartibility with OKI MSM518221
- Self refresh (No refresh control is required)
- Package:

16-Pin 300mil	Plastic DIP	(DIP16-P-300-W1)
26-Pin 300mil	Plastic SOJ	(SOJ26-P-300)
20-Pin 400mil	Plastic ZIP	(ZIP20-P-400)

PRODUCT FAMILY

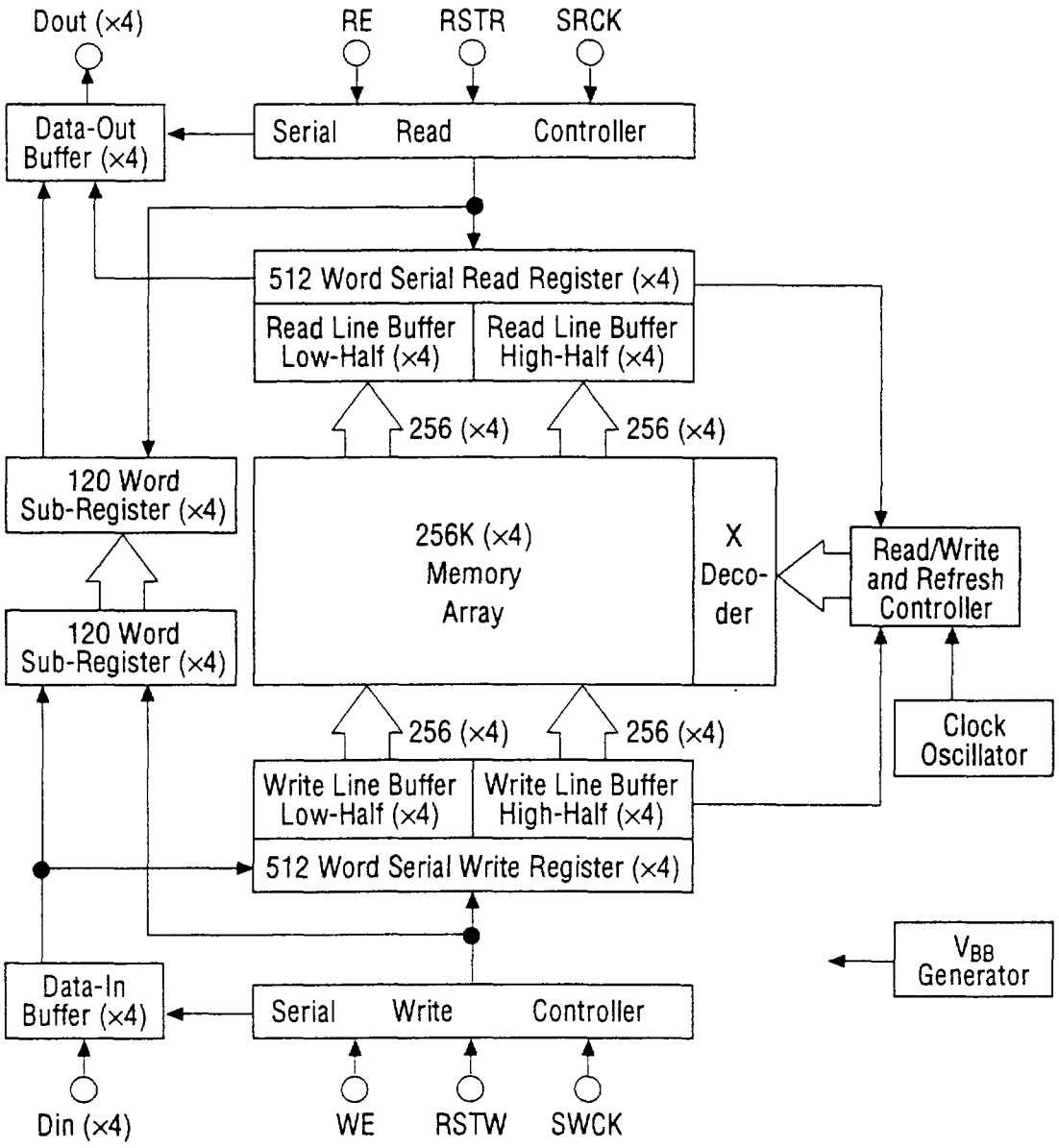
Family	Cycle Time (Min.)	Access Time (Max.)	Package
MSM514221B-RS-30	30ns	25ns	300mil 16-Pin DIP
MSM514221B-RS-40	40ns	30ns	300mil 16-Pin DIP
MSM514221B-RS-60	60ns	50ns	300mil 16-Pin DIP
MSM514221B-JS-30	30ns	25ns	300mil 26-Pin SOJ
MSM514221B-JS-40	40ns	30ns	300mil 26-Pin SOJ
MSM514221B-JS-60	60ns	50ns	300mil 26-Pin SOJ
MSM514221B-ZS-30	30ns	25ns	400mil 20-Pin ZIP
MSM514221B-ZS-40	40ns	30ns	400mil 20-Pin ZIP
MSM514221B-ZS-60	60ns	50ns	400mil 20-Pin ZIP

PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
SRCK	Serial Read Clock
SWCK	Serial Write Clock
WE	Write Enable
RE	Read Enable
RSTW	Write Reset Clock
RSTR	Read Reset Clock
Din0 - 3	Data Input
Dout0 - 3	Data Output
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection
NL	No Lead

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Write Operation

The write operation is controlled by tree clock, SWCK, RSTW, and WE. Write operation is accomplished by cycling SWCK and holding WE high after write address pointer reset operation or RSTW.

Each write operation, which begins after RSTW, must contain at least 130 active write cycles, i.e. SWCK cycles while WE is high. To transfer the last data, which at that time are stored in the serial data registers attached to DRAM array, to the DRAM array, an RSTW operation is required after the last SWCK cycle.

Write Reset: RSTW

The first positive transition of SWCK after RSTW going high resets the write address counters to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. Because the write reset function is solely controlled by SWCK rising edge after high level of RSTW, the states of WE are don't care in the write reset cycle.

Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

Data Inputs: Din0 - 3
Write Clock: SWCK

The SWCK latches the input data on chip when WE is high and also increments the internal write address pointer. Data-in setup time, t_{DS} and hold time, t_{DH}, are referenced to the rising edge of SWCK.

Write Enable: WE

WE is used for data write enable/disable control. WE high level enables the input, and WE low level disables the input and holds the internal write address pointer. There are no WE disable time (low) and WE enable time (high) restrictions because MSM514221B is fully static operation as long as power is on. Note that WE setup and hold times are referenced to the rising edge of SWCK.

Read Operation

The read operation is controlled by tree clocks, SRCK, RSTR, and RE. Read operation is accomplished by cycling SRCK and holding RE high after read address pointer reset operation or RSTR. Each read operation, which begins after RSTR, must contain at least 130 active read cycles, i.e. SRCK cycles while RE is high.

Read Reset: RSTR

The first positive transition of SRCK after RSTR going high resets the read address counters to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. Because the read reset function is solely controlled by SRCK rising edge after high level of RSTR the states of RE are don't care in the read reset cycle.
Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

Data Out : Dout0 - 3
Read Clock : SRCK

Data is shifted out of the data registers triggered by the rising edge of SRCK when RE is high during a read operation. The SRCK input increments the internal read address pointer when RE is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the rising edge of SRCK. There are no output valid time restriction on MSM514221B.

Read Enable: RE

The function of RE is gating of the SRCK clock, for incrementing the read pointer. When RE is high before the rising edge of SRCK, the read pointer is incremented. When RE is low, the read pointer is not incremented. RE setup times (t_{RENS} and t_{RDSS}) and RE hold times (t_{RENH} and t_{RDSH}) are referenced to the rising edge of the SRCK clock.

Power-up and Initialization

On Powering up, the device is designed to begin proper operation after at least 100μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. After this 100 μs stabilization interval, the following initialization sequence must be performed.

Because the read and write address counters are not valid after power-up, a minimum of 130 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW operation and an RSTR operation, to properly initialize the write and the read address pointer. Dummy write cycles/RSTW and dummy read cycles/RSTR may occur simultaneously.

If these dummy read and write operations start while V_{CC} and/or the substrate voltage have not stabilized, it is required to perform an RSTR operation plus a minimum of 130 SRCK cycles plus another RSTR operation, and an RSTW operation plus a minimum of 130 SRCK cycles plus another RSTW operation to properly initialize read and write address pointers.

Old/New Data Access

There must be minimum delay of 600 SWCK cycles between writing into memory and reading out from memory if reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as may as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 119 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called "old data".

In order to read out "new data", i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be "old data" or "new" data or a combination of old and new data. Such a timing should be avoided.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating
Input Output Voltage	V_T	at Ta = 25°C, V_{SS}	–1.0 to 7.0V
Output Current	I_{OS}	Ta = 25°C	50mA
Power Dissipation	P_D	Ta = 25°C	1W
Operating Temperature	T_{opr}	—	0 to 70°C
Storage Temperature	T_{stg}	—	–55 to 150°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Power Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	V_{CC}	V_{CC} + 1	V
Input Low Voltage	V_{IL}	–1.0	0	0.8	V

DC Characteristics

Parameter	Symbol	Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC} + 1$, Other Pins Tested at V = 0V		–10	10	µA
Output Leakage Current	I_{LO}	$0 < V_O < V_{CC}$		–10	10	µA
Output "H" Level Voltage	V_{OH}	I_{OH} = –5mA		2.4	—	V
Output "L" Level Voltage	V_{OL}	I_{OL} = 4.2mA		—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time, Output Open	–30	—	50	mA
			–40	—	45	
			–60	—	35	
Standby Current	I_{CC2}	Input Pin = V_{IH}/V_{IL}		—	10	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (Din, SWCK, SRCK, RSTW, RSTR, WE, RE)	Ci	7	pF
Output Capacitance (Dout)	Co	7	pF

AC Characteristics

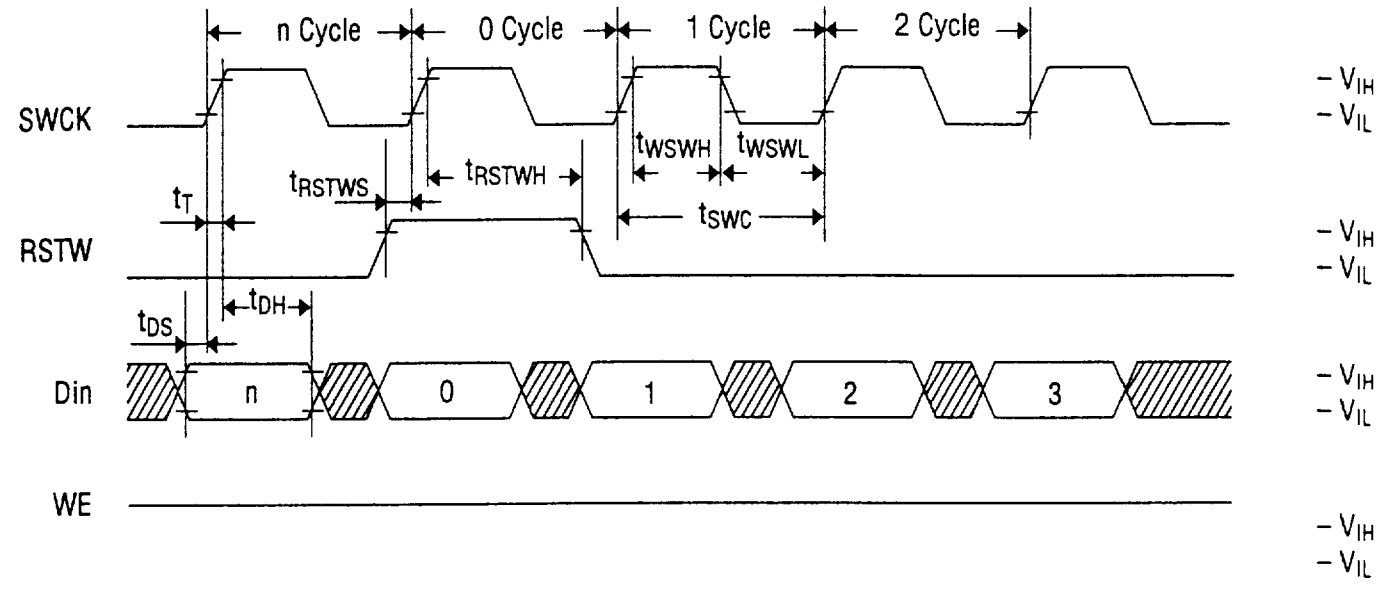
(V_{CC} = 5V±10%, Ta = 0 to 70°C)

Parameter	Symbol	MSM514221B-30		MSM514221B-40		MSM514221B-60		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Access Time from SRCK	t_{AC}	6	25	6	30	6	50	ns
Dout Hold Time from SRCK	t_{DDCK}	6	—	6	—	6	—	ns
Dout Enable Time from SRCK	t_{DECK}	6	25	6	25	6	25	ns
Dout Hold Time from RE	t_{DDRE}	9	—	9	—	9	—	ns
SWCK "H" Pulse Width	t_{WSWH}	12	—	17	—	17	—	ns
SWCK "L" Pulse Width	t_{WSWL}	12	—	17	—	17	—	ns
Input Data Setup Time	t_{DS}	5	—	5	—	5	—	ns
Input Data Hold Time	t_{DH}	6	—	6	—	6	—	ns
WE Enable Setup Time	t_{WENS}	0	—	0	—	0	—	ns
WE Enable Hold Time	t_{WENH}	5	—	5	—	5	—	ns
WE Disable Setup Time	t_{WDSS}	0	—	0	—	0	—	ns
WE Disable Hold Time	t_{WDSH}	5	—	5	—	5	—	ns
WE "H" Pulse Width	t_{WWEH}	5	—	10	—	10	—	ns
WE "L" Pluse Width	t_{WWEL}	5	—	10	—	10	—	ns
RSTW Setup Time	t_{RSTWS}	0	—	0	—	0	—	ns
RSTW Hold Time	t_{RSTWH}	10	—	10	—	10	—	ns
SRCK "H" Pulse Width	t_{WSRH}	12	—	17	—	17	—	ns
SRCK "L" Pulse Width	t_{WSRL}	12	—	17	—	17	—	ns
RE Enable Setup Time	t_{RENS}	0	—	0	—	0	—	ns
RE Enable Hold Time	t_{RENH}	5	—	5	—	5	—	ns
RE Disable Setup Time	t_{RDSS}	0	—	0	—	0	—	ns
RE Disable Hold Time	t_{RDSH}	5	—	5	—	5	—	ns
RE "H" Pulse Width	t_{WREH}	5	—	10	—	10	—	ns
RE "L" Pulse Width	t_{WREL}	5	—	10	—	10	—	ns
RSTR Setup Time	t_{RSTRS}	0	—	0	—	0	—	ns
RSTR Hold Time	t_{RSTRH}	10	—	10	—	10	—	ns
SWCK Cycle Time	t_{SWC}	30	—	40	—	60	—	ns
SRCK Cycle Time	t_{SRC}	30	—	40	—	60	—	ns
Trandition Time (Rise and Fall)	t_T	3	30	3	30	3	30	ns

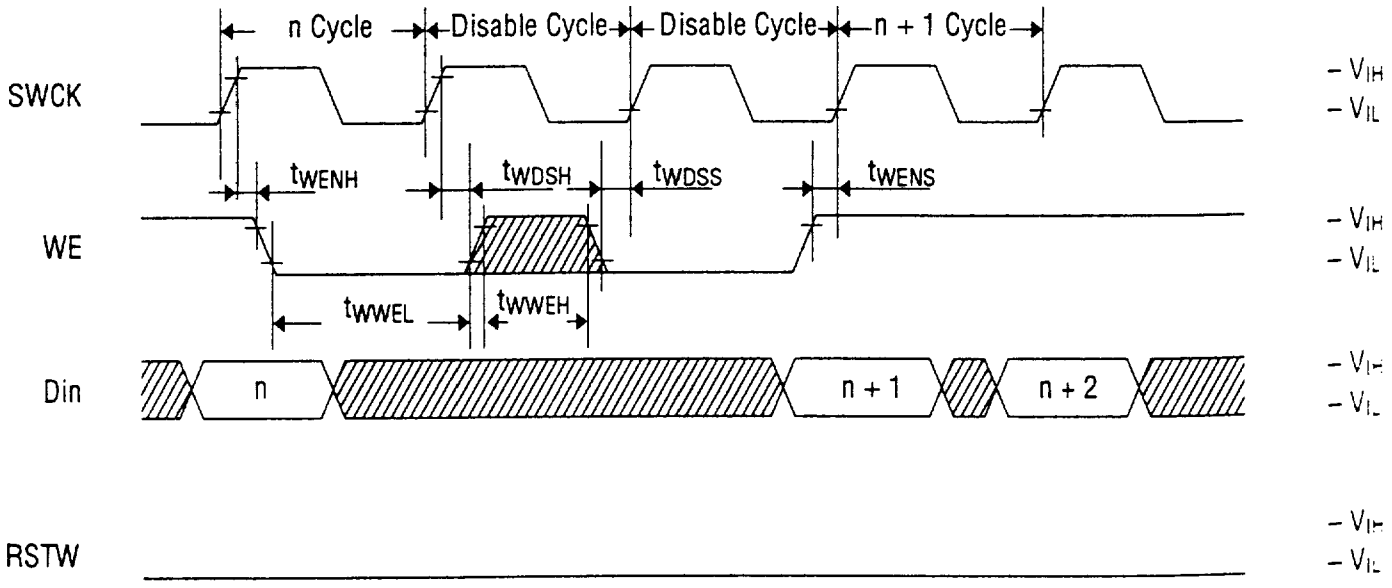
Notes:
1. Input signal reference levels for the parameter measurement are V_{IH} = 3.0V and V_{IL} = 0V. The transition time t_T is defined to be a transition time that signal transfers between V_{IH} = 3.0V and V_{IL} = 0V.
2. AC measurements assume t_T = 3ns.
3. Read address must have more than 600 address delay than write address in every cycle when asynchronous read/write is performed.
4. Read must have more than 600 address delay than write in order to read the data written in a current series of write cycle which has been started last write reset cycle: this is called "new data read".
   When read has less than 119 address delay than write, the read data are the data written in a previous series of write cycle which had been written before last write reset cycle: this is called "old data read".
5. When the read address delay is between more than 120 and less than 599, read data will be undetermined. However, normal write is achieved in this address condition.
6. Outputs are measured with a load equivalent to 2 TTL load and 30pF. Output reference levels are V_{OH} = 2.4V and V_{OL} = 0.8V.

TIMING WAVEFORM

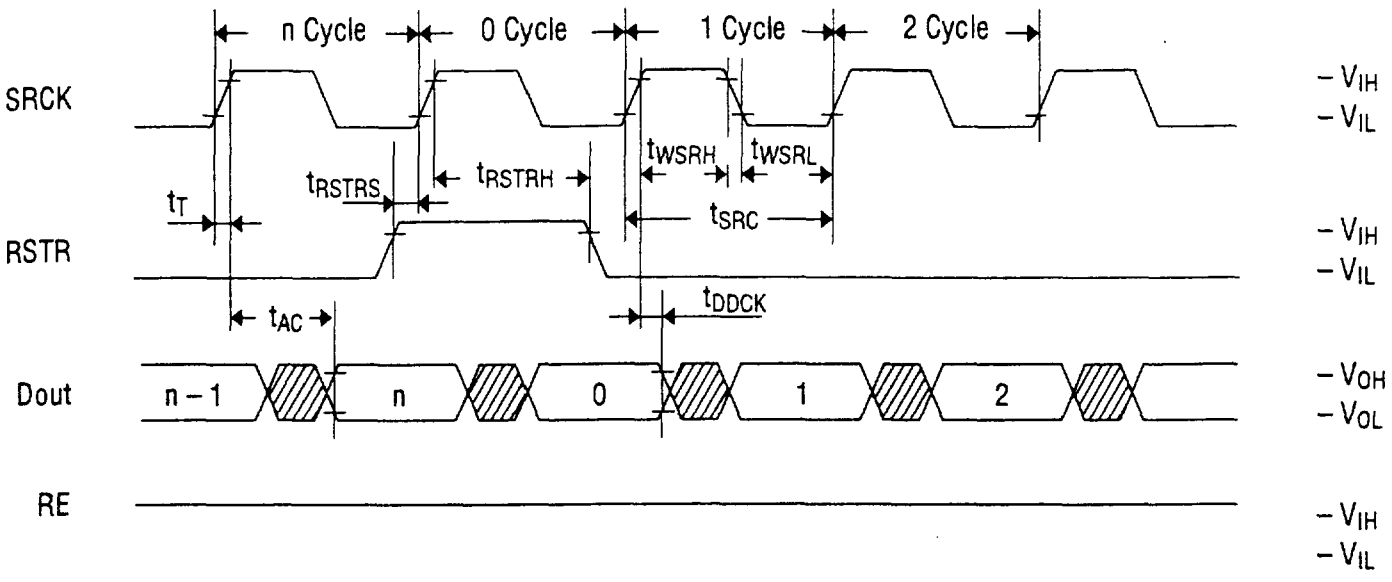
Write Cycle Timing (Write Reset)



Write Cycle Timing (Write Enable)



Read Cycle Timing (Read Reset)



Read Cycle Timing (Read Enable)