Preliminary

OKI semiconductor

MSM5188US

16,384-WORD × 4-BIT HIGH SPEED STATIC CMOS RAM

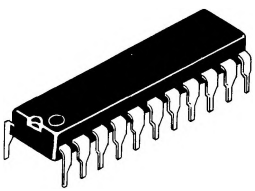
GENERAL DESCRIPTION

The MSM5188 is a static CMOS RAM organized as 16384 words by 4 bits. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary which makes this device very easy to use.

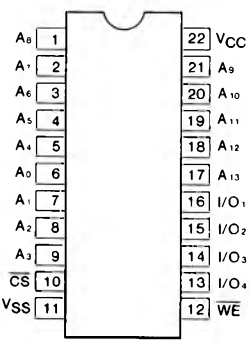
The MSM5188 is offered in a 22-pin slim package.

FEATURES

- Single 5V supply (±10%)
- Completely static operation
- Operating temperature range Ta = 0 to 70°C
- Low power dissipation
  - Standby ..... 11 mW MAX
  - Operation ..... 605 mW MAX
- Access time
  - 45/55/70 ns MAX
- Direct TTL compatible (Input and output)
- 3-State output
- 22 pin DIP PKG (300 mil width)

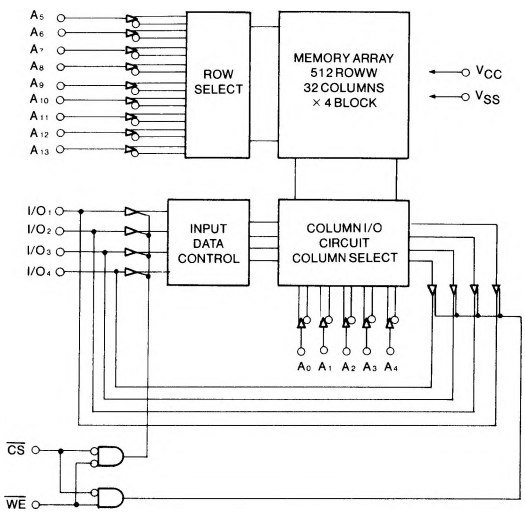


PIN CONFIGURATION



Pin Names	Function
A_0 to A_{13}	Address input
I/O_1 to I/O_4	Data input/output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C Respect to V_{SS}	−0.3 to 7.0	V
Input Voltage	V_{IN}		−0.3 to 7.0	V
Power Dissipation	PD	Ta = 25°C	1.0	W
Operating Temperature	Topr	–	0 to +70	°C
Storage Temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	V_{CC} = 5V ± 10%	2.2	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL}		−0.3	–	0.8	V
Output Load	CL	–	–	–	30	pF
	N	TTL Load	–	–	1	

* When pulse width is equal to or smaller than 20 ns, V_{IH} max = V_{CC} + 1.0V, V_{IL} min = −1.0V.

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	VI = 0 to V_{CC}	−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} VI/O = 0 to V_{CC}	−1		1	μA
"H" Output Voltage	V_{OH}	I_{OH} = −4 mA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC} - 0.2V$ VIN ≦ 0.2V OR VIN ≧ V_{CC} − 0.2V			2	mA
	I_{CCS_1}	$\overline{CS}$ = V_{IH} T_{CYC} = min cycle			18	mA
Operating Supply Current	I_{CCA}	Min cycle			110	mA

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	$V_I = 0V$		6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O} = 0V$		8	pF

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Conditions
Input Pulse Level	$V_{IH} = 3.0V$, $V_{IL} = 0V$
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, 1 TTL GATE

READ CYCLE

($V_{CC} = 5V \pm 10\%$, Ta = 0°C to 70°C)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}		45		55		70	ns
Address Access Time	T_{AC}		45		55		70	ns
Chip Select Access Time	T_{CO}		45		55		70	ns
Chip Selection to Output Active	T_{CX}	5		5		5		ns
Output Hold Time from Address Change	T_{OHA}	5		5		5		ns
Output 3-state from Deselection	T_{OTD}	0	25	0	30	0	30	ns
Chip Selection to Power up Time	T_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	T_{PD}	0	45	0	55	0	70	ns

Notes: 1. Read Condition: During the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. T_{CX} and T_{OTD} are measured ±200 mV from steady state voltage with specified loading in Figure 2.

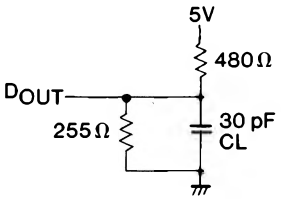


Figure 1 Output Load

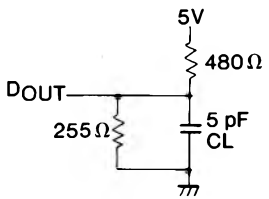


Figure 2 Output Load

Note: CL includes scope and jig.

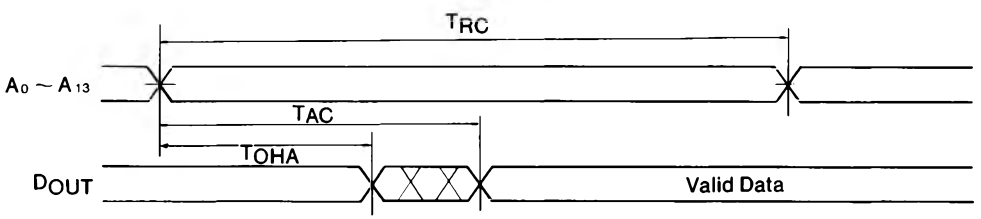
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

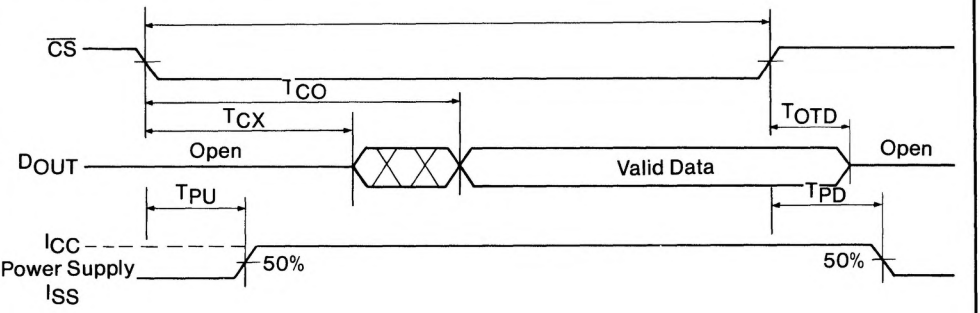
Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	45		55		70		ns
Chip Selection to End of Write	T_{CW}	40		45		55		ns
Address Valid to End of Write	T_{AW}	40		45		55		ns
Address to Write Setup Time	T_{AS}	0		0		0		ns
Write Time	T_W	30		35		40		ns
Write Recovery Time	T_{WR}	5		10		10		ns
Data Setup Time	T_{DS}	25		25		30		ns
Data Hold from Write Time	T_{DH}	0		0		0		ns
Output 3-state from Write	T_{OTW}	0	25	0	25	0	30	ns
Output Active from End of Write	T_{OW}	0		0		0		ns

Notes:
1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. T_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
3. T_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
4. T_{WR}, T_{DS} and T_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
5. T_{OTW} and T_{OW} are measured ±200 mV from steady state voltage with specified loading in Figure 2.
6. When I/O pins are Data output mode, don't force inverse input signals to those pins.

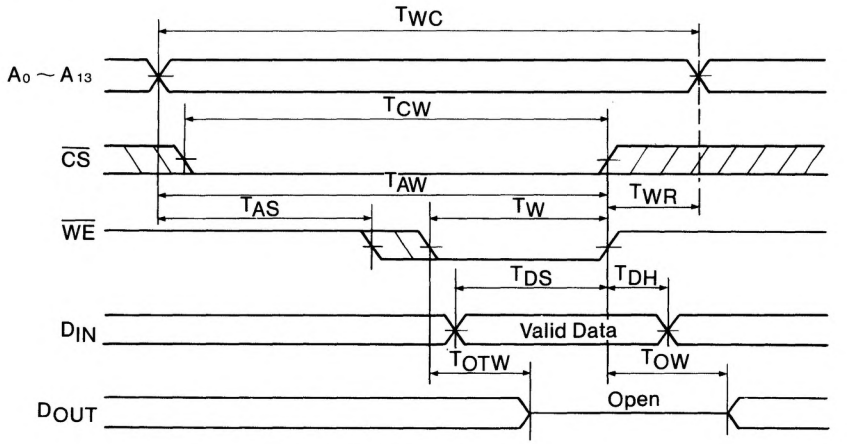
READ CYCLE TIMING 1



READ CYCLE TIMING 2



WRITE CYCLE TIMING 1
($\overline{WE}$ Control)



WRITE CYCLE TIMING 2
($\overline{CS}$ Control)