OKI semiconductor

MSM5205

ADPCM SPEECH SYNTHESIS IC

GENERAL DESCRIPTION

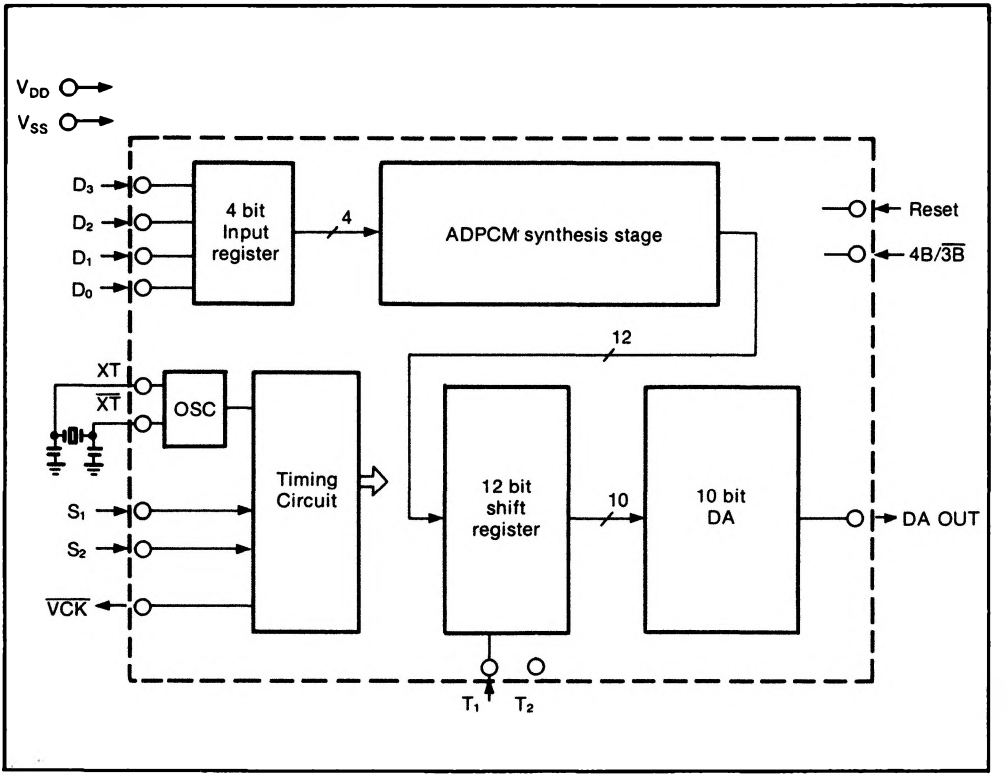
The MSM5205 is a speech synthesis integrated circuit which accepts Adaptive Differential Pulse Code Modulation (ADPCM) data. The circuit consists of synthesis stage which expands the 3- or 4-bit ADPCM data to 12-bit Pulse Code Modulation (PCM) data and a D/A stage which reproduces analog signals from the PCM data.

The MSM5205 is fabricated using Oki's advanced CMOS process which enables low power consumption. The single power supply requirement and its availability in 18-pin molded DIP allow the MSM5205 to be ideally suited for various applications.

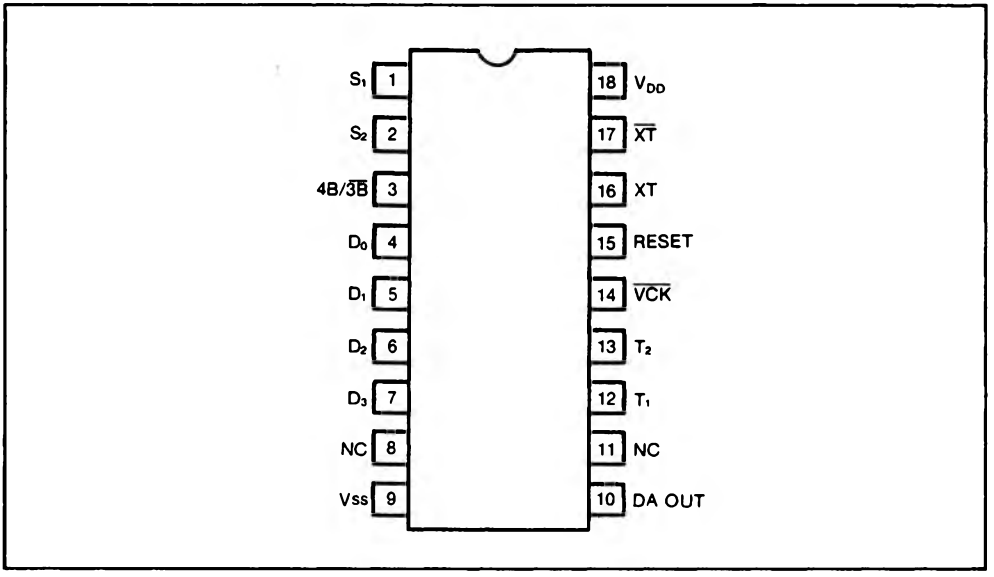
FEATURES

- 3 or 4 bit ADPCM system
- 12 to 32 kb/sec with INT $\overline{VCK}$
- On-chip 10-bit D/A converter
- Low power consumption (10 mW typical)
- Single +5V supply
- Wide operating temperature (Ta = -30°C to +70°C)
- 18-pin molded DIP

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	Ta = 25° C	-0.3 to +7.0	V
Input voltae	V_{IN}	Ta = 25° C	-0.3 to V_{DD}	V
Power dissipation	P_D	Ta = 25° C	200 max	mW
Storage temperature	Tstg	—	-55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device raliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	—	+3 to +6	V
Operating temperature	Top	—	-30 to +70	°C

D.C./A.C. CHARACTERISTICS

(V_{DD} = 5V ± 5%; Ta = -30° C to +70° C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All inputs except T_1, T_2	4.2	—	V_{DD}+.3	V
Input Low Voltage	V_{IL}	All inputs except T_1, T_2	V_{SS}—.3	—	0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	—	—	1	μA
Input Low Current	I_{IL}	V_{IN} = 0V	—	—	-1	μA
Output High Current	I_{OH}	$\overline{VCK}$ pin: Vo = 4.2V	-50	—	—	μA
Output High Current	I_{OL}	$\overline{VCK}$ pin: Vo = 0.4V	+50	—	—	μA
Oscillator Frequency	f_{OSC}	Specified Oscillator	—	384	768	kHz
Operating Current	I_{DD}	f_{OSC} = 384 kHz V_{DD} = 5V	—	2	4	mA
D/A Accuracy (Internal 10-bit D/A)	V_E	Full Scale; V_{DD} = 5V	—	±4	—	LSB
DA_{OUT} Output Impedance	V_{OR}		—	100	—	KΩ

PIN DESCRIPTION

Pin Name	Terminal Number	I/O
S_1	1	I
S_2	2	I

These inputs select the sampling frequency according to Figure 1.

4B/$\overline{3B}$	3	O

Specifies whether 3-bit or 4-bit ADPCM data is to be processed.

D_0	4	I
D_1	5	I
D_2	6	I
D_3	7	I

ADPCM data inputs. For 3-bit ADPCM data, D_0 input is not used and should be connected to ground.

Vss	9	I

Ground (0 V)

DA_{OUT}	10	O

Output for synthesized analog signal. Peak-to-peak swing is proportional to V_{DD}. Typical connection scheme is shown Figure 2.

PIN DESCRIPTION (continued)

T_1	12	I
T_2	13	I

IC test pins used at the factory for testing purposes only. During normal operations, T_1 is grounded and T_2 is left open.

Pin Name	Terminal Number	I/O
$\overline{VCK}$	14	O

This pin outputs a signal whose frequency is equal to the sampling frequency selected by the S_1, S_2 inputs. See note *1.

RESET	15	I

An active high input which initializes the internal circuitry. Internally, the reset pulse is synchronized with the $\overline{VCK}$ signal. To be effective, it must be true for at least twice $\overline{VCK}$ time.

XT	16	I/O
$\overline{XT}$	17	I/O

Oscillator input and output for a 384 kHz crystal or ceramic resonator (Figure 3).

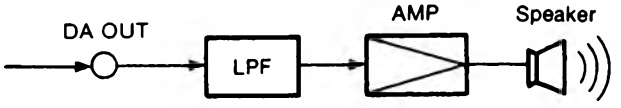
V_{DD}	18	I

Power supply pin (Typical +5 V)

S1	S2	Sampling Frequency
L	L	4 kHz (384 kHz/96)
L	H	6 kHz (384 kHz/64)
H	L	8 kHz (384 kHz/48)
H	H	Prohibited See Note *1

Note: *1 The 384 kHz oscillator must be used whether 4 kHz, 6 kHz, 8 kHz.

Figure 1 Functional table



Cut off frequency fc of LPF should be related to the selected sampling frequency f sample by,

$$fc = f\ sample/2 \times 0.85$$

Sound quality is strongly dependent on the sharpness of the low pass filter.

*If the 5205 is sent a stream of ADPCM data that causes greater than full scale output, the D/A output will wrap around: +5 0.0 +5.

Figure 2

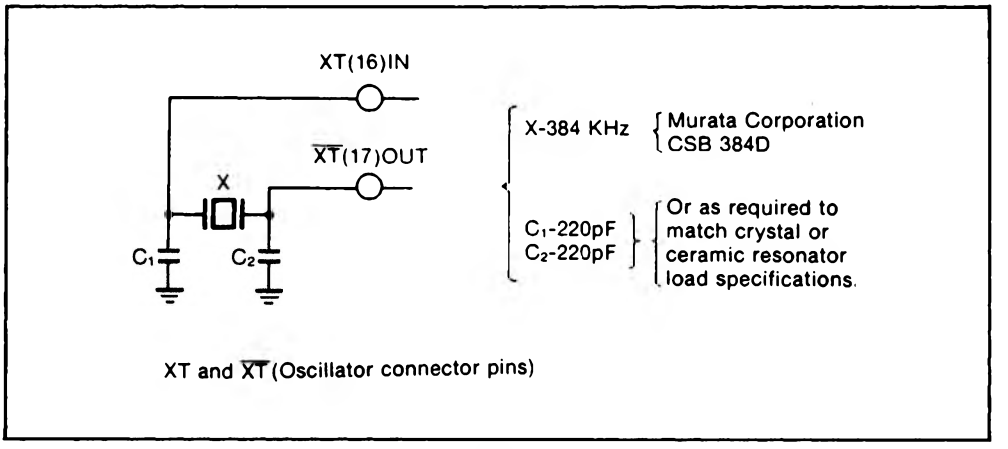


Figure 3

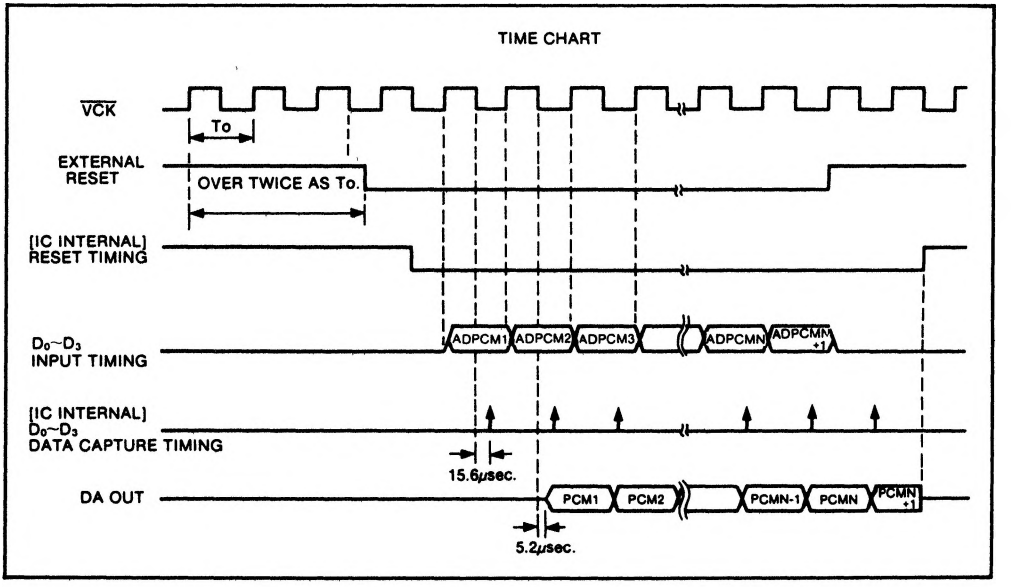


Figure 4

DISTINCTION BETWEEN MSM 5218 AND MSM5205

Both Synthesis stages (MSM5218 and MSM5205) work with the same method. However, with the exception that MSM5218 is equipped with an overflow protection.
In other words, when all 12 PCM bits become '1' any further exceeding analog input would cause a data overflow which is catched and re-routed as the MSB in case of MSM5218.
MSM5205 returns to 'all bits zero' when a data overflow sets in.
Therefore, the DA output of MSM5205 is distorted badly.

When MSM5218 is being used to generate ADPCM data for playback on MSM5205, the peak to peak input level to the A to D converter should be limited to 80% of the converters maximum input range. The use of an automatic gain control (AGC) amplifier or a hard limiter is recommended.

TYPICAL APPLICATION

MSM5205 to Centronics Interface Circuits (f_{SAMPLE} = 8kHz)

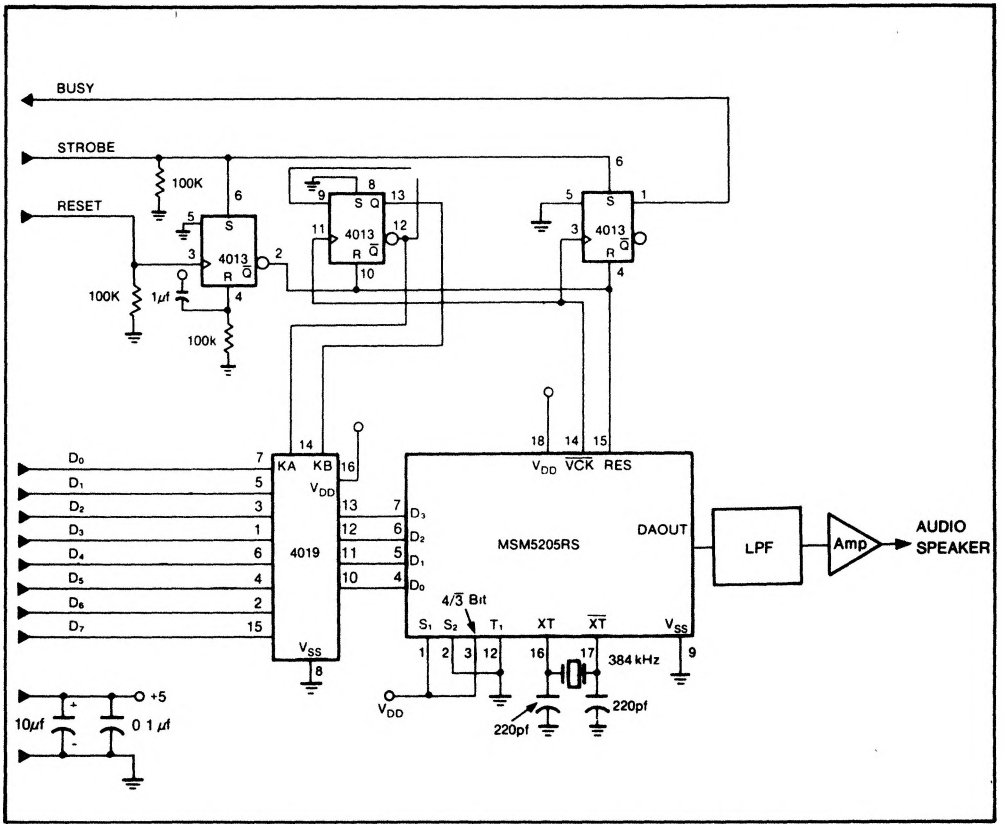


Figure 5

MSM5205 to Centronics Timing Diagram

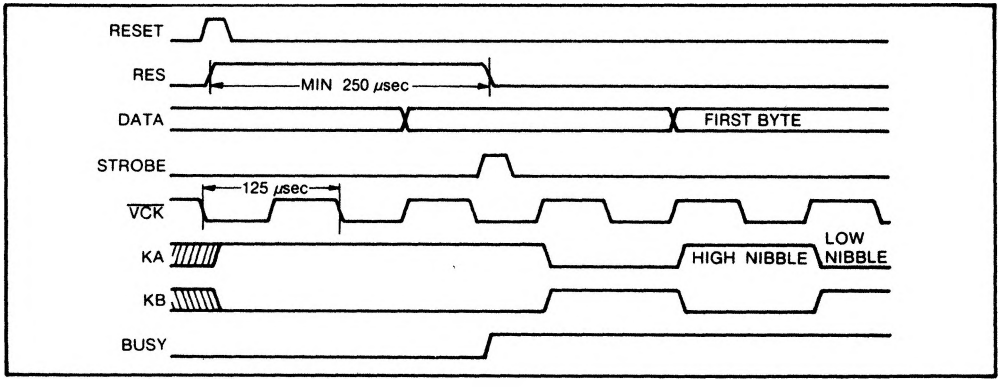


Figure 6