OKI semiconductor

MSM5248

48K BIT ROM ADPCM VOICE SYNTHESIZER

GENERAL DESCRIPTION

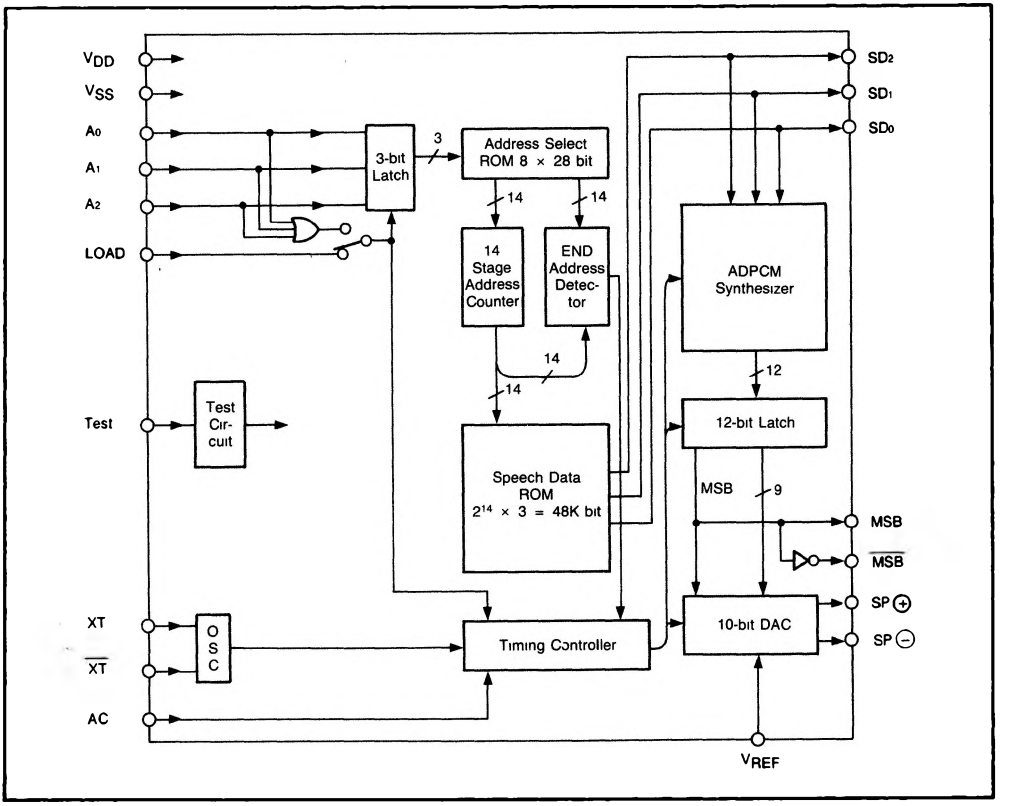
The MSM5248 is an ADPCM voice synthesizer LSI using the CMOS technology process. Its internal circuit consists of the voice synthesis stage, the ROM which stores the speech data, 10-bit D/A converter and the control circuit. It can be used in the variety of systems by connecting with the speaker via the simple interface.

The sampling frequency, etc. can be optionally selected by the user.

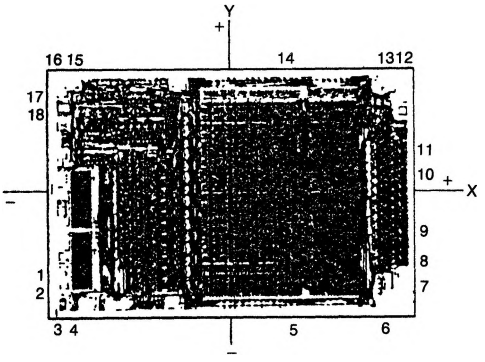
FEATURES

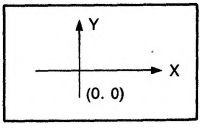
- COMS single chip
- 48K bit ROM for the user's program
- Single power supply: 3 V
- Low power consumption: 0.2 mA (typical)
- Maximum number of words: 7 words
- Maximum length of speech: 3 sec (Sampling frequency: 5.46 kHz)
- Built-in 10-bit D/A converter
- 32.768 kHz crystal oscillation
- Chip form, 18-pin plastic DIP or 24-pin flat package available

BLOCK DIAGRAM



PAD LAYOUT





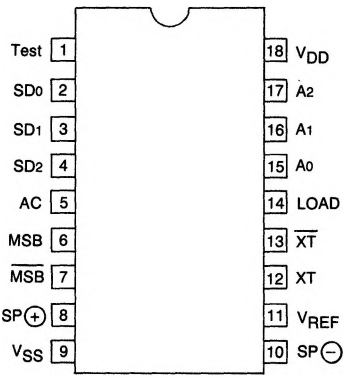
Note: • Chip size: 5.2 mm × 3.48 mm
• Pad size: 110 µm × 110 µm min

PAD LOCATION

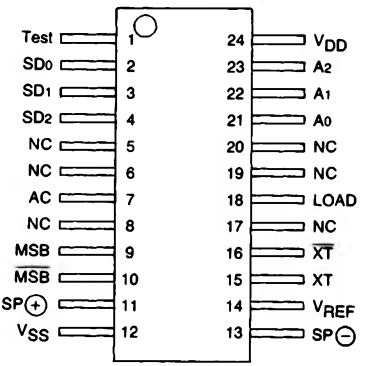
Pad No.	Symbol	Position	
		X	Y
1	TEST	−2445	−1197
2	SD_0	−2445	−1377
3	SD_1	−2445	−1585
4	SD_2	−2265	−1585
5	AC	893	−1585
6	MSB	2143	−1585
7	$\overline{MSB}$	2445	−1289
8	SP ⊕	2445	−987
9	V_{SS}	2445	−511
10	SP ⊖	2445	221
11	V_{REF}	2445	567
12	XT	2445	1585
13	$\overline{XT}$	2265	1585
14	LOAD	789	1585
15	A_0	−2265	1585
16	A_1	−2445	1585
17	A_2	−2445	1317
18	V_{DD}	−2445	1137

PIN CONFIGURATION

(Top View) 18 Lead Plastic DIP



(Top View) 24 Lead Plastic Flat Package



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings **Table 1** (V_{SS} = 0 V)

Parameter	Symbol	Conditions	Limit	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +3.6	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Power Dissipation	P_D		200 max	mW
Storage Temperature	Tstg	—	−55 to +150	°C

Operating Range **Table 2**

Parameter	Symbol	Conditions	Limit	Unit
Supply Voltage	V_{DD}	—	+2.4 to +3.6	V
Operating Temperature	Top	—	−10 to +60	°C
External Reference Resistor	R_{REF}	Applicable for V_{REF}	Min 100	kΩ

DC Characteristics **Table 3** (V_{DD} = 3.1 V, V_{SS} = 0 V, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	2.5	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Voltage *1	I_{IH}	V_{IH} = 3.1 V	—	—	1	µA
"L" Input Voltage	I_{IL}	V_{IL} = 0 V	—	—	−1	µA
"H" Input Voltage *2	I_{IH_1}	V_{IH_1} = 3.1 V	7	—	200	µA
"H" Output Voltage *3	I_{OH}	V_{OH} = 2.5 V	−0.1	—	—	mA
"L" Output Voltage *3	I_{OL}	V_{OL} = 0.5 V	0.1	—	—	mA
Power Consumption (1)	I_{DD_1}	Active	—	0.2	1.0	mA
Power Consumption (2)	I_{DD_2}	Standby (no oscillation)	—	—	1	µA
Power Consumption (3)	I_{DD_3}	Standby (oscillation)	—	10	20	µA
DA Synk Current *4	I_{SYNK}	Note 1	260	400	600	µA
DA Accuracy *4	I_E	Note 2	0.75 × 1	1	1.25 × 1	µA

Notes: *1 Applicable for A_0, A_1, A_2, when pull down resistor is not provided.
*2 Applicable for LOAD, AC and A_0, A_1 and A_2 when pull down resistor is applied.
*3 Applicable for MSB, MSB.
*4 Applicable for SP ⊕, SP ⊖.

Table 4
(Value of resistor V_{REF} is 2 MΩ)

MSB									LSB	Pin
0	1	1	1	1	1	1	1	1	1	SP ⊕
1	0	0	0	0	0	0	0	0	0	SP ⊖

Note 1: Lower 2 bit in output of 12 bit latch is disregarded, and data with 10 bit is input to D/A converter.
The characteristics indicates the value of the pin SP ⊕ and SP ⊖ when the value as shown below is input to D/A converter.

Table 5

Actual Measurement Value	Input Data to 10-bit D/A Converter										
I_1 =	MSB									LSB	Pin
	0	0	0	0	0	0	1	0	0	0	SP ⊕
I_0 =	MSB									LSB	Pin
	0	0	0	0	0	0	0	1	0	0	SP ⊖

Note 2: $0.75 \times 2I_0 < I_1 < 1.25 \times 2I_0$
This Formula is applied on following condition.

AC Characteristics
(V_{DD} = +2.4 to +3.6 V, Ta = −10 to +60°C)

Table 6
(Timing Chart)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator Frequency	f_{OSC}	—	32	32.768	35	kHz
AC Input Pulse Width	t_{ACW}	—	10	—	—	μs
Load Input Pulse Width	t_{LW}	—	65	—	—	μs
D/A Output Delay Time	t_{LO}	$f_{(OSC)}$ = 32.768 kHz	—	—	305	μs
Full-address Zero Interval	t_{OW}		2	—	—	μs

PIN DESCRIPTION

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
A_0	15	15	21	I
A_1	16	16	22	
A_2	17	17	23	I

Address selection input
Maximum 7 words or 3 words are determined according to A_0, A_1, and A_2 H/L combinations ~, except that $A_0 = A_1 = A_2$ = "L" is prohibited for users because of the test code for LSI.

LSI operation starting method is selected by masking option, too.
① One method is to apply appointed pulse to either A_0, A_1 or A_2.
② The other method is to apply load pulse to LOAD pin after determining A_0, A_1 or A_2.

When the voice starting method ① is selected, repeated operation or one time operation is selected by masking option. (See timing chart)

Existence of pull-down resistor of A_0, A_1 and A_2 is selected by masking option.

Starting method of IC with A_0 to A_2 pins.

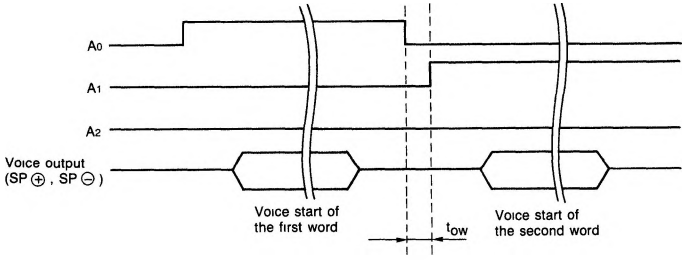


Figure 1

IC is activated by setting only one of A_1 to A_2 pins in "H" level. When switching to the voice start of another word, be sure to set full-address "L" interval (tow). The maximum number of words in three in case this starting method is selected.

LOAD	14	14	18	I

Pulse input pin for LSI starting
LOAD pin is a pulse input pin for voice start. Load pin is pulled down inside.

- When the voice is started by either A_0, A_1 or A_2, LOAD pin should be used as open.
- Either repeated operation or one time operation is selected by masking option. (See timing chart)

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
XT	12	12	15	I
$\overline{XT}$	13	13	16	I

Pins for crystal
Either external clock input or crystal oscillation can be selected by masking option.

- External clock input

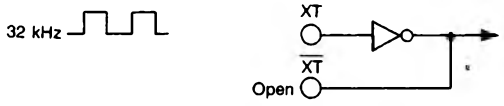


Figure 2

- Crystal oscillation

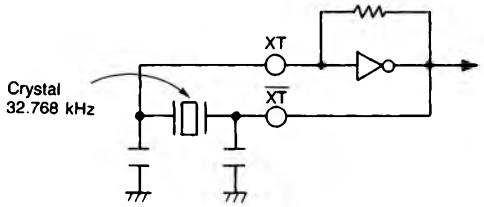


Figure 3

AC	5	5	7	I

All clear input pin
All functions of LSI are stopped by input of "H" level voltage to AC pin, and status of LSI turns to stand-by. AC pin is pulled down inside.
The built-in P.O.R. (Power on reset) function is designated by masking option.

V_{REF}	11	11	14	I

This pin is an input pin for the constant-current control of low impedance D/A converter.
The volume of speaker can be controlled by external resistor (variable) whose value is more than 100 kΩ.

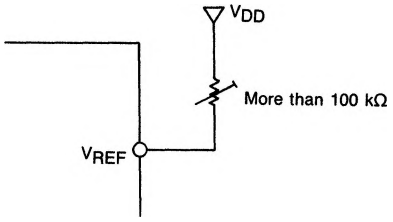


Figure 4

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number			I/O
	CHIP	18 DIP	24 FLT	
SP ⊕	8	8	11	O
SP ⊖	10	10	13	

These are output pins for 10-bit D/A converter (low impedance type). When LSI is at standby, SP ⊕ and SP ⊖ turn to high impedance.

MSB	6	6	9	O
$\overline{MSB}$	7	7	10	O

These are output pins for the most significatiant bit signal and the inverted signal.

TEST	1	1	1	I
SD_0	2	2	2	O
SD_1	3	3	3	O
SD_2	4	4	4	O

As test pin is pulled down, this pin should open.
SD_0, SD_1, SD_2 are 3-bit ADPCM data output pins, these pins should be open.

V_{SS}	9	9	12	I

This is a ground input pin.

V_{DD}	18	18	24	I

This is a supply voltage input pin.

TIMING CHART

REPEATED OPERATION

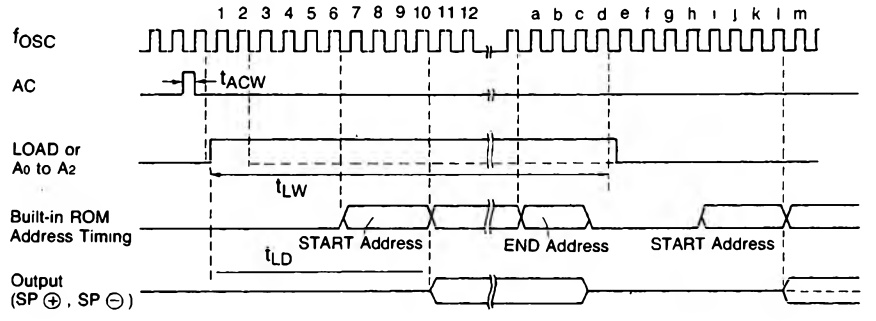


Figure 5

ONE TIME OPERATION

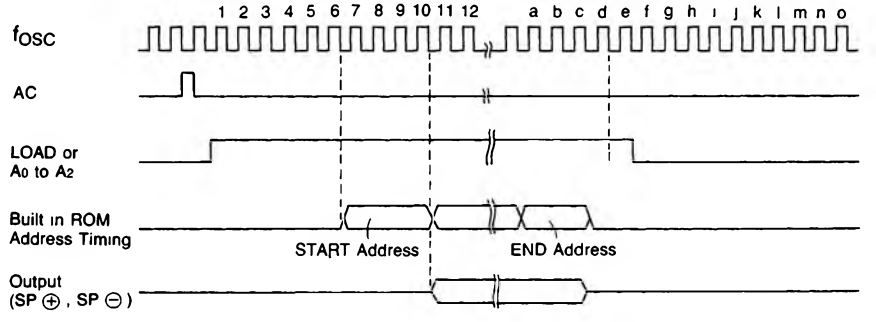


Figure 6

TYPICAL APPLICATION CIRCUIT

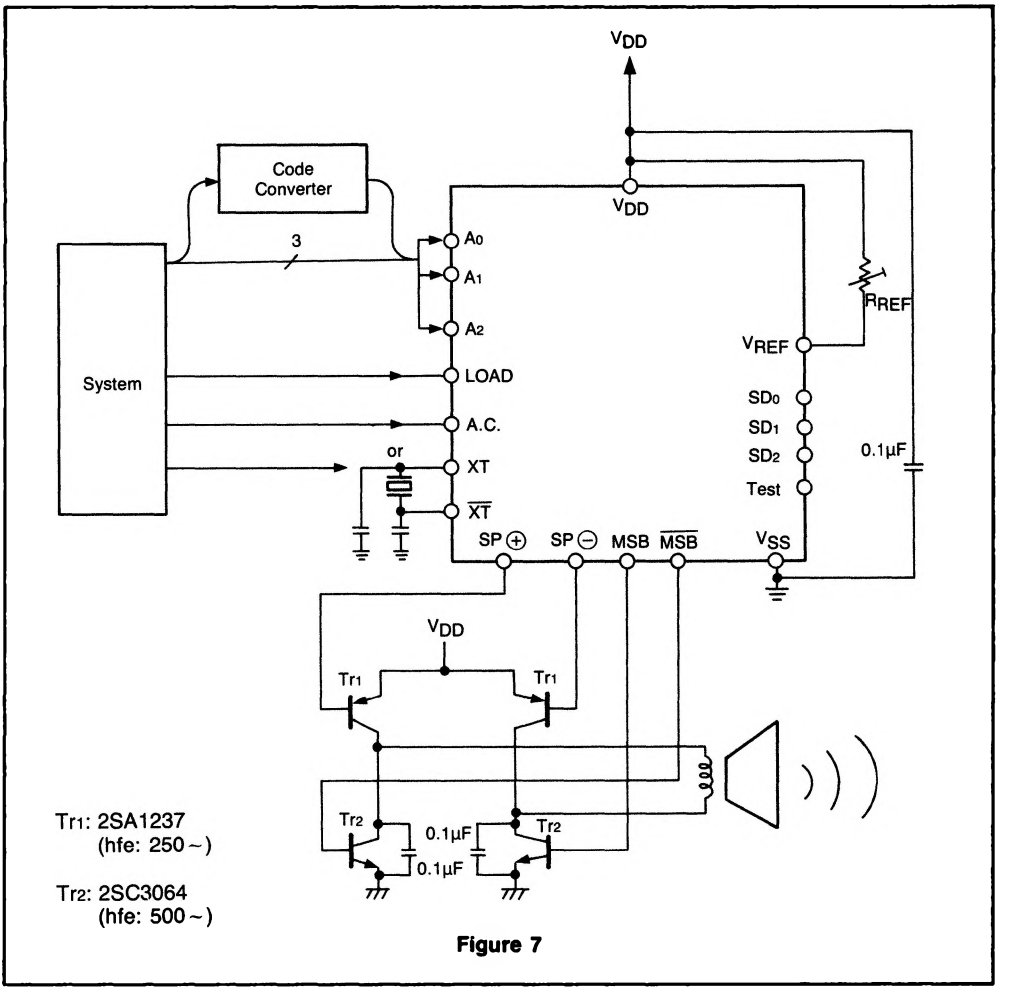


Figure 7

Combination in MSM5248 and MSM5041 (Melody chip)
This circuit is applied to Voice & Melody card and Toy, etc.

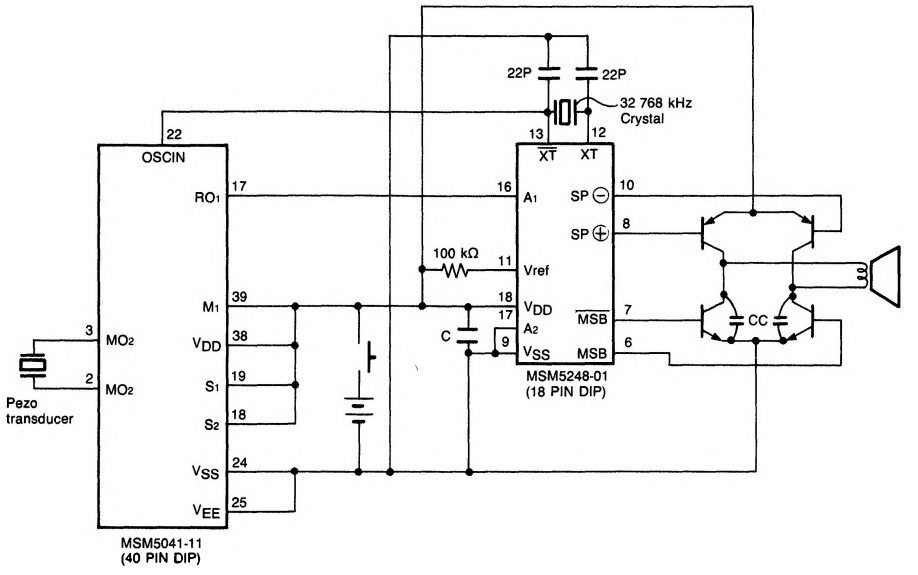


Figure 8

OPTION LIST

Table 7

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz	5.46 kHz	
OP-1	Pull-down for A_0	Yes	No	
OP-2	Pull-down for A_1	Yes	No	
OP-3	Pull-down for A_2	Yes	No	
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes	No	
OP-9	Oscillation	X'tal	External clock	
OP-10, 11	Starting method of LSI	A_0—A_2	LOAD	
OP-12	One time or repeatable	One time	Repeatable	
OP-14	Power on reset	Yes	No	

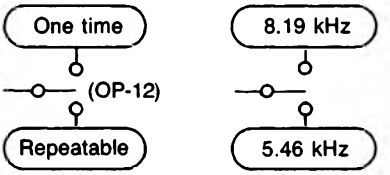


Figure 9

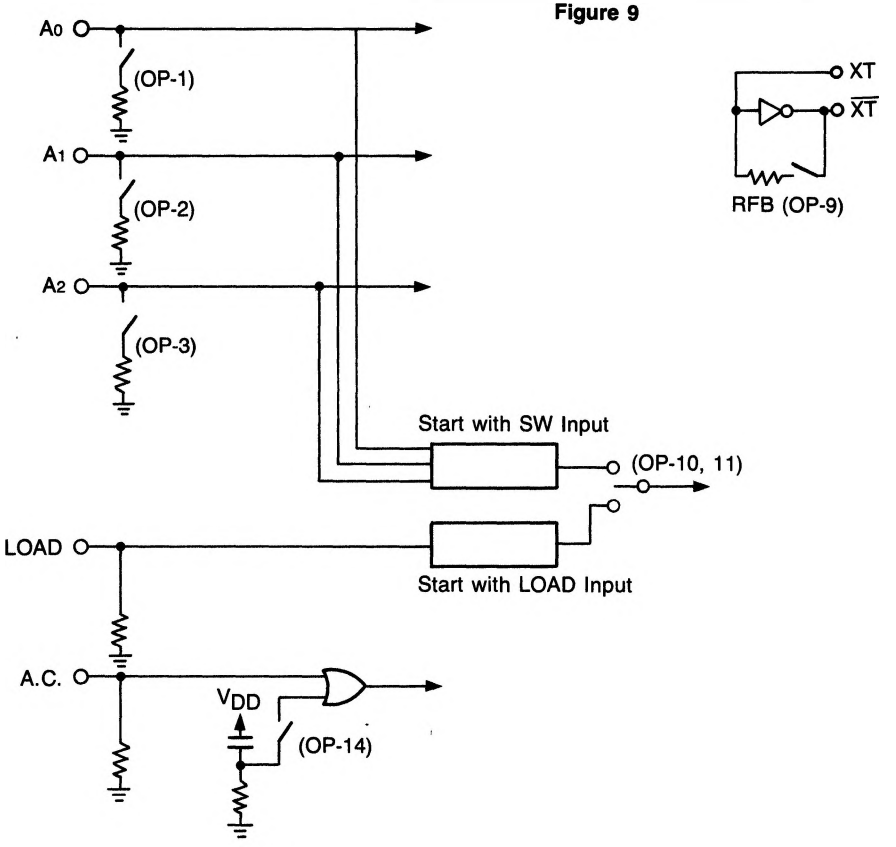


Figure 10

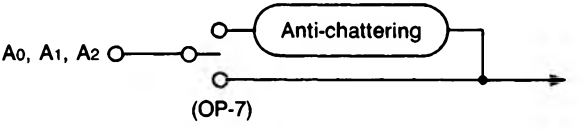


Figure 11

STANDARD VERSION LIST

Type No.	Contents	Selection		
		A_0	A_1	A_2
MSM5248-01	"Happy Birthday"	L	H	L
MSM5248-04	Fanfare Sound	H	L	L
MSM5248-05	"Merry Christmas & a Happy New Year"	H	L	L
	"Merry Christmas"	L	H	L

OPTION LIST OF STANDARD VERSION

MSM5248-01

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	Yes		
OP-2	Pull-down for A_1	No		
OP-3	Pull-down for A_2	No		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	A_0—A_2		
OP-12	One time or repeatable	One time		
OP-14	Power on reset	Yes		

MSM5248-04

No.	Items	Selection		
1	Package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	No		
OP-2	Pull-down for A_1	Yes		
OP-3	Pull-down for A_2	Yes		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	LOAD		
OP-12	One time or repeatable	Repeatable		
OP-14	Power on reset	Yes		

MSM5248-05

No.	Items	Selection		
1	package	Chip	18p DIP	24p FLAT
2	Sampling frequency	8.19 kHz		
OP-1	Pull-down for A_0	No		
OP-2	Pull-down for A_1	No		
OP-3	Pull-down for A_2	Yes		
OP-7	Anti-chattering when A_0—A_2 of starting method is selected.	Yes		
OP-9	Oscillation	X'tal		
OP-10, 11	Starting method of LSI	A_0—A_2		
OP-12	One time or repeatable	One time		
OP-14	Power on reset	Yes		