OKI semiconductor

MSM58422

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER WITH FLT DRIVER

GENERAL DESCRIPTION

OKI's MSM58422 is a low-power, high-performance 4-bit single-chip microcontroller implemented in complementary metal oxide semiconductor technology.

Integrated within the one chip is a mask ROM of 1536 × 8 bits, RAM of 40 × 4 bits, 10 input/output ports 11-bit timer-counter, clock oscillator, 4-bit parallel arithmetic circuit, 40 static FLT drivers etc.

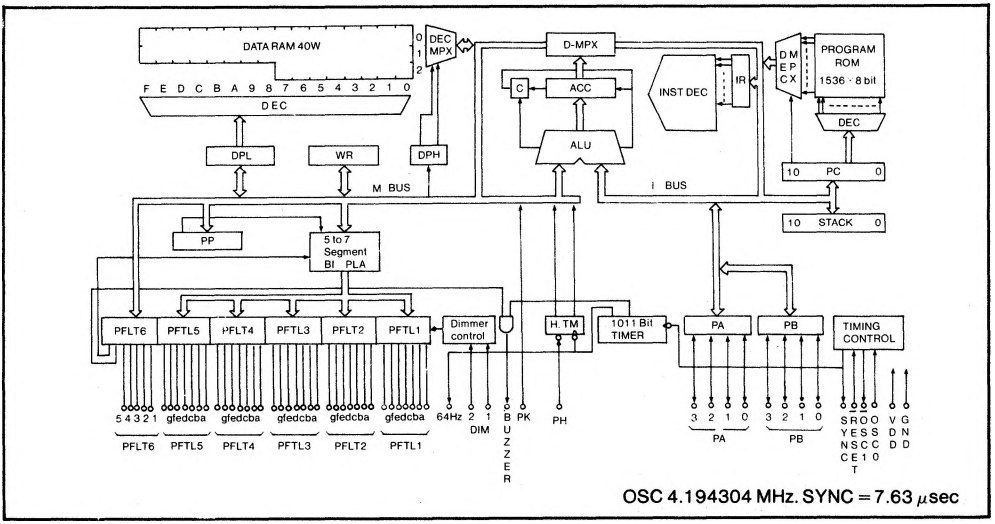
MSM58422 has an instruction set which consists of 4-bit arithmetic instructions, Boolean (bit) manipulation instructions (bit-set, bit-reset, bit-test), data input/output instructions, and 8-bit code translation (Table data out) instructions.

Also the pseudo-bilateral ports are used for connection to the buses of other 8-bit systems.

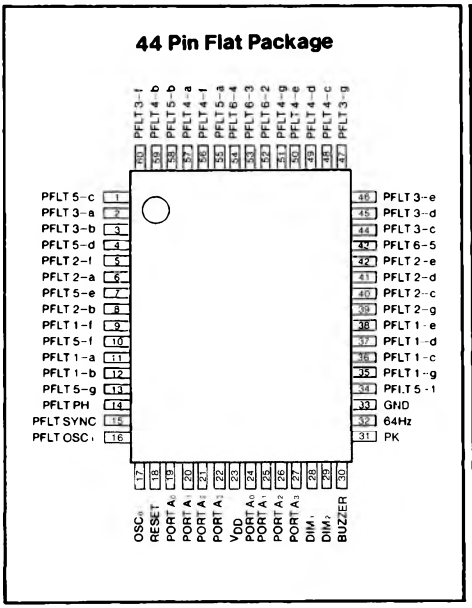
FEATURES

- Low Power Consumption CMOS 4-bit One-Chip Microcomputer
- 100% Static Logic
- 1536 × 8 bits MASK ROM
- 8-bit Interface Bus
- 1 Stack Register
- 52 Instructions
- +5V Single Power Supply
- 60-Pin Flat Package
- Built-in 11-bit Timer
- 94% of the 52 Instructions and 1 Byte and 1 Machine Cycle
- Integrated with 10 Input/Output Ports and 40 Static FLT Driver Circuit
- PK and PH Input contain Schmidt Trigger Circuits

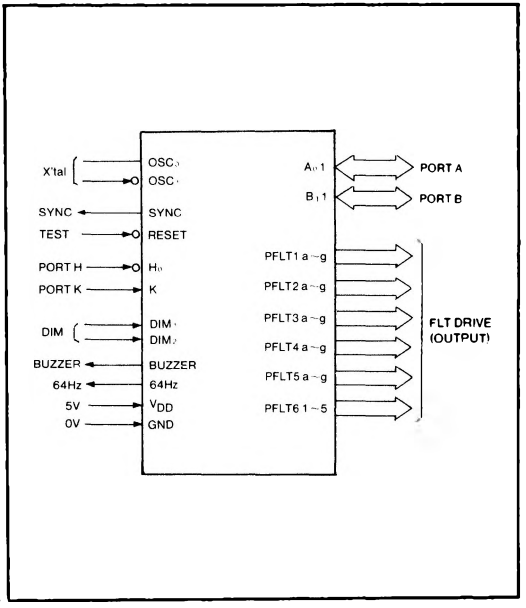
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 ~ V_{DD}	V
Output Voltage (FLT)	V_O	Ta = 25°C	V_{DD} ~ 30	V
Power Dissipation	P_D	Ta = 25°C per 1 package	200	mW
		Ta = 25°C per 1 FLT	8	
Storage Temperature	T_{stg}	–	−55 ~ +125	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage	V_{DD}	f(OSC) = 0 to 4.2 MHz	4 ~ 6	V
Operating Temperature	T_{OP}	–	−40 ~ +85	°C
Output Voltage (FLT)	V_O	–	V_{DD} ~ 26	V
Fan Out (excluding FLTs)	N	MOS Load	15	–
		TTL Load	1	

DC CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}		3.6			V
"L" Input Voltage	V_{IL}				0.8	V
"H" Output Voltage (1)	V_{OH}	I_O = −15 μA	4.2			V
"H" Output Voltage (2)	V_{OH}	I_O = −40 μA	4.2			V
"L" Output Voltage (3)	V_{OL}	I_O = 1.6 mA			0.4	V
OSC_o Input Leak Current	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$			10/−10	μA
Input Current (4)	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$			1/−20	μA
"H" Output Current (1)	I_{OH}	V_O = 0.4 V			−1	mA
"H" Output Current (5)	I_{OH}	V_O = 2.5 V	−0.25			mA
"H" Output Current (6)	I_{OH}	V_O = 3 V	−1			mA
"L" Output Current (3)	I_{OL}	V_O = 0.4 V	1.6			mA
FLT Output Leak Current	I_{LO}	$V_O = V_{DD}$ − 26 V			−10	μA
Input Capacity	C_I	f = 1 MHz, Ta = 25°C		5		pF
Output Capacity	C_O	f = 1 MHz, Ta = 25°C		7		pF
Current Consumption	I_{DD}	f = 4.2 MHz at no load		2	5	mA

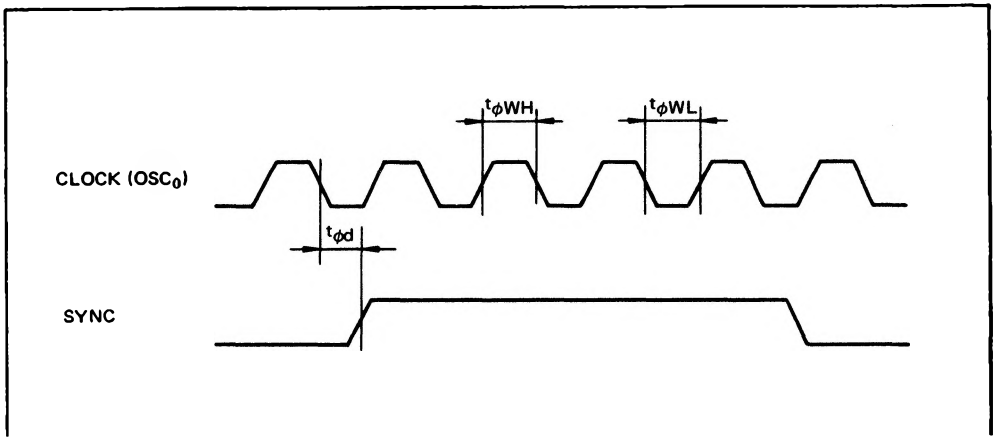
Notes: (1) Applied to PA, PB
(2) Applied to SYNC, BUZZER, 64 Hz and PFTL
(3) Applied to PA, PB, SYNC, BUZZER and 64Hz
(4) Applied to PH, RESET, DIM and PK
(5) Applied to SYNC and 64Hz
(6) Applied to BUZZER and PFLT

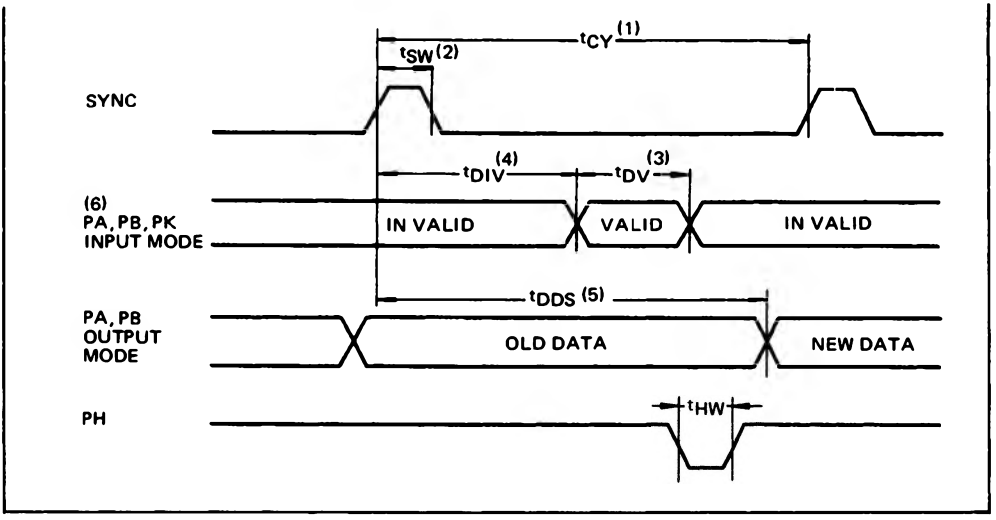
SWITCHING CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

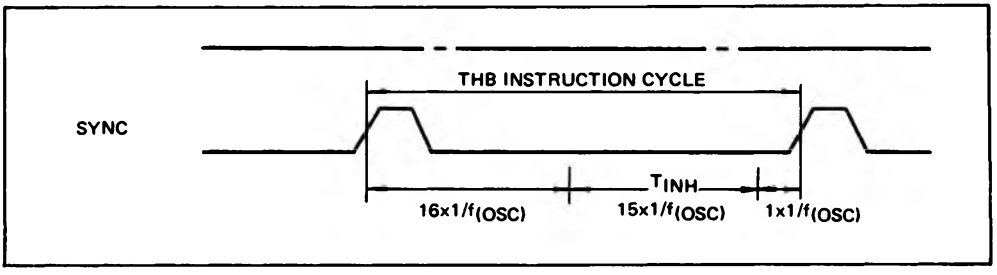
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SYNC Delay Time from Clock (OSC_0)	$t_{\phi d}$	C_L = 50pF			800	ns
Clock (OSC_0) Pulse Width	$t_{\phi WH}$ $t_{\phi WL}$		115			ns
Cycle Time	T_{CY}		(1)			μs
SINC Pulse Width	t_{SW}		(2)			μs
PA PB Data Valid Time PK	t_{DV}	C_L = 50pF	(3)			μs
PA PB Data Invalid Time PK	t_{DV}	C_L = 50pF			(4)	μs
Data Delay Time	t_{DDS}	C_L = 50pF			(5)	ns
Port H Set Pulse Width (8)	t_{HW}		500			ns
64Hz Delay Time from SYNC	t_{SFD}	C_L = 50pF			2	μs
BUZZER Delay Time from SYNC	t_{SBD}	C_L = 50pF			2	μs
SEGMENT Delay Time from SYNC	t_{SSD}	C_L = 50pF (8)			2	μs

Notes: (1) $t_{CY} = 32 \times 1/f_{(OSC)}$
(2) $t_{SW} = 4 \times 1/f_{(OSC)}$
(3) $t_{DV} = 8 \times 1/f_{(OSC)}$
(4) $t_{DIV} = 16 \times 1/f_{(OSC)} + 0.5\ \mu s$
(5) $t_{DDS} = 26 \times 1/f_{(OSC)} + 1\ \mu s$

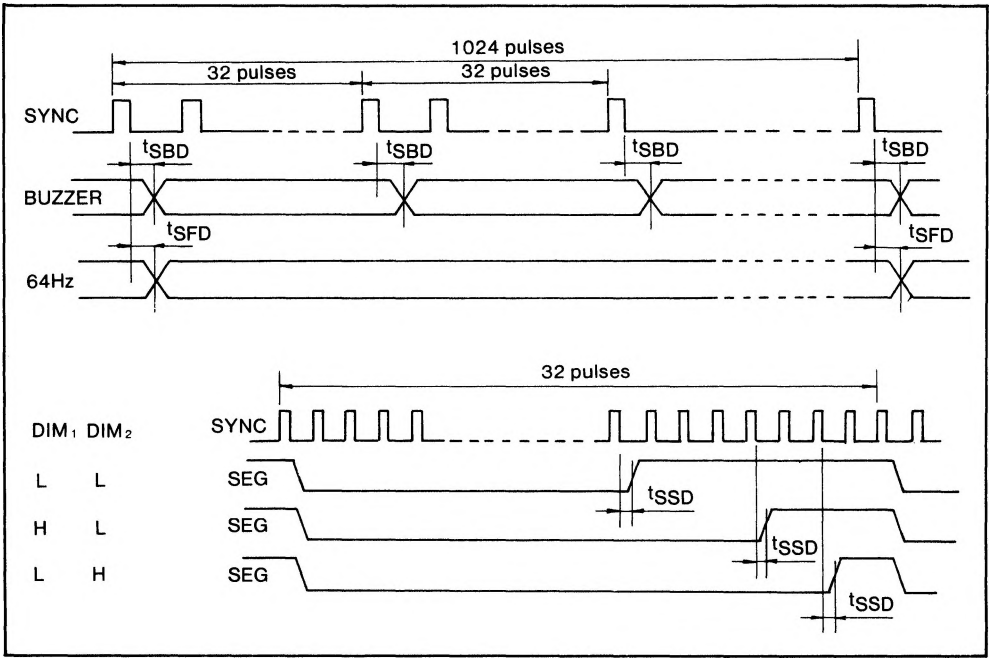




Notes: (6) When data input from PA or PB, set the contents of PA or PB to "1" prior to reading instruction.
(7) Alteration by the instructions relative to output ports PFLT (It is in the case that the outputs of open drain are pulled down to GND by a resistor below 20 kΩ).



Notes: (8) At execution of the THB instruction, any input made during a period of T_{INH} (15 × $1/f_{(OSC)}$ shown in the above figure may be neglected.



Notes: (9) The waveform shown above is in lighting up state, in the case that that open-drain output of FLT driver is pulled down to GND by a resistor below 20 kΩ.
DIM_1 and DIM_2 inputs must be in the state specified above.

DESCRIPTION OF TERMINALS

GND (Pin 33)
Circuit grounding potential

V_{DD} (Pin 23)
Main power supply

OSC_O (Pin 17)
Input of the internal oscillation circuit at one side of the crystal resonator and ceramic vibrator.

OSC_I (Pin 16)
Output of the internal oscillation circuit at the other side of the crystal resonator and ceramic vibrator (not TTL compatible)

PA, PB (Pins 19 ~ 22 and 24 ~ 27)
These are quasi-bidirectional ports for a 4-bit parallel I/O. To input data from these ports, it is necessary to write a "1" to them beforehand. When nothing is applied to their terminals, the content of the output ports is written into them, so they can also be used as registers. In addition, it is possible to use them to make an 8-bit parallel output depending on instructions.

PK (Pin 31)
1-bit input port with no latching function. Contains Schmidt a Schmidt Trigger Circuit.

PH (Pin 14)
Input port with latching function to be set by negative logical signal.

This terminal is set at the time the negative logical signal is applied to it from the outside. It is reset automatically after execution of the test instruction at this port.

RESET (Pin 18)
Reset must be active for greater than 1 machine cycle.

The RESET signal input has priority over all of other signals and performs the following functions:

(1) Resets all bits of the program counter;
(2) Resets the latches of I/O ports PA, PB and output port PFLT6;
(3) Resets the timer flag (TMF);
(4) Resets the accumulator;
(5) Resets the skip F/F circuit;
(6) Resets the machine cycle to MI;
(7) Resets the output port PFLT5–1 to the data of 7 Seg PLA address 0;

Since the RESET terminal is pulled up to V_{DD} by an internal resistor (approx. 800 kΩ), it is possible to activate power ON/reset by connecting it to an external capacitor.

SYNC (Pin 15)
This is a general-purpose synchronizing signal output. The signal is output at the beginning of each machine cycle. Output constantly, this signal is used also as a clock pulse to external units.

One SYNC cycle is 32 times that of the original oscillation (8 μs when the clock pulse is 4 MHz).

PFLT 1 ~ 6 (Pins 1 ~ 13 and 34 ~ 60)
These are 7-bit and 5-bit parallel output ports, respectively. They are used to directly drive an FLT (static type). Specification of each port is accomplished by the port pointer (PP), which is a 4-bit register and is set to the contents of the accumulator by the LPA instruction.

Latching data of each port is output through the logical AND operation with the DIMA signal (later described) and via buffer circuits. (When the data in the latch is 1, DIMA is output. When it is 0, the output is at high impedance.)

Content of PP				Port Specified
b_3	b_2	b_1	b_0	
×	0	0	0	PFLT1
×	0	0	1	PFLT2
×	0	1	0	PFLT3
×	0	1	1	PFLT4
×	1	0	0	PFLT5
×	1	0	1	PFLT6-1 ~ 4
×	1	1	0	PFLT6-5, BI and BZ
×	1	1	1	–

×: Don't care
BI: 7 Segment Decoder PLA Blank Input
BZ: Control Signal output for the buzzer output

The inputs with the latching function of ports PFLT1 ~ 5 are connected to the outputs of the 7 segment decoder PLA and that of PFLT6 directly to the internal buses.

DIM1, DIM2 (Pins 28, 29)
Input terminals for the dimmer control of output ports PFLT1-6.

DIM1	DIM2	DIMA
0	0	1/4 duty
1	0	1/8 duty
0	1	1/16 duty
1	1	1

BUZZER (Pin 30)
This terminal outputs the value of the logical AND operation between latching bit 2 of output port PFLT6 and the timer output (Q5).

By externally connecting a resistor and a transistor, this BUZZER output terminal is used to control an alarm, buzzer etc.

64 Hz (Pin 32)
This is an output terminal, whose frequency is 1/65536 of the OSC0. For example, when the frequency of oscillator is 4.194304 MHz, the frequency of the 64 Hz signal output is given 64 Hz.

This output pulse is used for adjusting the frequency. Its duty is 50%.

INSTRUCTIONS LIST

Mnemonic	Description	Instruction Code								Byte	Cycle
		7	6	5	4	3	2	1	0		
CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
CLL	Clear DP_L	0	0	1	0	0	0	0	0	1	1
CLH	Clear DP_H	0	1	1	0	0	0	0	0	1	1
LAI	Load Accumulator with Immediate	0	0	0	1	I_3	I_2	I_1	I_0	1	1
LLI	Load DP_L with Immediate	0	0	1	0	I_3	I_2	I_1	I_0	1	1
LHI	Load DP_H with Immediate	0	1	1	0	0	I_0	I_1	I_0	1	1
L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
LAL	Load Accumulator with DP_L	0	1	0	1	0	1	0	1	1	1
LLA	Load DP_L with Accumulator	0	1	0	1	0	1	0	0	1	1
LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
SI	Store Accumulator to Memory then Increment DP_L	1	0	0	1	0	0	0	0	1	1
LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
LTI	Load Timer with Immediate "0" (Clear Timer & TMF)	0	1	1	0	1	0	0	0	1	1
X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
INA	Increment Accumulator	0	0	0	0	0	0	0	1	1	1
INL	Increment DP_L	0	1	0	1	0	1	1	1	1	1
INM	Increment Memory	0	1	0	1	1	1	0	1	1	1
INW	Increment W Register	1	0	0	0	1	0	0	0	1	1
DCA	Decrement Accumulator	0	0	0	0	1	1	1	1	1	1
DCL	Decrement DP_L	0	1	0	1	0	1	1	0	1	1
DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	I_3	I_2	I_1	I_0	1	1
DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
CM	Compare Accumulator with Memory	0	1	0	1	1	1	1	0	1	1
SMB	Set Memory Bit	1	0	1	1	1	0	I_1	I_0	1	1
RMB	Reset Memory Bit	1	0	1	1	1	1	I_1	I_0	1	1
TAB	Test Accoumulator Bit	1	0	1	0	0	0	I_1	I_0	1	1
TMB	Test Memory Bit	1	0	1	0	0	1	I_1	I_0	1	1
THB	Test H Port Bit	1	0	1	0	1	1	0	0	1	1
TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1
J	Jump	0	0	1	1	0	I_{10}	I_9	I_8	2	2
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
JC	Jump in Current Page	1	1	I_5	I_4	I_3	I_2	I_1	I_0	1	1
JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
CAL	Call Subroutine	0	0	1	1	1	I_{10}	I_9	I_8	2	2
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	1
OTD	Output Table Data	0	1	1	1	0	0	0	1	1~15	2
OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
OP	Output Accumulator to Port designated Port Pointer	0	1	1	1	0	1	0	0	1	1
OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
NOP	No Operation	0	0	0	0	0	0	0	0	1	1