OKI semiconductor

MSM6212

ADPCM 288K ROM VOICE SYNTHESIZER

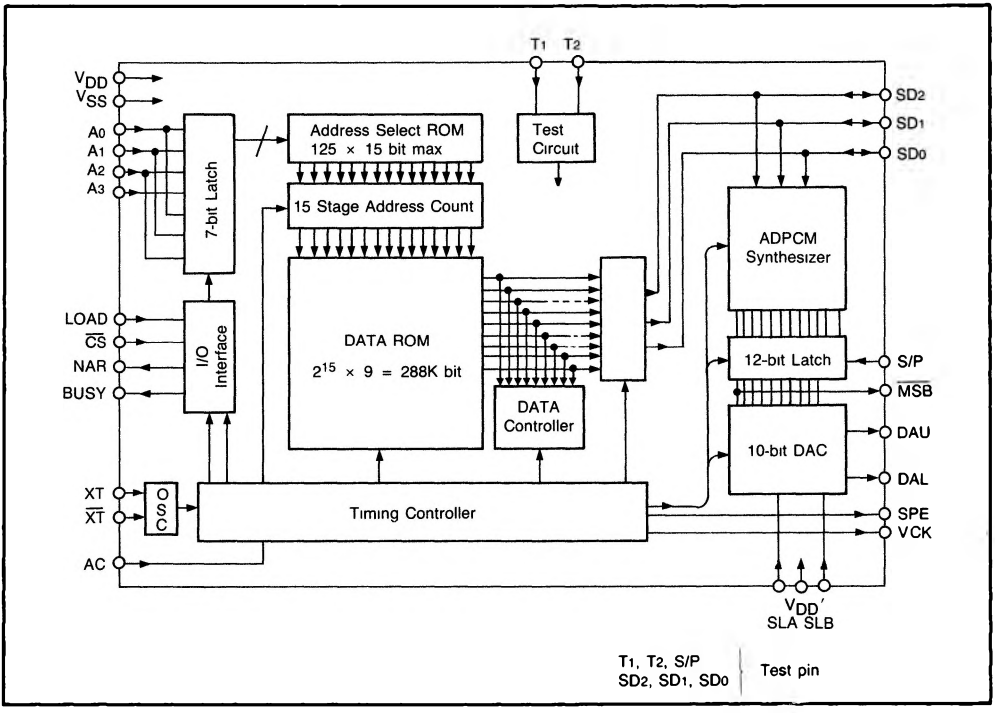
GENERAL DESCRIPTION

MSM6212 is a single-chip ADPCM speech synthesizer incorporating 288K bits ROM to store speech data. In addition to ROM and speech synthesizer circuits, MSM6212 contains an input interface, timing generator circuit and a 10-bit DA converter. Therefore it is possible to configurate a speech output system easily merely by connecting a simple circuit to the speech output consisting of a filter, an amplifier and a speaker.

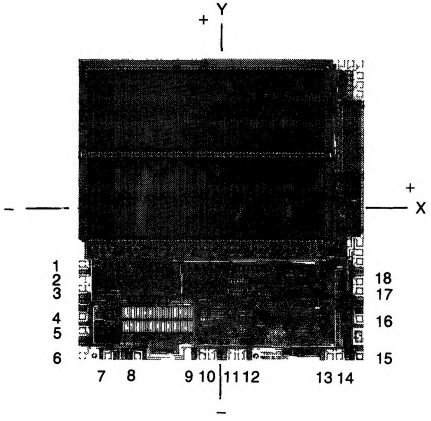
FEATURES

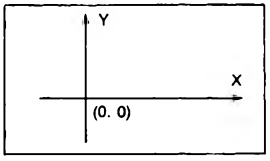
- Low power consumption
- On-chip 288K ROM
- 2 power supply selectable: 3 V or 5 V systems
- Maximum No. of syllable words: 124 words
- Maximum speaking time: 40 sec (compressed ADPCM)
- Class A and Class B analog outputs selectable
- Built-in 10-bit DA converter
- Oscillator frequency: 32,768 kHz
- Available in 40 pin plastic DIP, 60 pin plastic flat package, or die form.

BLOCK DIAGRAM



PAD LAYOUT





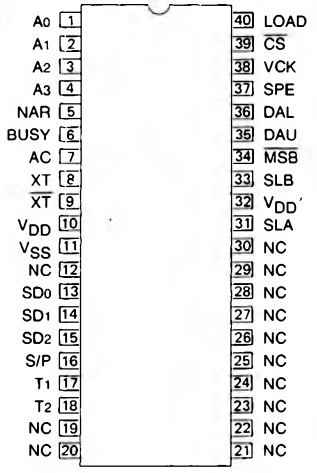
Note: • Chip size: 5.7 mm × 6.0 mm

PAD LOCATION

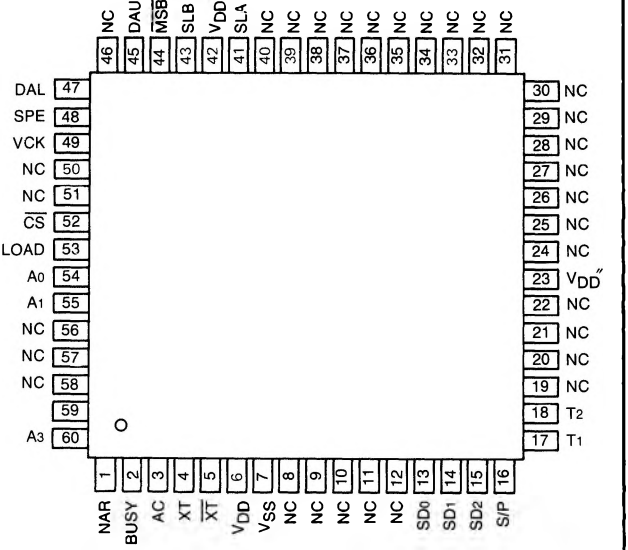
Pad No.	Symbol	Position	
		X	Y
1	SLA	−2699	−1063
2	V_{DD}'	−2699	−1365
3	SLB	−2699	−1545
4	$\overline{MSB}$	−2699	−2091
5	DAU	−2699	−2363
6	DAL	−2699	−2849
7	SPE	−2199	−2849
8	VCK	−1635	−2849
9	$\overline{CS}$	−381	−2849
10	LOAD	−201	−2849
11	A_0	201	−2849
12	A_1	381	−2849
13	A_2	2121	−2849
14	A_3	2301	−2849
15	NAR	2699	−2849
16	BUSY	2699	−2123
17	AC	2699	−1577
18	XT	2699	−1397
19	$\overline{XT}$	2699	−995
20	V_{DD}	2699	−815
21	V_{SS}	2699	−635
22	SD_0	2699	2263
23	SD_1	2699	2443
24	SD_2	2699	2623
25	S/P	2699	2849
26	T_1	2519	2849
27	T_2	2339	2849

PIN CONFIGURATION

(Top View)
40 Lead Plastic DIP
(MSM6212RS)



(Top View)
60 Lead Plastic Flat Package (MSM6212GS)



Note: Connect pin 23 (V_{DD}") with V_{DD} and V_{DD}' externally since this pin is conducted to the substrate.

ELECTRICAL CHARACTERISTICS

3 V System (V_{DD} = 3.1 V Typ)

Absolute Maximum Rating (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +3.6	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Storage Temperature	Tstg	—	−55 to +150	°C

Recommended Operating Range (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	—	+2.4 to +3.6	V
Operating Temperature	Top	—	−10 to +60	°C
DAU and DAL Output Level	V_{OD}	No load	0 to V_{DD}	V

DC Characteristics (V_{DD} = 3.1 V, V_{SS} = 0 V, Ta = 25°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	2.5	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Current *1	I_{IH1}	V_{IH} = 3.1 V	—	—	1	µA
"H" Input Current *2	I_{IH2}	V_{IH} = 3.1 V	10	—	150	µA
"L" Input Current	I_{IL}	V_{IL} = 0 V	—	—	−1	µA
"H" Output Current	I_{OH}	V_{OH} = 2.7 V	−50	—	—	µA
"L" Output Current	I_{OL}	V_{OL} = 0.4 V	50	—	—	µA
Operating Current Consumption	I_{DD1}	—	—	0.1	0.5	mA
Standby current Consumption	I_{DD2}	When selecting class "B" output	—	0.01	0.5	µA
DA Output Accuracy	$\lvert V_E \rvert$	No Load	—	—	100	mV
DA Output Impedance	V_{OR}	—	—	170	—	kΩ

Notes: *1 Applied to AC, LOAD and A_0 to A_3 terminals
*2 Applied to input terminals other than the above.
However, terminals SLA and SLB are applied when AC input is set to "H" (Conform to Note 1 when AC input is set to "L").

5 V System (V_{DD} = 5.0 V Typ)

Absolute Maximum Rating (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to +5.5	V
Input Voltage	V_I		−0.3 to V_{DD}	V
Storage Temperature	Tstg	—	−55 to +150	°C

Recommended Operating Range (V_{SS} = 0 V)

Item	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	—	+4.5 to +5.5	V
Operating Temperature	Top	—	−30 to +70	°C
DAU and DAL Output Level	V_{OD}	No load	0 to V_{DD}	V

DC Characteristics (V_{DD} = 5.0 V, V_{SS} = 0 V, Ta = −30 to +70°C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{IH}	—	4.0	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	1.0	V
"H" Input Current *1	I_{IH1}	V_{IH} = 5.0 V	—	—	1	µA
"H" Input Current *2	I_{IH2}	V_{IH} = 5.0 V	40	—	400	µA
"L" Input Current	I_{IL}	V_{IL} = 0 V	—	—	−1	µA
"H" Output Current	I_{OH}	V_{OH} = 4.6 V	−1	—	—	mA
"L" Output Current	I_{OL}	V_{OL} = 0.4 V	1	—	—	mA
Operating Current Consumption	I_{DD1}	—	—	0.2	0.7	mA
Standby current Consumption	I_{DD2}	—	—	30	100	µA
DA Output Accuracy	$\|V_E\|$	No Load	—	—	130	mV
DA Output Impedance	V_{OR}	—	—	150	—	kΩ

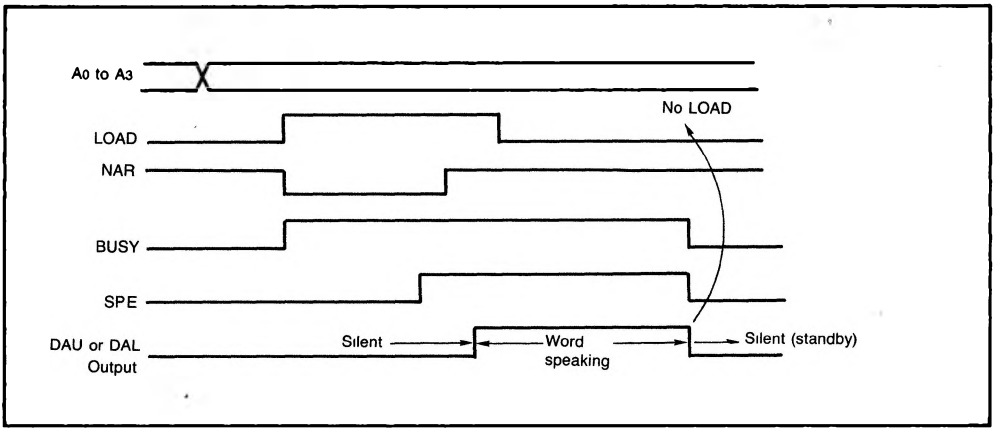
Notes: *1 Applied to AC, LOAD and A_0 to A_3 terminals
*2 Applied to input terminals other than the above. However, terminals SLA and SLB are applied when AC input is set to "H" AC power.
(Conform to Note 1 when AC input is set to "L").

AC Characteristics (Common to V_{DD} = +2.4, +5.5 V, 3 V system and 5 V system)
Ta = −30 to +70°C $f_{(OSC)}$ = 32.768 kHz

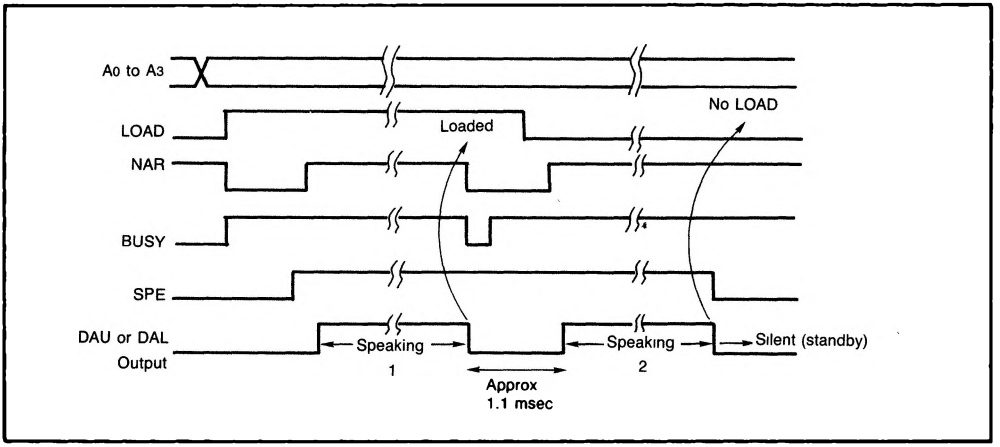
Item	Symbol	Conditions	Min	Typ	Max	Unit
Original oscillation frequency (1)	$f_{(OSC1)}$	3 V system	30	32.768	35	kHz
Original oscillation frequency (2)	$f_{(OSC2)}$	5 V system	30	32.768	65	kHz
Original oscillation duty cycle	f_{duty}	—	40	50	60	%
Load Input Pulse Width	t_L	When f sample = 8.19 kHz	1	—	45	µs
AC Input Pulse Width	$t_{W(AC)}$	—	1	—	—	µs
Sampling Frequency (1)	f_{S1}	$f_{(OSC)}/4$	—	8.192	—	kHz
Sampling Frequency (2)	f_{S2}	$f_{(OSC)}/5$	—	6.554	—	kHz
Sampling Frequency (3)	f_{S3}	$f_{(OSC)}/8$	—	4.096	—	kHz
NAR minimum "H" Level Width	t_{MN}	When f_{S1} is selected	1	—	—	µs
Input Change Standby Time	t_A	When f_{S1} is selected	1	—	—	µs
Load Pulse Interval	t_{NL}	When f_{S1} is selected	5	—	1000	µs

ACTUATION AND NON-OPERATION OF SW INPUT INTERFACE

1. Single Speaking



2. Repeated Speaking



PIN DESCRIPTION

Pin Name	Terminal Number			I/O
	CHIP	40 DIP	60 FLT	
LOAD	10	40	53	I

The LOAD pulse can be applied when NAR level (see below) is "H". When LOAD is set to "H", the code at A_0 to A_3 is transferred into the latch.
A single pulse or a pair of pulses switches the LSI from standby mode to active.

NAR	15	5	1	O

Next address request
NAR indicates whether the LOAD pulse (see above) can be applied or not. "H" level enables while an "L" output disable.
NAR outputs a "H" when the speaking of the current addressed word begins and indicates the next address code can be entered.

$\overline{CS}$	9	39	52	I

Chip select
This pin enables the use of multiple LSI's. It is open when a single LSI is used because it has an internal pull-down resister. If "H" is applied to $\overline{CS}$, the LSI is retained in "standby" mode.

BUSY	16	6	2	O

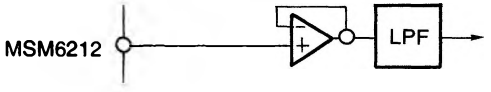
This pin is used for CPU interface, outputting "H" level during the speaking time.

AC	17	7	3	O

All clear
A "H" pulse to this pin stops all internal functions and the LSI switches to standby mode.
No power ON clear circuit is built in the LSI. Therefore, make sure that AC pulse is applied when the power supply is made.

DAU	5	35	45	O
DAL	6	36	47	O

These pins (DAU and DAL) are connected to the output of the 10-bit DA converter. These pins have no built-in LPF because of high output impedance. Use them connected to LPF through the buffer of external low-output impedance.
Example of circuit:

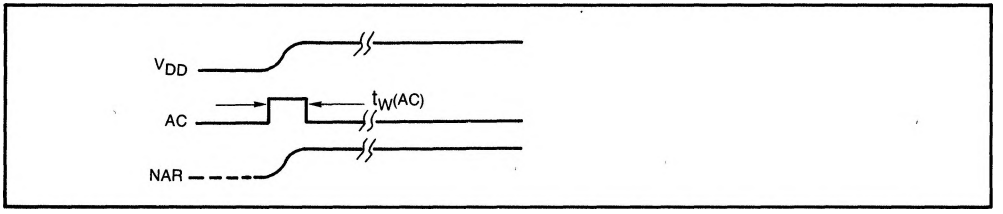


The following class A and class B modes can be obtained from two pins.

SLA	SLB	Mode	Output Pin
Open (L)	Open (L)	Class B × 2	DAU, DAL
V_{DD} (H)	Open (L)	Class B × 1	DAU, DAL
Open (L)	V_{DD}(H)	Class B × 4	DAU, DAL
V_{DD} (H)	V_{DD}(H)	Class A	DAU

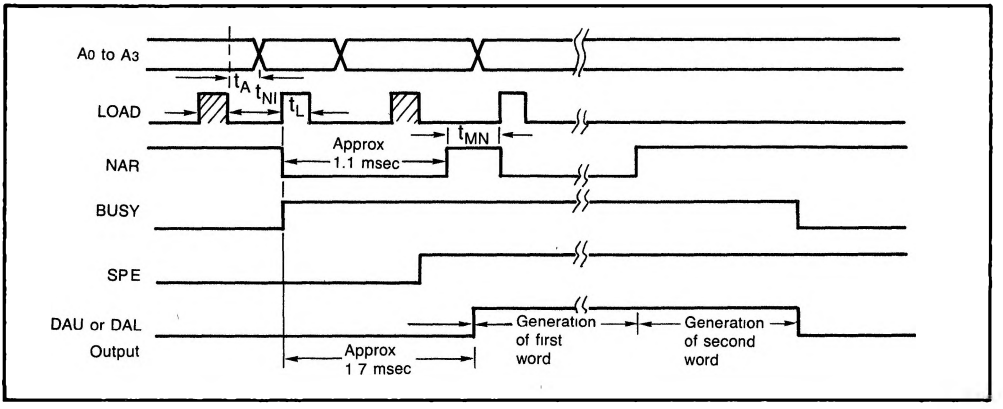
TIMING CHART

1. Power on Sequence

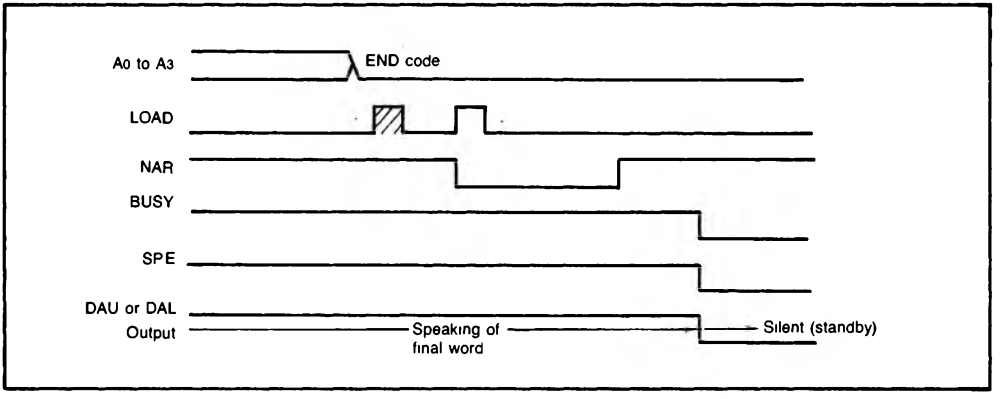


2. LSI Starting and Non-operation (Stand-by)

OPERATING SEQUENCE FOR CPU INTERFACE



FROM OPERATION TO STANDBY IN THE CASE OF CPU INTERFACE



Note: t_A ..... Address hold time
t_{NL} ..... Double LOAD pulse interval
t_L ..... LOAD pulse width
t_{MN} ..... NAR "H" width

FUNCTIONAL DESCRIPTION

DESIGNATION OF SYLLABLE CODES

User can designate syllable codes by A_0 to A_3 and can select either CPU interface or simple interface.

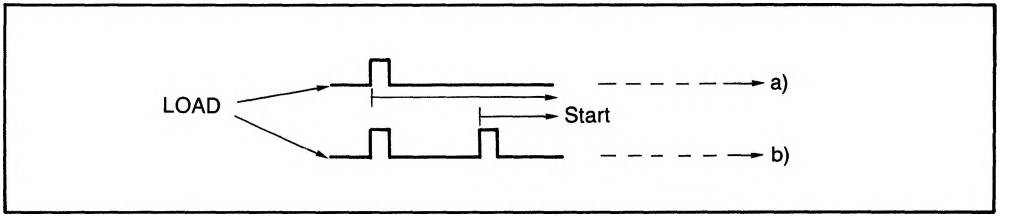
1. CPU Interface

In this case, the maximum number of user's designated words (syllables) is 124. All "L"s represent "END" code. A_0 to A_3 and "LOAD" pulse are related to each other as shown below.

a) Single "LOAD" pulse (The max No. of words is 14)
Input A_0 to A_3 → apply "LOAD" pulse → data is latched internally and at the same time, the LSI is actuated.

b) Two "LOAD" pulses (The max No. of words is 124)
Input A_0 to A_3 → apply first "LOAD" pulse → data is latched internally and LSI retains in "STANDBY" status. → Input A_0 to A_2 (A_3 ignored) → apply second "LOAD" pulse → data is latched internally and at the same time, the LSI is actuated.

For the timing of "LOAD" pulse application, apply it when "NAR" output is at "H" level. For the application of "END" code, conform to the above a) and b).



2. Simple Interface

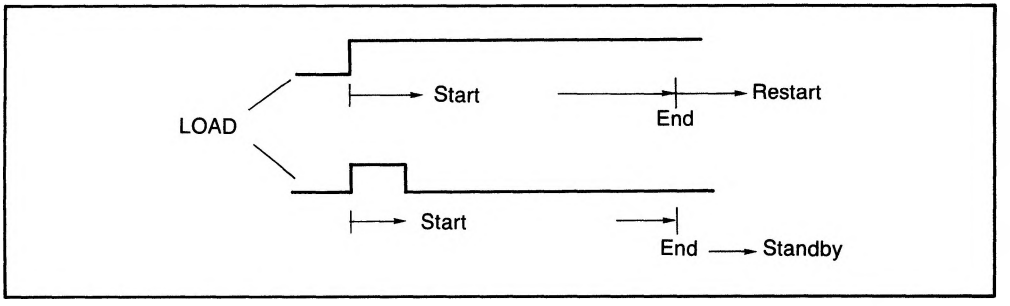
The maximum No. of words is 14. A_0 to A_3 = "H" is a test code.

If "LOAD" input is set at "H" level by means of a push switch after setting of a code by A_0 to A_3, the designated word is spoken (from "Standby" status to "operation" status).

If "LOAD" input is set at "H" level when the speaking of the designated word has ended, the same word is repeated. On the other hand, if "LOAD" input is set at "L" level, LSI is automatically shifted to "STANDBY" status.

Therefore, as long as the push switch continues to be depressed, the same word is repeated. If the push switch is released, the repetition is stopped simultaneous with the ending of speaking.

If the continuous speaking of different words is desired, change codes by A_0 to A_3 and retain "LOAD" input at "H" level, before the speaking of first word is ended.



3. Designation of Sampling Frequency

It is possible for the user to designate the sampling frequency for each word.

The relationship between a sampling frequency and the crystal oscillator frequency is as follows:

When $f_{(OSC)} = 32.768$ kHz

Selection 1 $\quad \frac{32.768\ \text{kHz}}{4} = 8.2$ kHz

Selection 2 $\quad \frac{32.768\ \text{kHz}}{5} = 6.55$ kHz

Selection 3 $\quad \frac{32.768\ \text{kHz}}{8} = 4.1$ kHz

STRAIGHT ADPCM AND COMPRESSED ADPCM

1. Straight ADPCM

The features are enumerated below.

1. Length of ADPCM bits ..... fixed in 3 bits.
2. Deletion of silent component is possible.
3. High bit rate and high tone quality.
4. Suitable to imitation sound.

Example of bit rate

f_{SAMPLE} = 8.2 kHz
Length of ADPCM bits = 3 bits
Deleted silent component ≒ 1/5 (speech)
B•R ≒ 8.2 × 3 × 4/5 ≒ 19.7 kb/sec

2. Compressed ADPCM

The features are enumerated below:

1. Length of ADPCM bits ..... fixed in 3 bits
2. Deletion of data by repeated detection of speech waveform
3. Deletion of silent component is possible.
4. Low bit rate.
5. Mainly applied to speech.

Example of bit rate

f_{SAMPLE} = 8.2 kHz
Length of ADPCM bits = 3 bits
Frequency of average repetition ≒ 3
(Deleted data component of waveform ≒ 1/3)
Deleted silent component ≒ 1/5 (speech)
B•R ≒ 8.2 × 3 × 1/3 × 4/5 ≒ 6.6 kb/sec

SAMPLING FREQUENCY AND BAND WIDTH

1. Simple Relationship between Sampling Frequency and Band Width

$f_{SAMPLE} \times 1/2 = f_{BAND}$ (UL)
Here f_{BAND} (UL) ..... Upper limit of band

f_{SAMPLE}	f_{BAND}	Quality
8.2 kHz	DC to 4.1 kHz	Clear maximum intelligibility
6.55 kHz	DC to 3.2 kHz	Female speech of high tone sounds nasal
4.1 kHz	DC to 2.0 kHz	Unclear both male and female speeches sound nasal

2. The Relationship between a Sampling Frequency and LPF (low pass filter)

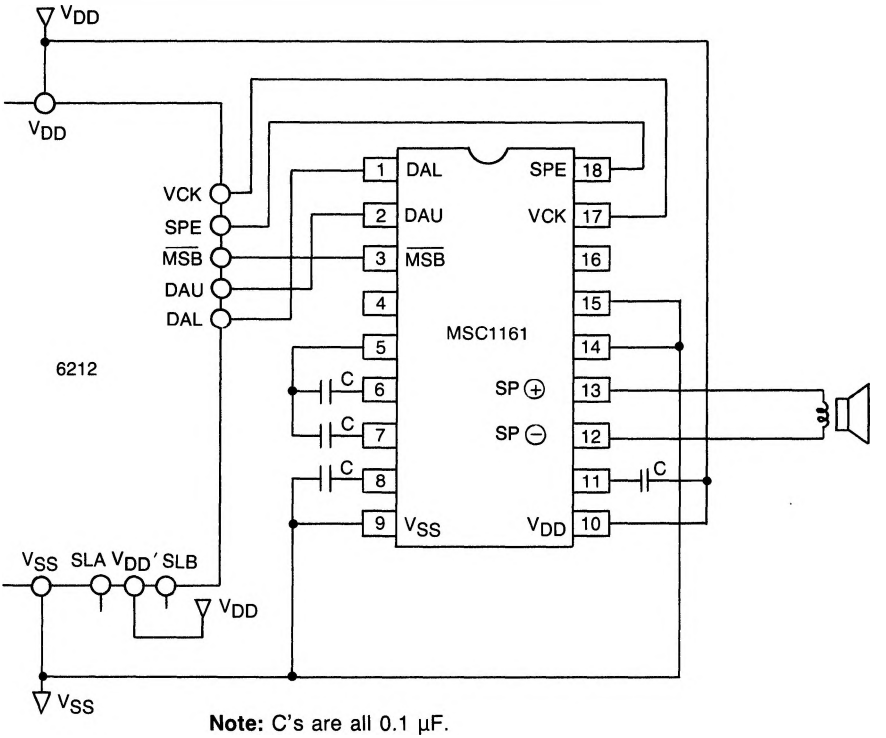
The relationship between a sampling frequency and LPF (low pass filter) is $f_{SAMPLE} \times 1/2 = f_C$ (cutoff frequency of ideal filter). However, realistically it is necessary to design "f_C" to be lower than the above equation according to the skirt characteristics of filter. That is, the band will be further narrowed according to filter characteristics.

As an example, the f_C and skirt characteristics of L.P.F. used for speech analysis by Oki are shown as follows.

f_{SAMPLE}	f_C	Skirt Characteristics	f_{BAND}
8.2 kHz	3.4 kHz	−48 dB/oct	DC to 3.4 kHz
6.55 kHz	2.7 kHz	−48 dB/oct	DC to 2.7 kHz
4.1 kHz	1.7 kHz	−48 dB/oct	DC to 1.7 kHz

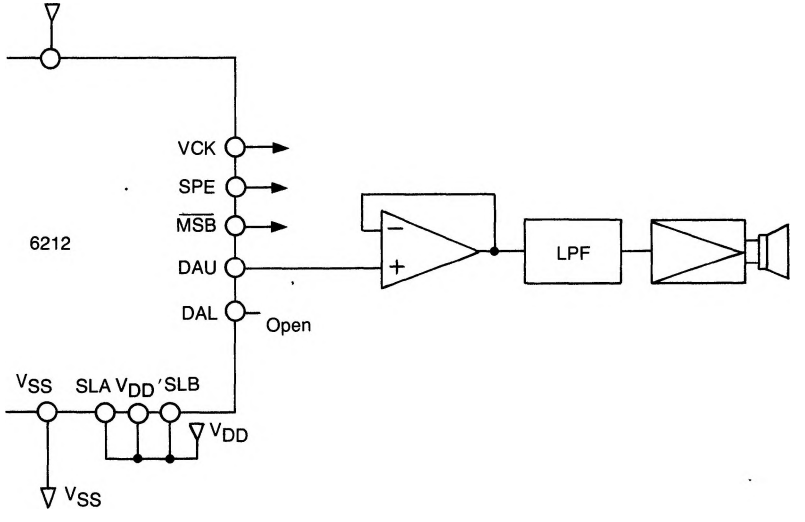
EXAMPLE OF OUTPUT INTERFACE

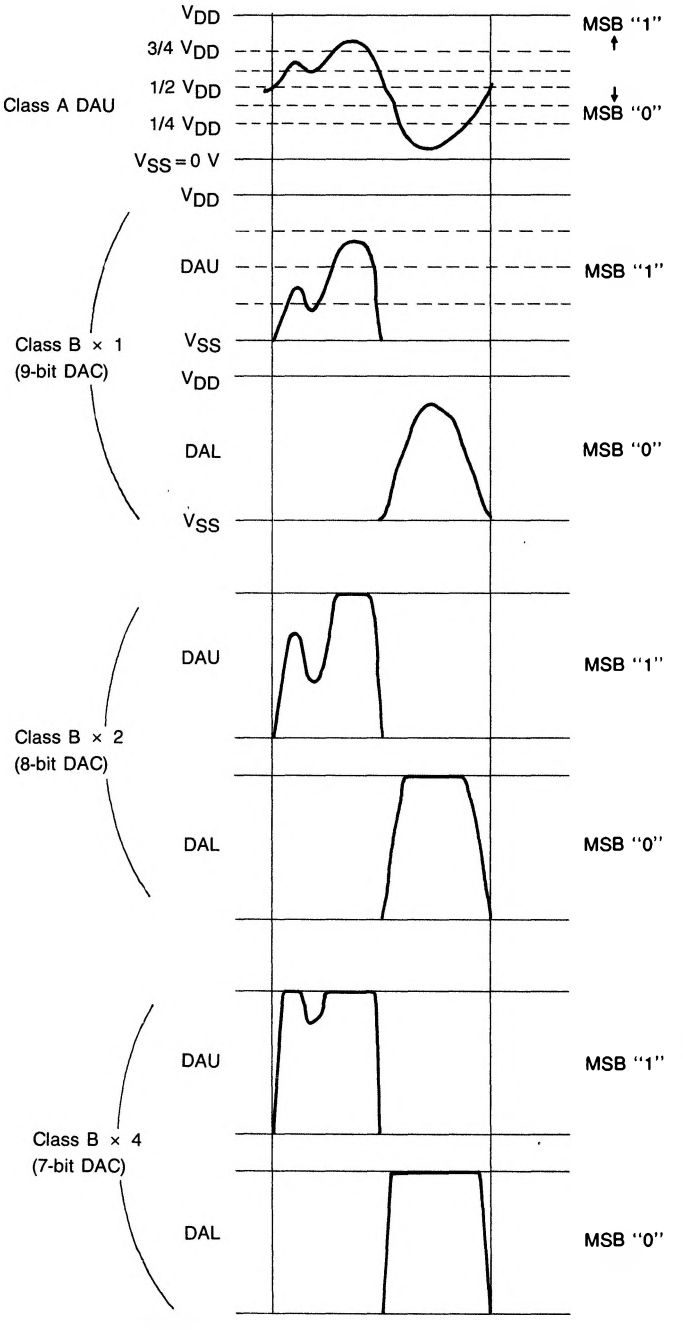
When connected to MSC1161 for Class B (for 3 V system only)



Note: C's are all 0.1 µF.

Class A Output





(An abbreviated name of the type is sometimes used as an indication representing an actual product)