OKI semiconductor

MSM62580

CMOS 8-BIT SINGLE CHIP MICROCONTROLLER WITH 16K BIT E²PROM

GENERAL DESCRIPTION

The MSM62580 is a CMOS one-chip microcontroller with on-board 16K bit E²PROM for applications such as IC-cards, etc.

The powerful instruction set consists of 95 instructions including special instructions for IC cards, executed by the 8-bit CPU in 800 ns at 5.0 MHz clock frequency.

The MSM62580 has improved hardware and software for security. Consequently, this chip suits application such as IC cards of low cost, high security and high reliability.

APPLICATION EXAMPLES

- IC Cards
- Mechanical Controls
- Automobile Controls
- Industrial Controls
- Compact Disc Players
- Audio/Video Equipment
- Household Appliances
- Musical Instruments

FEATURES

High speed instruction cycle

High number of instructions, and an efficient instruction set

(For example)

- Instructions for serial interface : SIN, SOUT, DLY
- Index addressing
- 1 byte call addresing : CZP
- Instructions for auto increment and auto crecrement : INC, DEC

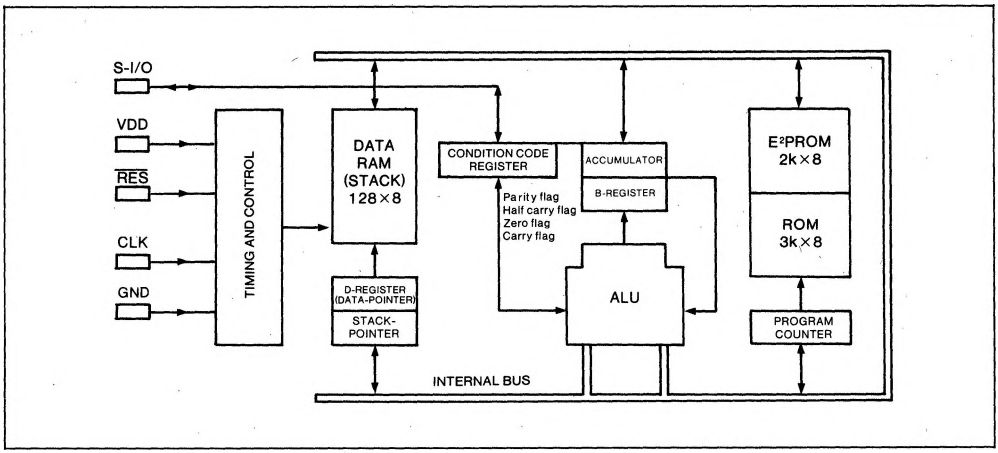
Small package size

- Simplified E²PROM write/erase operation by using control ROM. From D.C to 5 MHz clock frequency
- 9600 baud-rate serial interface using "DLY" instruction.

SPECIFICATIONS

- Single chip, low power CMOS
- 8-Bit Microcontroller
- 3K Bytes program ROM
- 512 Bytes control ROM
- 2K Bytes E²PROM
- 128 Bytes data RAM
- Clock frequency : 0 ~ 5.0 MHz
- Instrucion cycle : 800ns @ 5 MHz
- Number of instructions: 95
- Operation current : 4 mA typ.
- Ambient range : 0 to 70°C
- Number of pads : 5
- Supply voltage : +5 V ± 10%
- Die size : 5.0 × 4.5 mm

BLOCK DIAGRAM



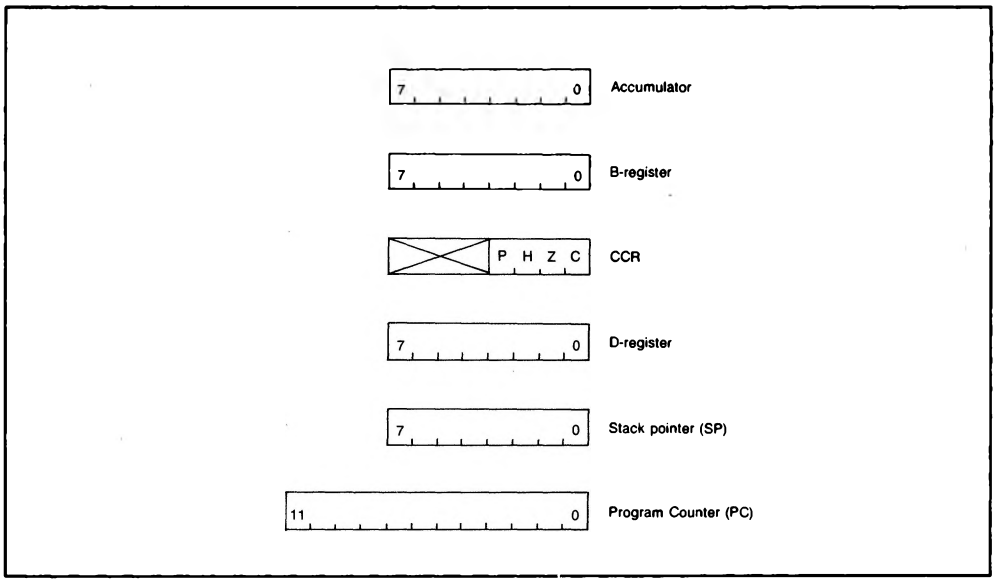
* E²PROM is not used as instruction area.

ALU : Arithmetic Logic Unit
E²PROM : Electrically Erasable-Programmable ROM
ROM : Read Only Memory
RAM : Randam Access Memory (Data memory)

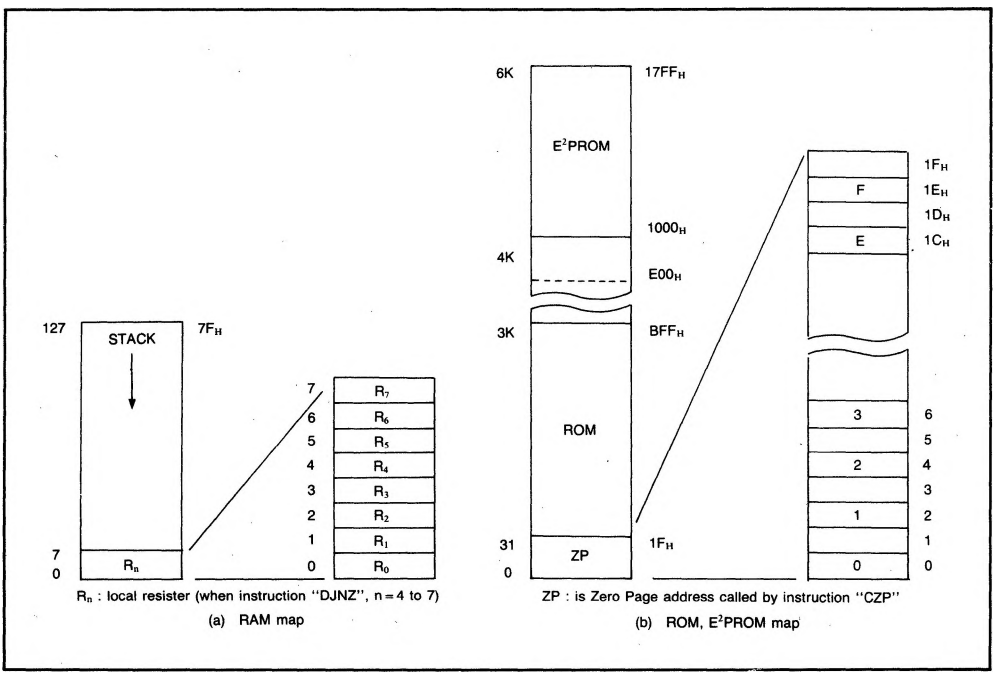
PIN DESCRIPTION

Description	Input/Output	Function
S-I/O	Input/Output	Serial data input/output port. Quasi bidirectional I/O port. Set "1" level after "Reset".
V_{DD}	—	Main power source
GND	—	Circuit GND potential
$\overline{RES}$	Input	"Reset" has priority over every other signal. $\overline{RES}$ input initialize the processor. Active "0" level.
CLK	Input	External clock input

REGISTER DIAGRAM



MEMORY MAP



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.5 to 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 to V_{DD} +0.5	V
Output Voltage	V_O	Ta = 25°C	−0.3 to V_{DD} +0.5	V
Storage Temperature	T_{stg}		0 to +70	°C

OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	4.5 to 5.5	V
Operating Temperature	T_{OP}	0 to +70	°C

D.C. CHARACTERISTICS

(V_{DD} = 5V± 10%, Ta = 0 to +70°C)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Operating Current		I_{DD}	f = 5 MHz	—	4	10	mA
Low Input Voltage	CLK	V_{IL}	—	−0.3	—	0.5	V
	RES			−0.3	—	0.5	
	SIO			−0.3	—	0.8	
High Input Voltage	CLK	V_{IH}	—	2.4	—	V_{DD}	V
	RES			4	—	V_{DD}	
	SIO			2.0	—	V_{DD}	
Low Output Voltage		V_{OL}	I_{OL} MAX = 1.6mA	0	—	0.4	V
High Output Voltage		V_{OH}	I_{OH} MAX = −100≥A	2.4	—	V_{DD}	V
Input Current (CLK, $\overline{RES}$)		I_{IH1}/I_{IL1}	V_I = O/V_{DD}	—	—	20	μA
Input Current (SIO)		I_{IH2}/I_{IL2}		—	—	−1	mA
Input Capacitance		C_I	f = 1MHz Ta = 25°C	—	15	—	pF
Output Capacitance		C_O		—	20	—	pF

Notes: = CLK, $\overline{RES}$ has poll down resistance SIO has pull up resistance.

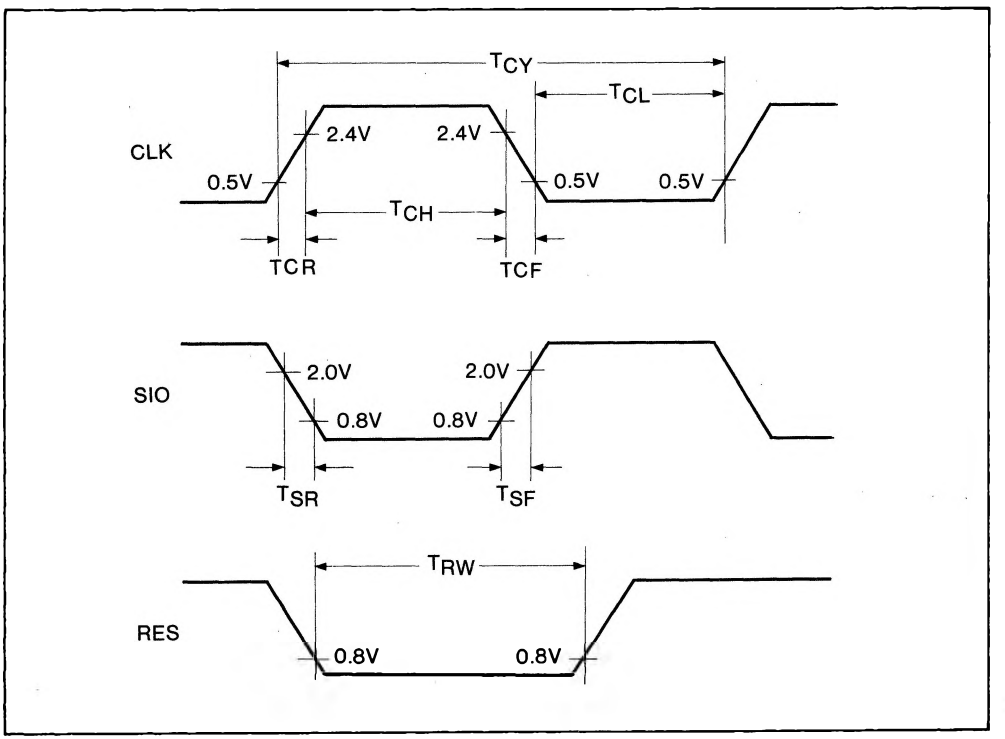
A.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
CLK Cycle Time	T_{CY}	200	—	—	ns
CLK Cycle Low Width	T_{CL}	0.4*T_{CY}	—	0.6*T_{CY}	ns
CLK Cycle High Width	T_{CH}	0.4*T_{CY}	—	0.6*T_{CY}	ns
CLK Cycle Rise Time	T_{CR}	—	—	5.0	μs
CLK Cycle Fall Time	T_{CR}	—	—	5.0	μs
$\overline{RES}$ Pulse Width	T_{RW}	8*T_{CY}	—	—	μs
SIO INPUT Rise Time	T_{SR}	—	—	5.0	μs
SIO INPUT Fall Time	T_{SF}	—	—	5.0	μs

Note: at output capacitance C_O = 30pF

TIMING CHARTS



INSTRUCTION LIST

MNEMONIC	opr	OPERATION	BYTE	CYCLE	FLAGS			
					C	P	H	Z
MOV A, opr	B	A ← B	1	1				*
	D	A ← D	1	1				*
	@D	A ← (D)	1	1				*
	@D+	A←(D), D←D+1	1	2				*
	@D−	A←(D), D←D−1	1	2				*
	N	A ← (N)	2	2				*
	N+D	A ← (N+D)	2	3				*
	#N	A ← #N	2	2				*
MOV opr, A	B	B ← A	1	1				
	D	D ← A	1	1				
	@D	(D) ← (A)	1	1				
	@D+	(D)←A, D←D+1	1	2				
	@D−	(D)←A, D←D−1	1	2				
	N	(N) ← A	2	2				
	N+@D	(N+D) ← A	2	3				
MOV D, opr	Rn	D ← Rn	1	2				
	#N	D ← #N	2	2				
MOV Rn, opr	D	Rn ← D	1	2				
	#N	Rn ← #N	2	3				
MOV @BA, opr	@D	(BA) ← (D)	1	4				
MOV @D, opr	@BA	(D) ← (BA)	1	4				
MOV @D+, opr	#N	(D)← #N,D←D+	2	2				
MOVW @D+, opr	BA	(D)←A, (D+1)←B	1	3				
MOVW BA, opr	@D	A←(D), B←(D+1)	1	3				*
MOVW BA, opr	#N	A← #N1, B← #N2	3	3				*

MNEMONIC	opr	OPERATION	BYTE	CYCLE	FLAGS			
					C	P	H	Z
XCH A, opr	B	A ↔ B	1	2				*
	D	A ↔ D	1	2				*
	@D	A↔(D)	1	2				*
	N	A ↔ (N)	2	2				*
XCH D, opr	B	D ↔ B	1	2				
	SP	D ↔ SP	1	2				
XCH C, opr	P	C ↔ P	1	1	*	*		
ADD A, opr	@D	A ← A+(D)	1	1	*		*	*
	N	A ← A+(N)	2	2	*		*	*
	#N	A← A+ #N	2	2	*		*	*
ADC A, opr	@D	A←A+(D)+C	1	1	*		*	*
	N	A←A+(N)+C	2	2	*		*	*
	#N	A←A+ #N+C	2	2	*		*	*
DAA		Decimal adjust	1	1	*			*
CMP A, opr	@D	A ← (D)	1	1	*			*
	N	A ← (N)	2	2	*			*
	#N	A ← #N	2	2	*		*	*
CMP @D, opr	@BA	(D) ← (BA)	1	4	*			*
EOR A, opr	@D	A ← AV(D)	1	1				*
	N	A ← AV(N)	2	2				*
	#N	A ← AV#N	2	2				*
OR A, opr	@D	A ← AV(D)	1	1				*
	N	A ← AV(N)	2	2				*
	#N	A ← AV#N	2	2				*
AND A, opr	@D	A ← A (D)	1	1				*
	N	A ← A #(N)	2	2				*
	#N	A ← A #N	2	2				*

MNEMONIC	opr	OPERATION	BYTE	CYCLE	FLAGS			
					C	P	H	Z
INC opr	A	A ← A+1	1	1				*
	D	D ← D+1	1	1				
	@D	(D) ← (D)+1	1	1				*
	N	(N) ← (N)+1	2	2				*
DEC opr	A	A ← A−1	1	1				*
	D	D ← D−1	1	1				
	@D	(D) ← (D)−1	1	1				*
	N	(N) ← (N)−1	2	2				*
RRC opr	A	↳C → A7 ~0┘	1	1	*			*
	@D	↳C → (D)7~0┘	1	1	*			*
	N	↳C → (N)7~0┘	2	2	*			*
RLC opr	A	└C ← A7 ~0↵	1	1	*			*
	@D	└C ← (D)7~0↵	1	1	*			*
	N	└C ← (N)7~0↵	2	2	*			*
PUSH opr	PSW	(SP)←A,(SP−1)←CCR, SP←SP−2	1	3				
	D	(SP)←D, SP←SP−1	1	2				
POP opr	PSW	CCR←(SP−1), A←(SP−2), SP←SP+2	1	3	*	*	*	*
	D	D←SP+1, SP←SP+1	1	2				
JZ opr	addr	if Z=1, PC←PC+2+addr	2	2/3				
JNZ opr	addr	if Z=1, PC←PC+2+addr	2	2/3				
JC opr	addr	if C=1, PC←PC+2+addr	2	2/3				
JNC opr	addr	if C=1, PC←PC+2+addr	2	2/3				
JB opr	baddr,addr	if(baddr)=1,PC←PC+3+addr	2	3/4				
JNB opr	baddr,addr	if(baddr)=1, PC←PC+3+addr	2	3/4				
DJNZ opr	Rn,addr	Rn←Rn-1, if Rn=0, PC←PC+2+addr (n=4~7)	2	3/4				
JMNE opr	#N,addr	if (D) ≠ #N, PC←PC+3+addr	3	3/4				
JDNE opr	#N,addr	if D ≠ #N, PC←PC+3+addr	3	3/4				

MNEMNIC	opr	OPERATION	BYTE	CYCLE	FLAGS			
					C	P	H	Z
JMP opr	addr	PC←addr(0～4K)	2	2				
CAL opr	addr	(SP)←PC+2, PC←addr(0～4K) SP←SP-2	2	4				
CZP opr	addr	(SP)←PC+2,PC←ZP,SP←SP-2	1	4				
RT		PC←(SP), SP←SP+2	1	3				
NOP		No Operation	1	1				
CLR opr	A	A ← 0	1	1				1
RC		C ← 0	1	1	0			
SC		C ← 1	1	1	1			
RB	baddr	(baddr) ← 0	2	2				
SB	baddr	(baddr) ← 1	2	2				
CPL opr	A	A ← $\overline{A}$	1	1				*
	C	C ← $\overline{C}$	1	1	*			
CHK opr	P	P←C, if A=odd, C←1 ELSE C←0	1	1	*	*		
SIN		C ← SIO	1	1	*			
SOUT		SI/O ← C	1	1				
DLY opr	#N	DELAY N+3 CYCLES	2	3～258				