Preliminary

OKI semiconductor

MSM6295

4-CHANNEL ADPCM VOICE SYNTHESIS LSI

GENERAL DESCRIPTION

The Oki MSM6295 is a 4-channel ADPCM voice synthesis LSI which is fabricated using Oki's low power CMOS silicon gate technology.

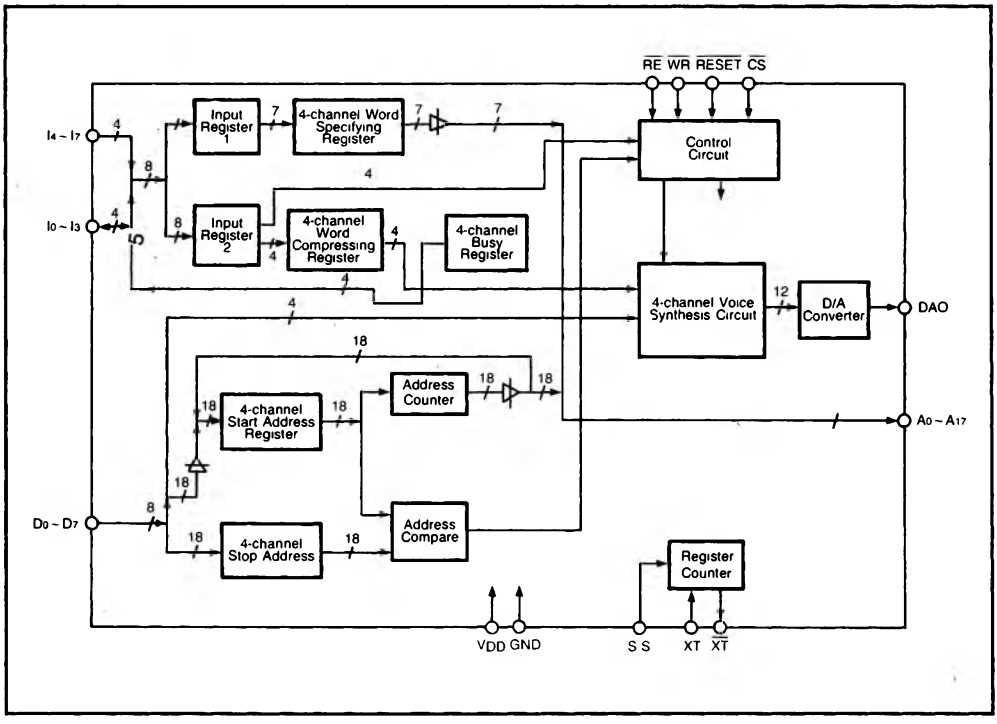
The MSM6295 can access an external ROM, where speech or sound effect data is stored. The maximum size ROM is 256K bytes.

The MSM6295 has a 4-channel synthesis stage which allows the simultaneous playback of four different channels. So, it is quite useful to have a voice with BGM effect, instrumental sound, echo etc.

FEATURES

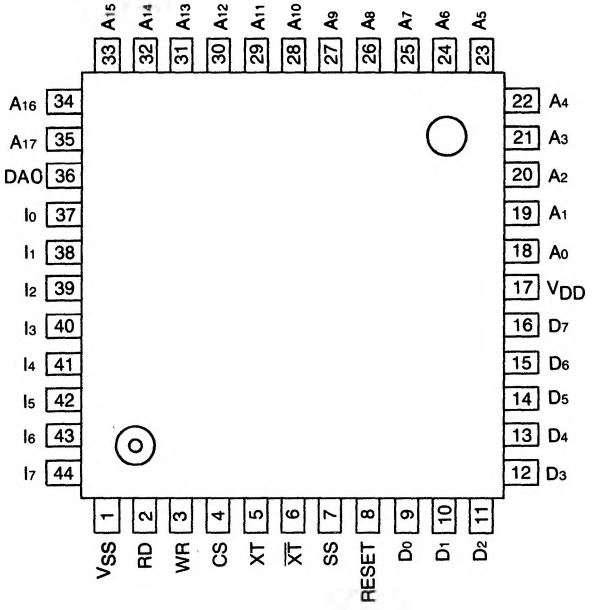
- Oki straight ADPCM algorithm
- Number of bits/sample: 4
- 18 address lines for external ROM
- 8-bit control bus for mode setting
- External memory capacity 2M-bit
- Interface with common CPU and MPU
- Clock frequency: 1 MHz and 4 MHz
- Sampling frequency: 6.4 kHz and 8 kHz (@ 1 MHz clock)
  25.6 kHz and 32 kHz (@ 4 MHz clock)
- Number of words: 127 maximum
- Vocalization time: 60 sec maximum (@ 8 kHz, straight)
- Built-in DA converter: 12-bit
- DA output format: A class
- Voice level reduction on each channel: −3 dB ~ −24 dB (8 steps) −3 dB/step
- Low power CMOS process
- 3 V or 5 V single power supply
- 44 pin plastic flat package

BLOCK DIAGRAM



PIN CONFIGURATION

44 pin Flat Package



PIN DESCRIPTION

Pin Symbol	Pin No.	I/O	Function
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7	37 38 39 40 41 42 43 44	I/O I/O I/O I/O I I I I	Data bus and condition output These terminals are inputs of phrase specification. Maximum number of phrases is 127. Also, $I_0 \sim I_3$ terminals are outputs of operating state, busy state, for 1 ~ 4 channel.
$\overline{WR}$	3	I	Writing input Write the data on the data bus of $I_0 \sim I_7$. The data is written by the setting-up of $\overline{WR}$.
$\overline{RD}$	2	I	Reading out input Output busy state of 1 ~ 4 channel on the data bus of $I_0 \sim I_3$. "L" level or "H" level is output while RD is "L". When it becomes "H", busy state is output.

PIN DESCRIPTION (continued)

Pin Symbol	Pin No.	I/O	Function
$\overline{CS}$	4	I	Chip selection input Input "L" level either when $\overline{WR}$ signal is input or when $\overline{RD}$ signal is input.
$\overline{RESET}$	8	I	Reset input Reset condition is available by inputting "L" level. All functions are suspended during reset.
A_0 ( ) A_{17}	18 ( ) 35	I ( ) I	Address output These terminals are to addresses the external ROM in which original voice data is stored.
D_0 ( ) D_7	9 ( ) 16	I ( ) I	Input of original voice data Input the data from external ROM which stores original voice data.
SS	7	I	Sampling input Selecting sampling frequency. When oscillation frequency is 1.18 MHz or 4.13 MHz, following choices are available by inputting "H" level or "L" level into SS.
			SS="H" / SS="L" Oscillation frequency 1.18 MHz: 8 kHz / 6.4 kHz Oscillation frequency 4.13 MHz: 32 kHz / 25.6 kHz
DA_0	36	O	Voice synthesis output Voice synthesized analog signal is output from this terminal.
XT	5	I	Crystal oscillator connector terminal.
$\overline{XT}$	6	O	Same as above
V_{DD}	17	I	Power supply terminal
V_{SS}	1	I	Ground

FUNCTION EXPLANATION

1. Phrase Specification

Phrases are specified and read into the 2 byte data which is made up of $I_0 \sim I_7$ data bus. The phrases specification data are latched when $\overline{WR}$ goes high while $\overline{CS}$ keeps low (L).
Format of phrase specification input is as follows.

	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1 Byte	1	Phrase specification data						
2 Byte	Channel specification				Reduction specification			

As shown in the above chart, I_7 of the first 1 byte data is 1. $I_0 \sim I_6$ of the first 1 byte data specifies the phrase. Phrase specification data has a selection of 127 phrases which corresponds to 0000001 ~ 1111111. The phrase specification data is equivalent to $A_3 \sim A_9$ address outputs, and specify both start and stop address which are stored in the external out ROM.

CORRESPONDENSE BETWEEN PHRASE SPECIFICATION DATA AND ROM ADDRESS

Phrase specification data	—	I_6	I_5	I_4	I_3	I_2	I_1	I_0	—	—	—
External ROM address	$A_{17} \sim A_{10}$	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Specification Not Valid	0 ~ 0	0	0	0	0	0	0	0	0	0	0
Phrase 1	0 ~ 0	0	0	0	0	0	0	1	0	0	0
Phrase 2	0 ~ 0	0	0	0	0	0	1	0	0	0	0
Phrase 3	0 ~ 0	0	0	0	0	0	1	1	0	0	0
Phrase 127	0 ~	1	1	1	1	1	1	1	0	0	0

* Phrases cannot be specified with all 0s.

The second byte of data specifies the synthesis operation channel as well as channel specific reduction of playback synthesis sound. As to the format of channel specification, please refer to the following chart for channel specification format.

CHANNEL SPECIFICATION

Channel	I_7	I_6	I_5	I_4
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

It is impossible to specify multiple channels at the same time. For example, it is impossible to specify channel 1 and channel 3 simultaneously.

REDUCTION SPECIFICATION

All 0 is considered as 0 dB, the analyzed sound itself. The reduction is made through 8 levels from about −3 dB to −24 dB with the steps of about −3 dB. As to the format for reduction, please refer to the following chart.

REDUCTION SPECIFICATION

Reduction rate	I_3	I_2	I_1	I_0
0 dB	0	0	0	0
− 3.2 dB	0	0	0	1
− 6.0 dB	0	0	1	0
− 9.2 dB	0	0	1	1
−12.0 dB	0	1	0	0
−14.5 dB	0	1	0	1
−18.0 dB	0	1	1	0
−20.5 dB	0	1	1	1
−24.0 dB	1	0	0	0

2. Channel Voice Synthesis Suspension

Voice synthesis operation of any channel can be suspended. Its data consists of 1 byte of data. To suspend a channel, make I_7 = 0. And I_3 ~ I_6 represent the channel which should be suspended.

Suspended channel	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
1	0	0	0	0	1	X	X	X
2	0	0	0	1	0	X	X	X
3	0	0	1	0	0	X	X	X
4	0	1	0	0	0	X	X	X

Channel suspension occurs even if multiple channels are specified. For example, if I_3 ~ I_6 are all 1, channels 1 ~ 4 are suspended simultaneously.

3. Data ROM

1. ADDRESS DATA

This specifies start and stop address of ADPCM sound source data. One sound address data consists of 8 bytes. The first 3 bytes show start address while the last 3 bytes show stop address. The other 2 bytes are empty.
By specifying the first address in which the start address is stored, the sound source which should be synthesized is selected.

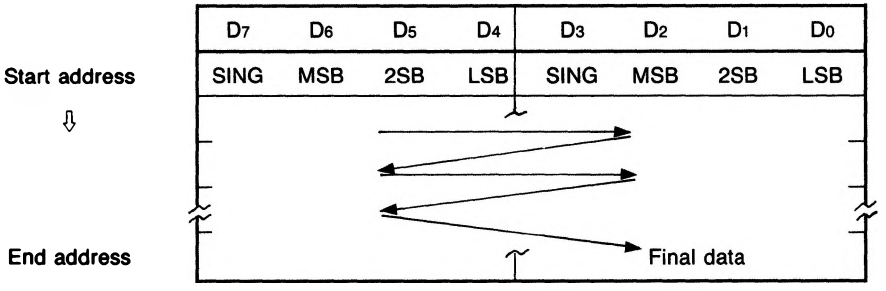
Address 0	SA_1
1	SA_2
2	SA_3
3	EA_1
4	EA_2
5	EA_3
6	EMPTY
7	EMPTY

Start address (SA_1 ~ SA_3) and stop addresses (EA_1 ~ EA_3) are stored according to the chart shown below.

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_1, EA_1	0	0	0	0	0	0	A_{17}	A_{16}
SA_2, EA_2	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
SA_3, EA_3	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

2. ADPCM SOUND SOURCE DATA

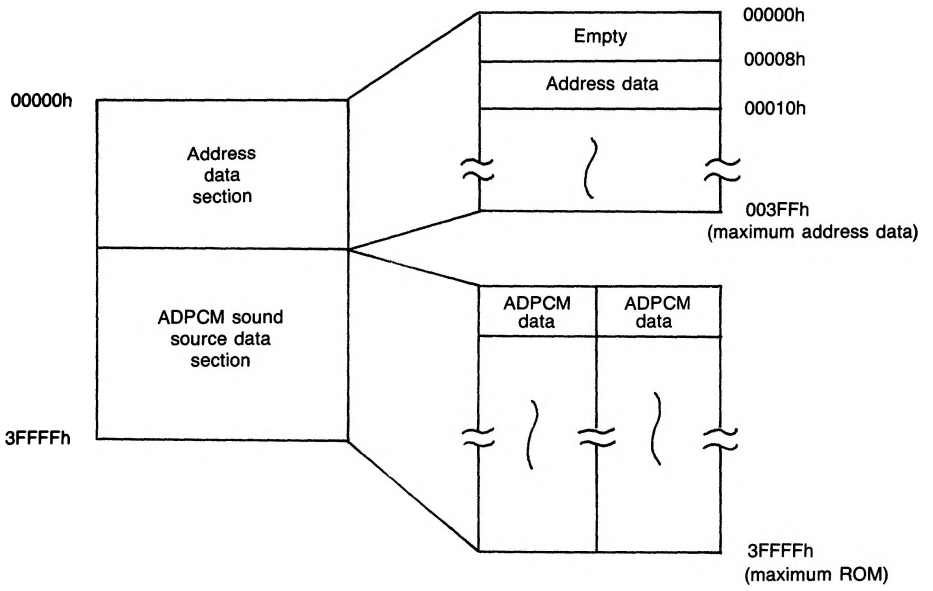
ADPCM sound source data consists of 1 sample for every 4 bits. So, 1 byte stores data of 2 samples. Data arrangement proceeds from higher rank bits (D_4 ~ D_7) to lower rank bits (D_0 ~ D_3). The construction of sound source data should always be ended with lower rank bit. So, construct it with even number of samples.



Sound source data is compatible with the data which is analyzed by MSM5218 or MSM6258. In addition, the data which is analyzed by analyzer is usable, too.

3. STRUCTURE OF SOUND SOURCE DATA ROM

Following chart shows the memory map of the sound source data ROM.

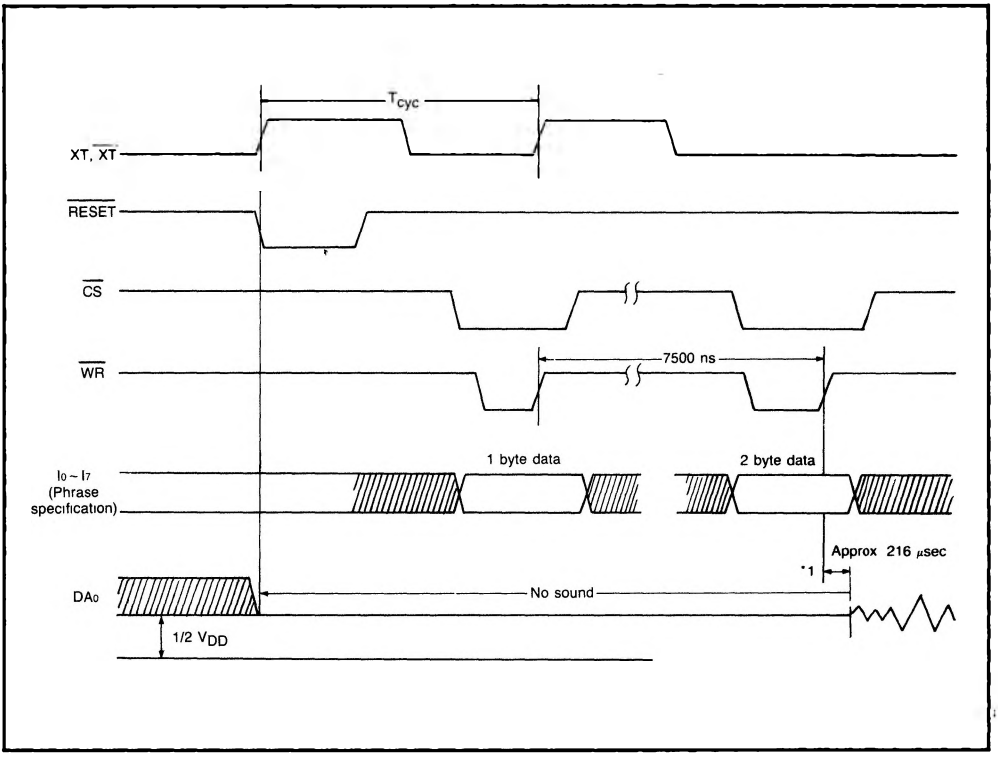


When the maximum 127 phrases are selected in address data section, the data is written up to ROM address 003FFh.
When 1 phrase is selected, address data is written from ROM address 00008h to 0000Fh, and the rest is used as the ADPCM data section.

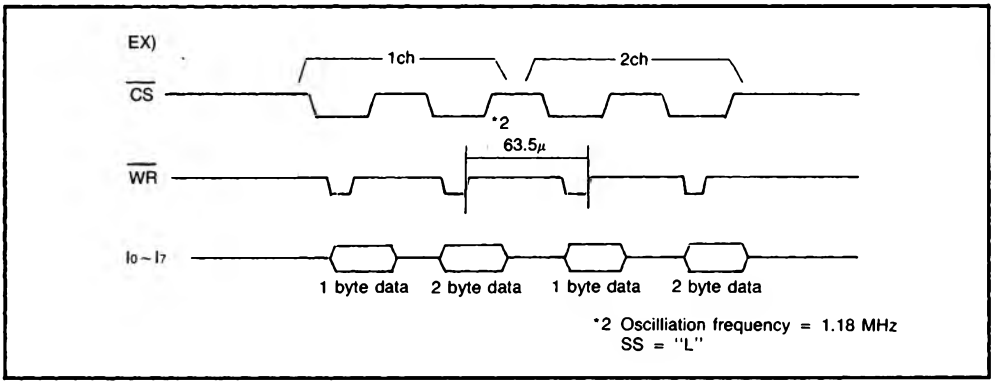
FUNCTIONAL DESCRIPTION

1. Phrase Specifying Input

This procedure is to input phrase specifying data onto the data bus input $I_0 \sim I_7$. The data is latched inside when $\overline{WR}$ goes "L" to "H" while $\overline{CS}$ remains "L".
Voice synthesis operation does not start till the second byte is fully latched.



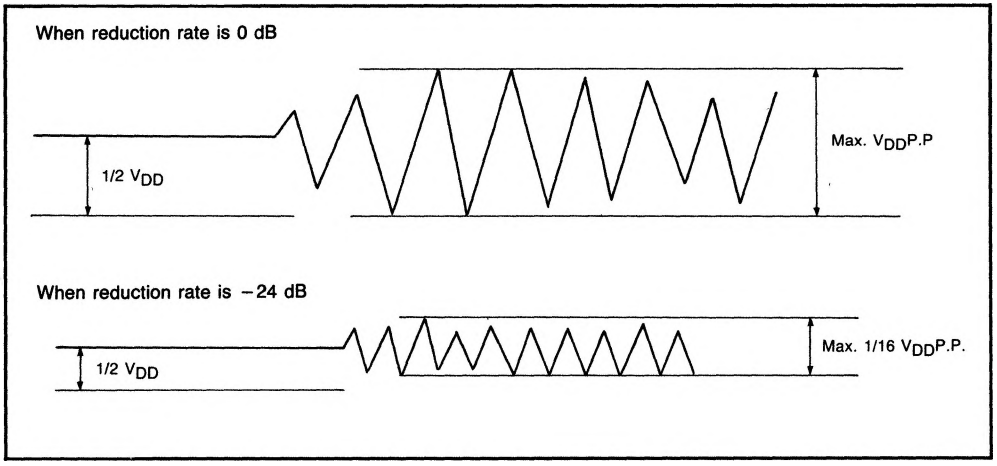
Phrase specifying input is from channel 1 to channel 4 continuously. *1 An interval of 15 Tcyc (max.) is needed between phrases.



Voice synthesis operation can be started from any channel, 1 to 4. The arrangement of each channel is of no concern.

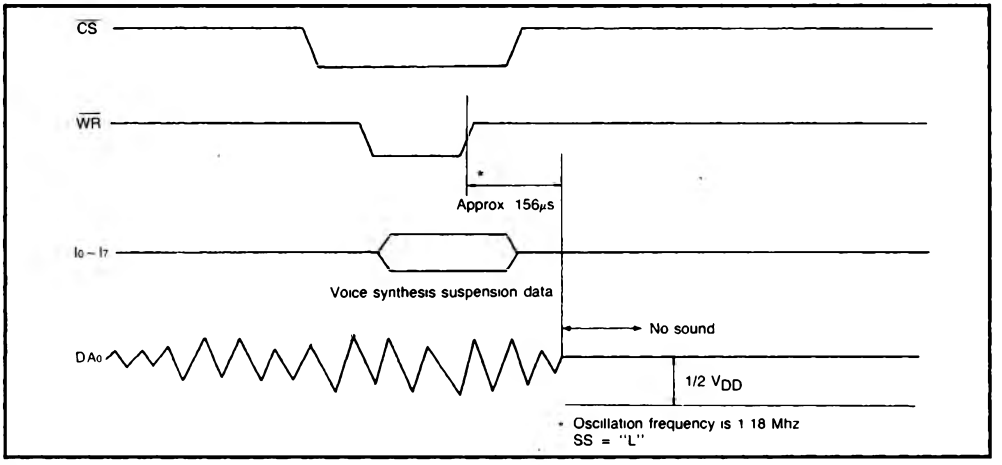
2. Reduction of Synthesized Sound

This procedure is made by the second byte of phrase specifying data. Considering all 0 data of I_0 ~ I_3 as 0 dB, synthesized sound is reduced between approx. −3 dB and −24 dB with the steps of −3 dB.



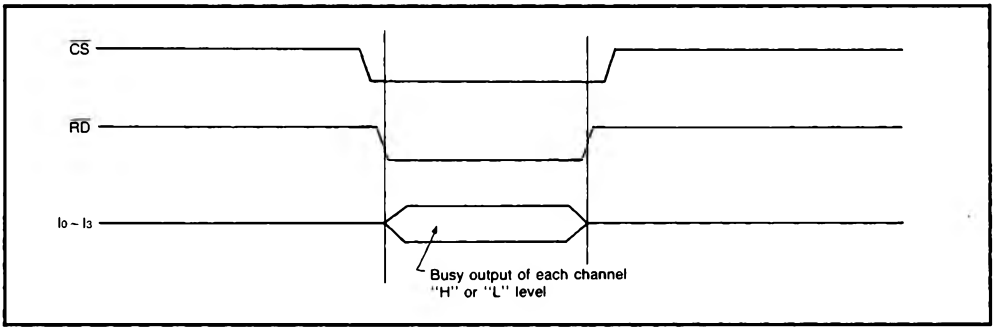
3. Channel Voice Synthesis Suspension

This is accomplished by inputting synthesis suspension data onto data bus input $I_3 \sim I_7$. The data is latched inside when $\overline{WR}$ goes from "L" to "H" while $\overline{CS}$ remains active (L). Since synthesis suspension data is 1 byte data, synthesis operation is suspended right after $\overline{WR}$ is input. Multiple channels can be specified. Therefore it is possible to make suspended channels 1 ~ 4 simultaneously.



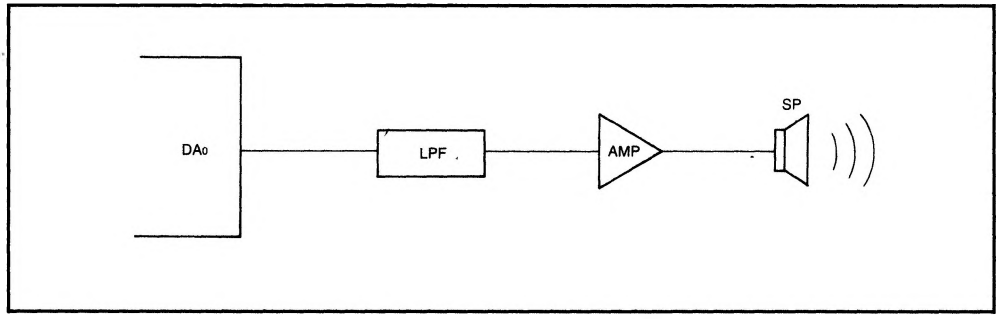
4. Reading-out of Busy State

While $\overline{CS}$ is "L" and $\overline{RD}$ is "L", each operation state, busy state of channels 1 ~ 4 is output on $I_0 \sim I_3$. "H" is output during the operation.



5. Output of Voice Synthesized Sound

MSM6295 has a 12 bit A class (voltage type) DA converter on chip. So, analog signal is available from DA_0 terminal.
DA_0 turns approx. 1/2 V_{DD} (when no sound is output) right after power supply is on. This terminal outputs the amplitude of max. V_{DD}p.p.
To output sound connects LPF and AMP to DA_0 terminal.



APPLICATION CIRCUIT

Interface with Microcontroller