OKI semiconductor

MSM6352

CMOS 4BIT SINGLE CHIP LOW POWER MICROCONTROLLER FOR TELEPHONE

GENERAL DESCRIPTION

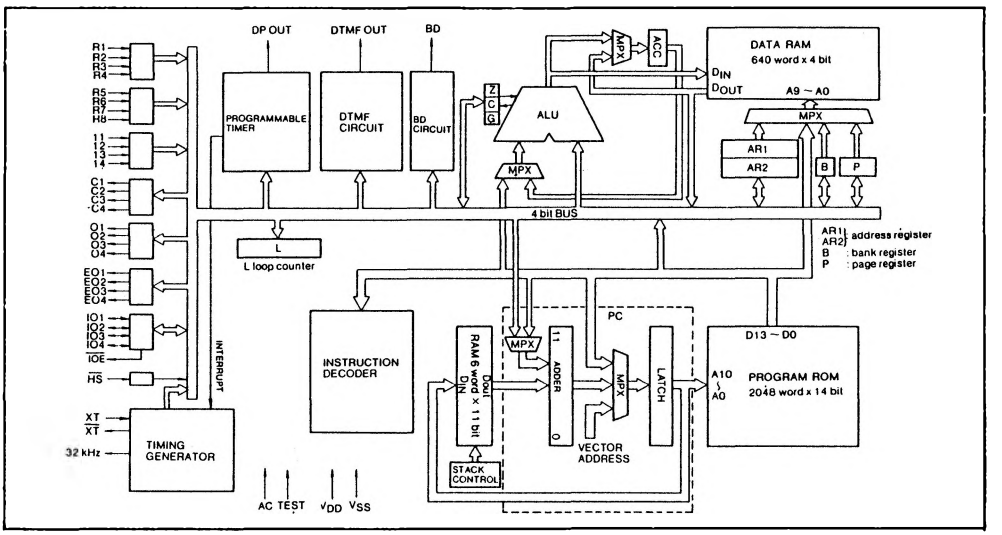
The OKI MSM6352 is a low-power, high-performance single-chip 4-bit microcontroller employing complementary metal oxide semiconductor technology, especially designed for use in sophisticated telephone sets. Integrated onto a single chip are a 4-bit ALU, 28K bits of mask programmable ROM, 2560 bits of data RAM, programmable timer, oscillator, 12-bits of input port, 12-bits of output port and 4-bits of input/output port. In addition to these units, a DTMF generator is provided.

With the MSM6352, sophisticated telephone sets become feasible through a single chip instead

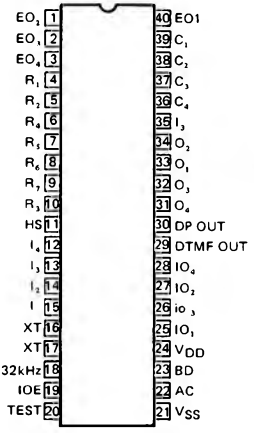
FEATURES

- Low Power Consumption 1.8mA Typical @3V (DTMF output off)
- 2048 × 14 Internal ROM
- 640 × 4 Internal RAM
- 3 × 4 Input Port
- 3 × 4 Output Port
- 1 × 4 Input/Output Port
- DTMF Generator (Single Tone Mode or Dual Tone Mode)
- Buzzer Sound Output
- 4 Bits Programmable Timer Applicable for Output of Dial Pulse
- Watch Dog Timer
- On Hook Dialing and Off Hook Dialing Function
- Interrupt
  Programmable Timer-Interrupt
  Real Time Interrupt
- 5 Level Stack
- Power Down Mode
- 52 Instruction Set
- Instructions Useful for Data Management (Data Search and Block Data Transfer)
- 2.0 to 5.5V (2.2 to 5.5V at TONE MODE) Operating Voltage
- Low Voltage Detector
- 3.58 MHz Oscillator
- 17.9 μs Instruction Cycle
- −20 to 75°C Operating Temperature
- 28 Pin DIP, 40 Pin DIP or 44 Pin FLAT
- Software Compatibility with MSM6052

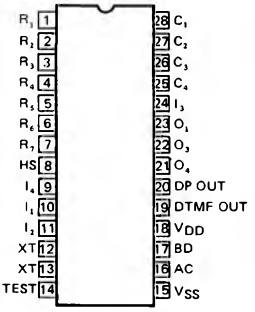
FUNCTIONAL BLOCK DIAGRAM



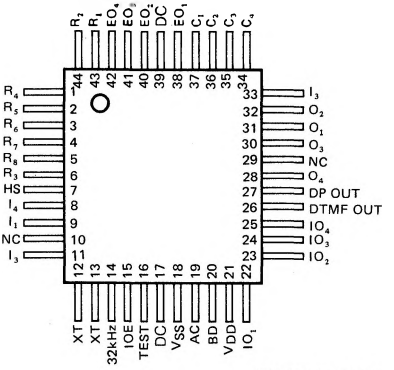
PIN CONFIGURATION



(a) 40 Lead Plastic DIP



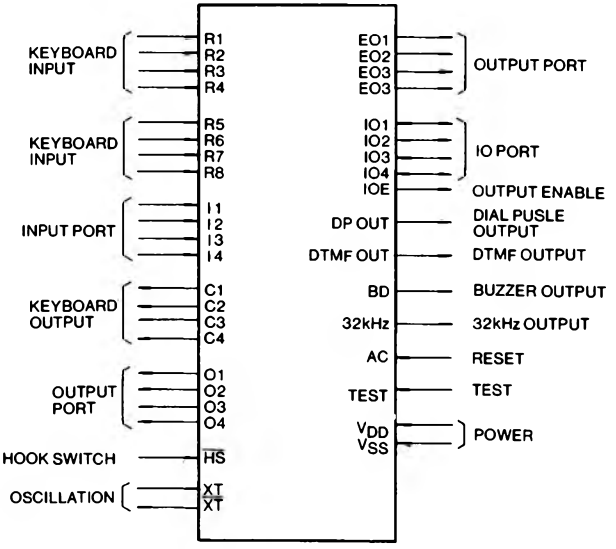
(b) 28 Lead Plastic DIP



DC: Don't connect.

(c) 44 Lead Plastic Flat Package
(NC pin must not be connected to any signal.)

LOGIC SYMBOL



PIN DESCRIPTION

Designation	Function
V_{DD}	Pource source
V_{SS}	Circuit ground potential
AC	Terminal to clear internal logic, pulled down to V_{SS}. After power is turned on, the MSM6052 must be reset by this terminal.
TEST	Terminal to test internal logic, pulled down to V_{SS}. This terminal must be open in normal operation.
XT, $\overline{XT}$	Input and output terminals of oscillator inverter. 3.58 MHz ceramic resonator is connected to these terminals.
$\overline{HS}$	Input terminal connected to the hook switch, pulled up tp V_{DD}.
DP OUT	Output terminal of dial pulse. Dial pulse rate (10 pps or 20 pps) and Make Break ratio (40% or 33 %) can be selected by software.
DTMF OUT	Output terminal of DTMF signal
BD	Output terminal of buzzer sound
32 kHz	Output terminal of 32 kHz clock
$R_1 \sim R_4$ $R_5 \sim R_8$	Input port pulled down to V_{SS}.
$I_1 \sim I_4$	Input port having clocked pull-down resistor to V_{SS}. Only when this port is accessed, pull-down resistors are connected to this port.
$C_1 \sim C_4$ $O_1 \sim O_4$	Output port
$IO_1 \sim IO_4$	Tri-state bidirectional port
IOE	Output terminal When $IO_1 \sim IO_4$ is accessed, input completion signal (when read) or load signal (when written) is output from IOE terminal.

FUNCTIONAL DESCRIPTION

A block diagram of the MSM6352 is given on page 149. Each block of logic will be briefly discussed. For more information, please refer to the MSM6352 user's manual.

Program ROM

The MSM6352 will address up to 1 K words of internal mask programmable ROM. Each word consists of 14-bits and all instructions are one word. The instructions are routed to a programmed logic array which generales the signals necessary for control of logic.

Data RAM

Data is organized in 4-bit nibbles. Internal data RAM consists of 640 nibbles.

All locations are addressed by 10-bit address registers (AR_1, AR_2), 2-bit bank register (B), 4-bit page register (P) or a part of the instruction's operand.

Program Counter (PC)

The PC is an 11-bit counter to specify the ROM's address. The PC is normally incremented by one by every execution of the instruction, and then specifies the next instruction to be executed. However, Jump, Conditional branch, and Subroutine instructions are exceptions.

When the JMP adrs or CALL adrs instruction is executed, all of the PC contents are rewritten, so jump can be done to any address of the ROM.

Bank Register (B)

The bank register is a 2 bits register which specifies the bank of the RAM. Read/Write operation is performed by the Input/Output instruction.

Page Register (P)

The page register is a 4 bits register which specifies the page of the RAM. Read/Write operation is performed by the Input/Output instruction.

Address Register 1 (AR_1)

The address register AR_1 is a 10 bits register which specifies the RAM's address. This register is used by the RDAR instruction or the MVAR instruction. Read/Write operation is performed by the Input/Output instruction.

Address Register 2 (AR_2)

The address register AR_2 is a 10 bits register which specifies the RAM's address. This register is used by the MVAR instruction. Read/Write operation is performed by the Input/Output instruction.

Loop Counter (L)

The loop counter is a 10 bits down counter which specifies a number of words of the data to be searched or to be moved by the RDAR instruction or the MVAR instruction. Its contents can be rewritten by the output instruction.

ALU, Conditional Flag, ACC

(a) ALU

The ALU performs 4-bits parallel operation of the RAM contents and ACC contents, or the RAM contents and an immediate data. The arithmetic, logic, comparison and rotate operations can be done.

(b) Conditional flag

The zero flag (Z), carry flag (C) and greater flag (G) are provided. These flags are set or reset depending on the operation result and referred to by the conditional branch instruction.

The flag operation instruction enables these flags to be set or reset individually or allogether.

(c) ACC

The ACC is 4-bits register for arithmetic, and equipped with data transfer instruction between ACC and RAM.

Stack

The stack consists of a RAM of 5 words x 11 bits. It is used to save the PC contents when the sub-routine is called or a timer interrupt is generated, and 5-level nesting can be done including a timer interrupt. The PC contents saved in the stack is popped to the PC by the RETURN instruction.

Interrupt

MSM6352 has two kinds of interrupt as below.

- Realtime interrupt
- Programmabletimer interrupt

Stop Mode

Stop mode is established by the execution of the STOP instruction. In the stop mode, oscillation of system clock stops and all operations are suspended, but the RAM contents and all register contents are maintained.

Halt Mode

Halt mode is established by the execution of the HALT instruction and the execution of program of main routine is suspended. In the halt mode, all RAM contents and register contents are maintained.

Timer Activation and Realtime Interrupt Circuit

The timer activation and realtime interrupt circuit are to release HALT mode (timer activiation) and to generate interrupt (Realtime interrupt) at the talling edge of the 31.21 Hz clock obtained by dividing the 3.579545 MHz system clock by 114688. The timer activation and realtime interrupt circuit can be used for the generation of timer activation and realtime interrupt by setting or resetting the mode setting flag (TMF).

Divider Circuit

The 3 stage binary divider circuit to which 31.21 Hz clock is supplied is provided. The divider circuit's contents can be read by the input instruction (IN2, AP), and at the same time HS input port data is also read. The divider circuit can be reset by the RST instruction.

Programmable Timer and Programmable Timer Interrupt

The programmable timer is used for dial pulse output or timer interrupt generation. This timer consists of control resistor PTL, 1/100 divider circuit, 4 bit presettable down counter PTC, interrupt flag IRQF, interrupt enable flag EIF, selection flag EOF of off and on-hook dialing made, and dial pulse phase selection flag DPE, 1/100 divider circuit, PTC, IRQF, EIF, EOF and DPF are reset at system reset.

DTMF Output Circuit

The DTMF output circuit is to generate DTMF tone signal and is controlled by DTMF and TONE register. Rewriting the contents of the output latch for DTMF circuit by output instructions, 12 kinds of dual or single tones can be output to the DTMF output port. The tone output frequency is selected by the DTMF register.

BD Circuit

The BD circuit generates the square wave which can be used as the confirmation sound, warning sound and so on. 15 kinds of sound (4.66 to 0.82 kHz) are output by an output instruction specifying the frequency.

Watchdog Timer WDT

The watchdog timer is to generate the system reset signal to recover from system ran away trouble.

Input Port ($R_1 \sim R_4$)

$R_1 \sim R_4$ is 4-bits input port, which status is fetched by the input instruction. The port is pulled down to the low level (V_{SS}) by resistor, so it can be used as keyboard input port.

Input ($R_5 \sim R_8$)

$R_5 \sim R_8$ is 4-bits input port, which status is fetched by the input instruction. The port is pulled down to the low level (V_{SS}) by resistor, so it can be used as keyboard input port.

Input Port ($I_1 \sim I_4$)

$I_1 \sim I_4$ is 4-bits input port, which status can be fetched by the input instruction. It is pulled down to low level (V_{SS}) by register via transistor only when it is desired to fetch the port status or input signal is low level.

As input current is restricted, it can be used being fixed at high level (V_{DD}).

$\overline{HS}$ Input Pin

It is one bit input pin, which status can be fetched by the input instruction. It is pulled up to high level (V_{DD}) by resistor. It is used as a hook switch input pin.

Output Port ($C_1 \sim C_4$)

$C_1 \sim C_4$ is 4-bits output port. The contents of the output latch can be rewritten by the output instruction. The low level is output at each output pin after the system is reset. When the HS input pin is open or at high level, the low level is output to each output pin irrespective of the contents of the output latch.

The outputs of $C_1 \sim C_4$ are all CMOS output.

Output Port ($O_1 \sim O_4$)

$O_1 \sim O_4$ is 4-bit output port. The contents of the output latch can be rewritten by the output instruction.

Output latch of O_1 and O_2 are reset and O_3 and O_4 are set at system reset.

Each output from $O_1 \sim O_4$ port is C-MOS.

Output Port $EO_1 \sim EO_4$)

$EO_1 \sim EO_4$ is 4-bits output port. The contents of the output latch can be rewritten by the output instruction. The level is output at each output pin after the system is reset. Each output of $EO_1 \sim EO_4$ is CMOS output.

Input/Output Port ($IO_1 \sim IO_4$)

$IO_1 \sim IO_4$ is 4-bits input/output port. Fetching of the port status and rewriting of the output latch contents can be done by the input/output instruction.

Each Output of $IO_1 \sim IO_4$ is CMOS at output mode.

IOE Output Pin

It is one bit output pin. A load signal is output at this pin when the output latch's ($IO_1 \sim IO_4$) contents are rewritten.

DTMF Output Pin

It is output pin to output DTMF signals. Start and stop of the DTMF output are done by the output instruction.

DP Output Pin

It is an output pin for dial pulse output. Start and top of the dial pulse output can be done by the output instruction.

The DP OUT pin output is C-MOS output.

BD Output Pin

It is output pin for the buzzer output. The buzzer output can be started and stopped by the output instruction. Output of BD port is CMOS output.

32 kHz Output Pin

It is an output pin to output 31.960 kHz clock (duty: 50%) which is obtained by dividing the 3.579545 MHz system clock by 112. This clock keep outputting as long as system clock oscilation is executed. Output of 32 kHz pin is CMOS out-out.

XT, $\overline{XT}$ Pins

These are input and output pins of the oscillator inverter, and the oscillator circuit is provided with the built in feed back resistor. By connecting to them oscillation of system clock status. 3.579545 MHz ceramic resonator and capacitors.

ELECTRIC CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−30 ~ 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_O	Ta = 25°C	−0.3 ~ V_{DD} + 0.3	V
Power Dissipation	P_D	Ta = 25°C	200 max.	mW
Storage Temperature	Tstg	—	−55 ~ +125	°C

• Operating Conditions

Parameter	Symbol	Conditions	Limits	Unit
Operating Voltage	V_{DD}	Pulse Mode f_{OSC} = 3.58 MHz	2.0 ~ 5.5	V
Memory Retension Voltage	V_{DDM}	—	1.2 ~ 5.5	V
Operating Temperature	Topr	—	−20 ~ +75	°C

Note: Operating conditions for tone mode is V_{DD} = 2.2 ~ 5.5V.

• DC Characteristics

(Ta = −20 ~ +75°C)

Parameter	Symbol	Conditions		Supply Voltage	Min.	Typ.	Max.	Unit	Survey Circuit
"H" Output Current (1)	I_{OH_1}	O_3, O_4 DP OUT	V_{OH} = 2.6V	3.0 V	−0.2	–	–	mA	1
"L" Output Current (1)	I_{OL_1}		V_{OL} = 0.4V	3.0V	0.5	–	–	mA	
"H" Output Current (2)	I_{OH_2}	$C_1 \sim C_4$	V_{OH} = 2.6V	3.0V	−1.0	–	–	mA	
"L" Output Current (2)	I_{OL_2}		V_{OL} = 0.4V	3.0V	10	–	–	μA	
"H" Output Current (3)	I_{OH_3}	O_1, O_2 BD	V_{OH} = 2.6V	3.0V	−2.0	–	–	μA	
"L" Output Current (3)	I_{OL_3}		V_{OL} = 0.4V	3.0V	10	–	–	μA	
"H" Output Current (4)	I_{OH_4}	$IO_1 \sim IO_4$ IOE $EO_1 \sim EO_4$	V_{OH} = 2.6V	3.0V	−150	–	–	μA	
"L" Output Current (4)	I_{OL_4}		V_{OL} = 0.4V	3.0V	300	–	–	μA	
"H" Output Current (5)	I_{OH_5}	32kHz	V_{OH} = 2.6V	3.0V	−40	–	–	μA	
"L" Output Current (5)	I_{OL_5}		V_{OL} = 0.4V	3.0V	25	–	–	μA	
"H" Input Voltage	V_{IH}	–		3.0V	2.2	–	–	V	2
				5.5V	40	–	–		
"L" Input Voltage	V_{IL}	–		3.0V	–	–	0.8	V	
				5.5V	–	–	1.4		
"H" Input Current (1)	I_{IH_1}	HS	V_{IH} = 5.5V	5.5V	–	–	2	μA	3
"L" Input Current (1)	I_{IL_1}		V_{IL} = 0V	3.0V	−2.0	–	−180	μA	
				5.5V	−40	–	−360		
"H" Input Current (2)	I_{IH_2}	$R_1 \sim R_3$	V_{IH} = 5.5V	5.5V	20	–	180	μA	
			V_{IH} = 3.0V	3.0V	10	–	90		
"L" Input Current (2)	I_{IL_2}		V_{IL} = 0V	5.5V	–	–	−2	μA	
"H" Input Current (3)	I_{IH_3}	$I_1 \sim I_4$ AC, TEST	V_{IH} = 5.5V	5.5V	60	–	600	μA	
			V_{IH} = 3.0V	3.0V	30	–	300		
"L" Input Current (3)	I_{IL_3}		V_{IL} = 0V	5.5V	–	–	−2	μA	
"H" Input Current (4)	I_{IH_4}	$IO_1 \sim IO_4$	V_{IH} = 5.5V	5.5V	–	–	2	μA	
"L" Input Current (4)	I_{IL_4}		V_{IL} = 0V	5.5V	–	–	−2	μA	
Current Consumption (1)	I_{DDP}	Tone output off With no load		2.5V	–	0.25	0.5	mA	4
				5.0V	–	1.5	2.4		
Current Consumption (2)	I_{DDT}	Tone output on With on load		2.5V	–	1.3	2.4	mA	
				5.0V	–	4.2	6.8		
Current Consumption (3)	I_{DDM}	ON HOOK, Ta = 25°C With no load		2.5V	–	–	0.2	μA	

• AC Characteristics

(Ta = –20 ~ +75°C)

Parameter	Symbol	Conditions	Supply Voltage	Min.	Typ.	Max.	Unit	Survey Circuit
Cycle Time	t_{CY}	f = 3.579545MHz	3.0V	–	17.9	–	μs	
Tone Output	V_{OUT}	Row side only R_L = 1kΩ	2.2V	–	180	–	mV rms	
			4.0V	–	260	–		
			5.5V	–	330	–		
High/Low Level Ratio	dB_{CR}	–	3.0V	1	2	3	dB	
			5.5V	1	2	3		
Distorsion Ratio	$\%d_{IS}$	R_L = 1kΩ	3.0V	–	–	5	%	
			5.5V	–	–	5		
Switch Input Time	t_{KIN}		–	3.3	–	–	ms	5
Rise/Fall Time (1)	t_{TLH_1}	Q_3, Q_4, DP OUT C_L = 50pF	3.0V	–	–	0.5	μs	
	t_{THL_1}		3.0V	–	–	0.5		
Rise/Fall Time (2)	t_{TLH_2}	$C_1 \sim C_4$ C_L = 50pF	3.0V	–	–	0.5	μs	
	t_{THL_2}		3.0V	–	–	10		
Rise/Fall Time (3)	t_{TLH_3}	Q_1, Q_2, BD, 32kHz C_L = 50pF	3.0V	–	–	5	μs	
	t_{THL_3}		3.0V	–	–	10		
Rise/Fall Time (4)	t_{TLH_4}	$IO_1 \sim IO_4$, IOE $EO_1 \sim EO_4$ C_L = 50pF	3.0V	–	–	1	μs	
	t_{THL_4}		3.0V	–	–	1		

• DTMF Tone Output Freqeuncy

	Standard Frequency (Hz)	Output Freqeuncy (Hz)	Deviation (%)
R1	697	699.1	+0.30
R2	770	766.2	–0.49
R3	852	847.4	–0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	–0.32
C3	1477	1471.9	–0.35

f_{OSC} = 3.579545MHz

	Mnemonic	Instruction Code															ACC	Zero	Carry	Greater	Description
		13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Arithmetic operation	ADD ACC, AP	0	0	0	0	0	P	0	1	0	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP) + ACC
	ADD #D, AP	0	1	1	0	0	P	D				A				$D=0_H\sim F_H$ $A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP) + D
	ADC AP	0	0	0	0	0	P	0	1	0	1	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP) + ACC + C
	SUB ACC, AP	0	0	0	0	1	P	0	1	0	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP)– ACC
	SUB #D, AP	0	1	1	0	1	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP) – D
	SBC AP	0	0	0	0	1	P	0	1	0	1	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	AP ← (AP) – ACC – C
	CMP ACC, AP	0	0	0	0	1	P	1	1	1	0	A				$A=0_H\sim F_H$, P=0 or 1	–	•	–	•	(AP) – ACC
	CMP #D, AP	0	1	0	1	1	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, P=0 or 1	–	•	–	•	(AP) – D
	XOR ACC, AP	0	0	0	0	0	P	0	1	1	1	A				$A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∀ ACC
	XOR #D, AP	0	1	1	1	1	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∀ D
Bit operation	BIT ACC, AP	0	0	0	0	0	P	1	1	1	0	A				$A=0_H\sim F_H$, P=0 or 1	–	•	–	–	(AP) ∨ $\overline{ACC}$
	BIT #D, AP	0	1	0	1	0	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, p=0 or 1	–	•	–	–	(AP) ∨ $\overline{D}$
	BIS ACC, AP	0	0	0	0	0	P	1	1	1	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∨ ACC
	BIS #D, AP	0	1	0	0	0	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∨ D
	BIC ACC; AP	0	0	0	0	1	P	0	1	1	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∧ $\overline{ACC}$
	BIC #D, AP	0	1	0	0	1	P	D				A				$D=0_H\sim F_H$, $A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← (AP) ∧ $\overline{D}$
Rotate	ROR AP	0	0	0	0	0	P	0	0	1	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	⌊ (AP) → C ⌋
	ROL AP	0	0	0	0	1	P	0	0	1	0	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	⌊ (AP) ← C ⌋
	ASR AP	0	0	0	0	0	P	0	0	1	1	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	0 → (AP) → C
	ASL AP	0	0	0	0	1	P	0	0	1	1	A				$A=0_H\sim F_H$, P=0 or 1	•	•	•	–	C ← (AP) ← 0
Flag operation	SEZ	0	0	0	0	1	0	1	0	1	0	0	0	0	0		–	1	–	–	Z ← 1
	CLZ	0	0	0	0	0	0	1	0	1	0	0	0	0	0		–	0	–	–	Z ← 0
	SEC	0	0	0	0	1	0	1	0	0	1	0	0	0	0		–	–	1	–	C ← 1
	CLC	0	0	0	0	0	0	1	0	0	1	0	0	0	0		–	–	0	–	C ← 0
	SEG	0	0	0	0	1	0	1	0	0	0	0	0	0	0		–	–	–	1	G ← 1
	CLG	0	0	0	0	0	0	1	0	0	0	0	0	0	0		–	–	–	0	G ← 0
	SEA	0	0	0	0	1	0	1	0	1	1	0	0	0	0		–	1	1	1	Z ← 1, C ← 1, G ← 1
	CLA	0	0	0	0	0	0	1	0	1	1	0	0	0	0		–	0	0	0	Z ← 0, C ← 0, G ← 0
Data transfer	MOV ACC, AP	1	1	1	1	0	1	0	0	0	0	A				$A=0_H\sim F_H$	–	–	–	–	AP ← ACC
	MOV ACC, AX	1	1	1	1	0	0	X				A				$X=0_H\sim F_H$ $A=0_H\sim F_H$	–	–	–	–	AX ← ACC
	MOV #D, AP	0	1	1	1	0	P	D				A				$D=0_H\sim F_H$ $A=0_H\sim F_H$, P=0 or 1	•	•	–	–	AP ← D
	MOV AP, ACC	1	1	1	1	1	1	0	0	0	0	A				$A=0_H\sim F_H$	•	•	–	–	ACC ← (AP)
	MOV AX, ACC	1	1	1	1	1	0	X				A				$X=0_H\sim F_H$ $A=0_H\sim F_H$	•	•	–	–	ACC ← (AX)
	CHG AP	1	1	1	0	0	1	0	0	0	0	A				$A=0_H\sim F_H$	•	–	–	–	(AP) ↔ ACC
	CHG AX	1	1	1	0	0	0	X				A				$X=0_H\sim F_H$ $A=0_H\sim F_H$	•	–	–	–	(AX) ↔ ACC

	Mnemonic	Instruction Code																ACC	Zero	Carry	Greater	Description
		13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Data transfer	RDAR	1	1	0	0	0	0	0	0	0	0	0	0	0	0			*	*	–	–	ACC ← (AR$_1$)
	RDAR +(–)	1	1	0	0	0	0	0	0	1	D/I	0	0	0	0	D/I = 0 or 1		*	*	–	–	ACC ← (AR$_1$), AR$_1$ ← AR$_1$ ±1
	RDAR +(–), Z	1	1	0	0	0	0	0	1	0	D/I	0	0	0	0	D/I = 0 or 1		0	1	–	–	ACC ← (AR$_1$) if (AR$_1$)=0 then PC ← PC+1 else AR$_1$ ← AR$_1$ ±1, repeat
	RDAR +(–), N	1	1	0	0	0	0	1	0	0	D/I	0	0	0	0	D/I = 0 or 1		*	0	–	–	ACC ← (AR$_1$) if (AR$_1$)=0 then PC ← PC+1 else AR$_1$ ← AR$_1$ ±1, repeat
	RDAR +(–),Z,L	1	1	0	0	1	0	0	1	0	D/I	0	0	0	0	D/I = 0 or 1		*	*	–	–	ACC ← (AR$_1$), L ← L–1 if (AR$_1$)=0 or L=0 then PC ← PC+1 else AR$_1$ ← AR$_1$ ±1, repeat
	RDAR +(–),N,L	1	1	0	0	1	0	1	0	0	D/I	0	0	0	0	D/I = 0 or 1		*	*	–	–	ACC ← (AR$_1$), L ← L–1 if (AR$_1$)=0 or L=0 then PC ← PC+1 else AR$_1$ ← AR$_1$ ±1, repeat
	MVAR	1	1	0	1	0	0	0	0	0	0	0	0	0	0			–	*	–	–	(AR$_2$) ← (AR$_1$)
	MVAR +(–)	1	1	0	1	0	0	0	0	1	D/I	0	0	0	0	D/I = 0 or 1		–	*	–	–	(AR$_2$) ← (AR$_1$), AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1
	MVAR +(–), Z	1	1	0	1	0	0	0	1	0	D/I	0	0	0	0	D/I = 0 or 1		–	1	–	–	(AR$_2$) ← (AR$_1$) if (AR$_1$)=0 then PC ← PC+1 else AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1, repeat
	MVAR +(–), N	1	1	0	1	0	0	1	0	0	D/I	0	0	0	0	D/I = 0 or 1		–	0	–	–	(AR$_2$) ← (AR$_1$) if (AR$_1$)=0 then PC ← PC+1 else AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1, repeat
	MVAR +(–), L	1	1	0	1	1	0	0	0	0	D/I	0	0	0	0	D/I = 0 or 1		–	*	–	–	(AR$_2$) ← (AR$_1$), L ← L–1 if L=0 then PC ← PC+1 else AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1, repeat
	MVAR +(–),Z,L	1	1	0	1	1	0	0	1	0	D/I	0	0	0	0	D/I = 0 or 1		–	*	–	–	(AR$_2$) ← (AR$_1$), L ← L–1 if (AR$_1$)=0 or L=0 then PC ← PC+1 else AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1, repeat
	MVAR +(–),N,L	1	1	0	1	1	0	1	0	0	D/I	0	0	0	0	D/I = 0 or 1		–	*	–	–	(AR$_2$) ← (AR$_1$), L ← L–1 if (AR$_1$)=0 or L=0 then PC ← PC+1 else AR$_1$←AR$_1$ ±1, AR$_2$←AR$_2$ ±1, repeat
Subroutine	CALL adrs	1	0	1	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	a_{10}~a_0=000$_H$~7FF$_H$		–	–	–	–	STACK ← (PC), PC ← adrs
	RET	0	0	0	0	0	0	1	1	0	0	0	0	0	0			–	–	–	–	PC ← (STACK) + 1
	RTI	0	0	0	0	1	0	1	1	0	0	0	0	0	0			–	–	–	–	PC ← (STACK) or PC ← (STACK) + 1
Jump	JMP adrs	1	0	0	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	a_{10}~a_0=000$_H$~7FF$_H$		–	–	–	–	PC ← adrs
	JMP @ AP	0	0	0	0	0	P	1	1	0	1	A				A=0$_H$~F$_H$, P=0 or 1		–	–	–	–	PC ← (PC) + (AP) + 1
	JMPIO @ AP	0	0	0	0	1	P	1	1	0	1	A				A=0$_H$~F$_H$, P=0 or 1		–	–	–	–	PC ← (PC) + [(AP) A 7] + 1
Branch	BEQ n (BZE n)	1	1	1	0	1	P	0	1	0	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if Z=1 then PC←PC–n or PC←PC+n+1 else PC←PC+1
	BNE n (BNZ n)	1	1	1	0	1	P	1	1	0	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if Z=0 then PC←PC–n or PC←PC+n+1 else PC←PC+1
	BCS n	1	1	1	0	1	P	0	0	0	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if C=1 then PC←PC–n or PC←PC+n+1 else PC←PC+1
	BCC n	1	1	1	0	1	P	1	0	0	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if C=0 then PC←PC–n or PC←PC+n+1 else PC←PC+1
	BGT n	1	1	1	0	1	P	0	0	1	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if G=1 then PC←PC–n or PC←PC+n+1 else PC←PC+1
	BLE n	1	1	1	0	1	P	1	0	1	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if G=0 then pC←PC–n or PC←PC+n+1 else PC←PC+1
	BGE n	1	1	1	0	1	P	0	1	1	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if Z=1 or G=1 then PC←PC–n or PC+n+1 else PC←PC+1
	BLT n	1	1	1	0	1	P	1	1	1	n_4	n_3	n_2	n_1	n_0	n_4~n_0=00$_H$~1F$_H$ P=0 or 1		–	–	–	–	if Z=0 then PC←PC–n or PC←PC+n+1 and G=0 else PC←PC+1
Input/Output	IN PORT, AP	0	0	0	1	0	P	P_L				A				P_L=0$_H$~F$_H$ A=0$_H$~F$_H$, P=0 or 1		*	*	–	–	AP ← (PORT)
	OUT AP, PORT	0	0	1	0	P_H	P	P_L				A				P_L=0$_H$~F$_H$, P_H=0 or 1 A=0$_H$~F$_H$, P=0 or 1		–	–	–	–	PORT ← (AP)
	OUT #D, PORT	0	0	1	1	P_H	0	P_L				D				P_L=0$_H$~F$_H$, P_H=0 or 1 D=0$_H$~F$_H$		–	–	–	–	PORT ← D

	Mnemonic	Instruction Code														ACC	Zero	Carry	Greater	Description
		13	12	11	10	9	8	7	6	5	4	3	2	1	0					
CPU Control & Others	STOP	0	0	1	1	1	0	0	0	0	0	0	0	0	0	–	–	–	–	Stop system clock
	HALT	0	0	1	1	1	0	0	0	0	1	0	0	0	0	–	–	–	–	Halt CPU
	ACT	0	0	1	1	1	0	0	0	1	0	0	0	0	0	–	–	–	–	Activate CPU
	EI	0	0	1	1	1	0	0	1	1	0	1	0	0	0	–	–	–	–	Enable timer interrupt
	DI	0	0	1	1	1	0	0	1	1	0	0	1	0	0	–	–	–	–	Disable timer interrupt
	ET	0	0	1	1	1	0	0	1	1	0	0	0	1	0	–	–	–	–	Enable timer activate
	DT	0	0	1	1	1	0	0	1	1	0	0	0	0	1	–	–	–	–	Disable timer activate
	EC	0	0	1	1	1	0	0	1	1	1	1	0	0	0	–	–	–	–	Enable output port ($C_1 \sim C_4$)
	DC	0	0	1	1	1	0	0	1	1	1	0	1	0	0	–	–	–	–	Disable output port ($C_1 \sim C_4$)
	OM	0	0	1	1	1	0	0	1	1	1	0	0	1	0	–	–	–	–	Set I/O port ($IO_1 \sim IO_4$) to output mode
	IM	0	0	1	1	1	0	0	1	1	1	0	0	0	1	–	–	–	–	Set I/O port ($IO_1 \sim IO_4$) to input mode
	RST	0	0	1	1	1	0	1	0	0	1	0	0	0	0	–	–	–	–	Reset divider
	SELINT	0	0	1	1	1	0	1	1	0	0	1	0	0	0	–	–	–	–	Select interrupt mode
	SELHR	0	0	1	1	1	0	1	1	0	0	0	1	0	0	–	–	–	–	Select timer activation mode
	EHLH	0	0	1	1	1	0	1	1	0	0	0	0	1	0	–	–	–	–	Enable hook switch low to high transmission
	DHLH	0	0	1	1	1	0	1	1	0	0	0	0	0	1	–	–	–	–	Disable hook switch low to high transmission
	SELN	0	0	1	1	1	0	1	0	1	1	0	0	1	0	–	–	–	–	Select negative phase
	SELP	0	0	1	1	1	0	1	0	1	1	0	0	0	1	–	–	–	–	Select positive phase
	EO	0	0	1	1	1	0	1	0	1	1	1	0	0	0	–	–	–	–	Enable on-hook dial
	DO	0	0	1	1	1	0	1	0	1	1	0	1	0	0	–	–	–	–	Disable on-hook dial
	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–	–	–	–	No operation