OKI semiconductor

MSM6411

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

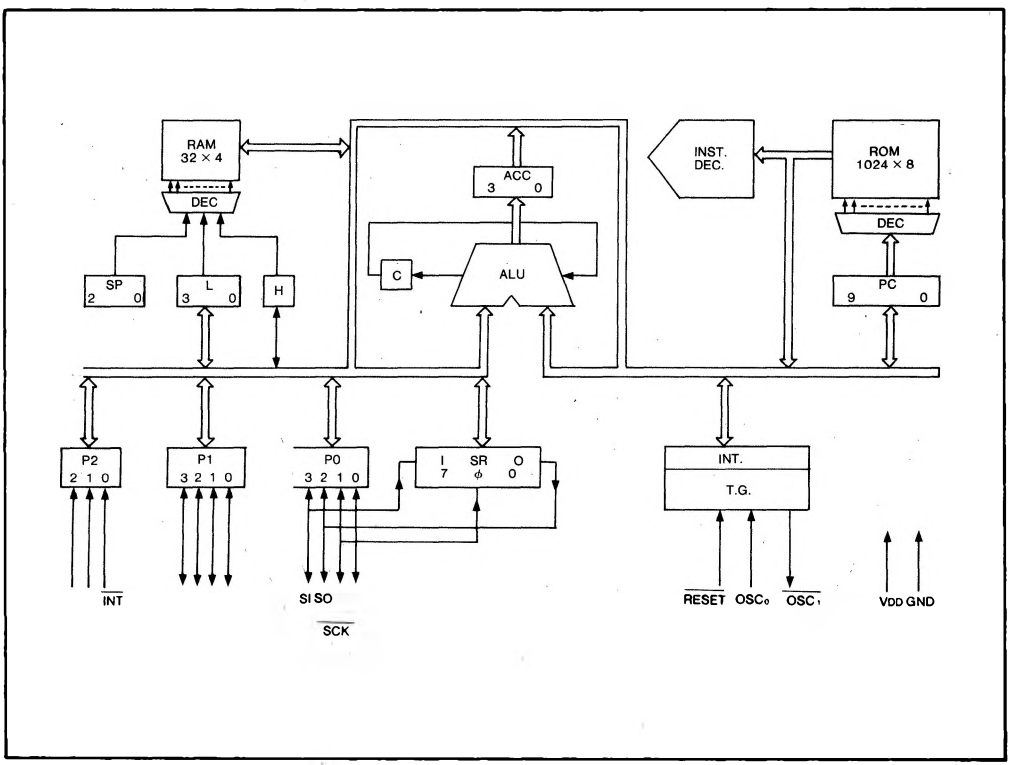
GENERAL DESCRIPTION

The OKI MSM6411 microcontroller is a low-power, high-performance single-chip device implemented in complementary metal oxide semiconductor technology. 1024 × 8 bits of program ROM, 32 × 4 bits of data RAM, 11 Input/Output lines and oscillator. Program memory is byte wide and data paths are organized as 4-bit wide. 63 instructions include binary, logical operations; bit set, reset, test; multifunctional.

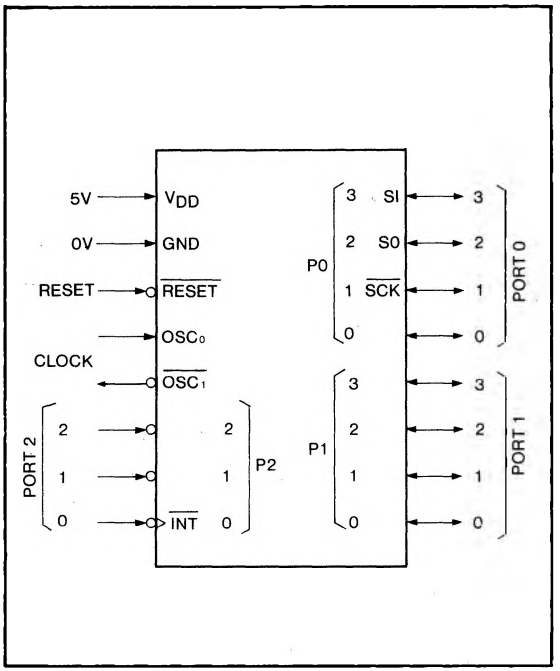
FEATURES

- 1024 × 8 Internal ROM
- 32 × 4 Internal RAM
- 11 I/O Lines (8 I/O Lines, 3 Input Lines)
- 8-bit serial I/O Register
- 2 Interrupt Levels
- 8 Stack Levels
- 952 ns 4.2MHz (V_{DD} 5V±10%)
- 63 Instructions
- Self-Contained Oscillator
- −40 to +85°C Operating Temperature
- 3 to 6V Operating V_{DD}
- Low Power Consumption 5 μW Typical (STOP, V_{DD} = 5V, no load)
- Mask Option Crystal/Ceramic Oscillator

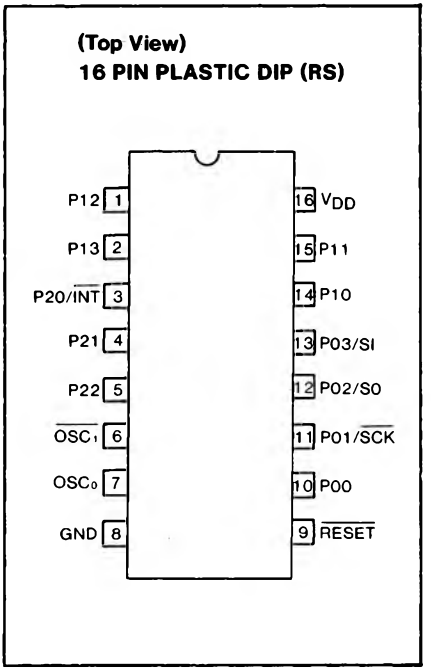
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



PIN CONFIGURATION



PIN DESCRIPTION

Designation	Input/Output	Pin No.	Function	Reset
P00 P01/$\overline{SCK}$ P02/SO P03/SI	Input/Output	10 11 12 13	4 Bits I/O port. P01 to P03 are used both I/O port and terminal of shift resister	"1"
P10 P11 P12 P13	Input/Output	14 15 1 2	4 Bits I/O port	"1"
P20/$\overline{INT}$ P21 P22	Input	3 4 5	3 Bits input port with latch. P20 is used as both input port and input terminal of INT (input of falling edge trigger).	Latch is reset. ("0")
OSC_0	Input	7	Input terminal of system clock. Oscillation circuit consists of OSC_0 and $\overline{OSC_1}$.	Clock pulse In
$\overline{OSC_1}$	Output	6	Oscillation circuit consists of OSC_0 and $\overline{OSC_1}$.	
$\overline{RESET}$	Input	9	Input terminal of system reset	
V_{DD} GND	Input	16 8	Main power source and circuit GND potential.	

FUNCTIONAL DESCRIPTION

ROM

ROM is organized in 1024 words by 8 bits. It is used to stored developed application programs (instructions). It is addressed by the program counter (PC).

PC

The PC consists of a 10-bit binary counter and is used to address ROM.

Stack and Stack Pointer

An interrupt or CAL instruction causes the contents of the PC to be saved in the stack. The PC is restored from the stack by RT instruction.

All RAM locations (up to 8 levels) are available as the stack. Note that four words of RAM are used for each level.

The stack pointer is a 5-bit up-down counter that points to the address of the next stack to be used. It allows the RAM locations to be used as a push-down stack.

RAM

RAM consists of up to 32 words 4 bits wide. It is addressed by the H- and L-registers or by the contents of the second byte of an instruction.

L-REGISTER

A 4-bit register which specifies RAM locations A3-A0.

H-REGISTER

A 1-bit register which specifies RAM location A4.

ALU

A 4-bit logic circuit that provides arithmetic and logical operations.

ACC

Consisting of a 4-bit register, the accumulator holds the result of operations or the data present on ports.

C FLAG

The flag that holds a carry generated from the result of operations.

INPUT/OUTPUT Ports (2 × 4 bit)

Organized into 4 bits, 2 ports are provided for effecting and controlling data transfer to and from an external source. The ports are selected by codes included in instructions.

Input Ports (1 × 4 bit)

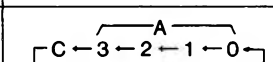
Contained port 2 (P2), which is an input port with latching function. P20 is set at falling edge of the input signal P21 and P22 are set at "0" level inputs. Also, P20 is used as an interrupt request flag. When P20 is set and an interrupt operation occurs, it is automatically reset.

TIMING CONTROL (TC)

A 0 level on the $\overline{\text{RESET}}$ pin for longer than 2 machine cycles initializes the internal circuitry.

Clock pulses are supplied to the XT pin from an external source. Also, by mask-option, it organizes a circuit of oscillation with P20 and produces clock pulses (by connecting externally to crystal, ceramic or CR).

INSTRUCTION LIST

	Mnemonic		Description	Code	Byte	Cycle
Load, Push, Pop	LAI	n	A ← n	90 – 9F	1	1
	LLI	n	L ← n	80 – 8F	1	1
	LHLI	nn	HL ← nn	15nn	2	2
	LAL		A ← L	21	1	1
	LLA		L ← A	2D	1	1
	LAM		A ← M	38	1	1
	LMA		M ← A	2F	1	1
	LAMD	mm	A ← Md	10mm	2	2
	LMAD	mm	Md ← A	11mm	2	2
	LMSR		M(w) ← SR	3E5A	2	2
	LSRM		SR ← M(w)	3E52	2	2
	PUSH		ST ← C, A, H, L, SP ← SP−1	1C	1	3
	POP		C, A, H, L ← ST, SP ← SP+1	1D	1	3
Input Output	IPD	p	A ← Pp	3DpD	2	2
	OPD	p	Pp ← A	3DpC	2	2
Arithmetic	ADS		A ← A+M, SKIP IF Cy = "1"	02	1	1
	ADC		C, A ← C+A+M	03	1	1
	AIS	n	A ← A+n, SKIP IF Cy = "1"	3E4n	2	2
	DAS		A ← A+10	0A	1	1
	AND		A ← A ∧ M	0D	1	1
	EOR		A ← A ∀ M	04	1	1
	CMA		A ← $\overline{A}$	0B	1	1
	CAM		SKIP IF A = M	16	1	1
	SC		C ← "1"	07	1	1
	RC		C ← "0"	08	1	1
	TC		SKIP IF C = "1"	09	1	1
	RAL			0E	1	1
Ex-change	X		A ⟷ M	28	1	1
Increment/ Decrement	INL		L ← L+1, SKIP IF L = "0"	31	1	1
	INH		H ← H+1, SKIP IF H = "0"	32	1	1
	INM		M ← M+1, SKIP IF M = "0"	33	1	1

INSTRUCTION LIST (CONT.)

	Mnemonic		Description	Code	Byte	Cycle
Increment/ Decrement	INMD	mm	Md ← Md+1, SKIP IF Md = "0"	12mm	2	2
	DCL		L ← L−1, SKIP IF L = "F"	35	1	1
	DCH		H ← H−1	36	1	1
	DCM		M ← M−1, SKIP IF M = "F"	37	1	1
Bit operation	TAB	n2	SKIP IF [A bit n2] = "1"	54−57	1	1
	TMB	n2	SKIP IF [M bit n2] = "1"	58-5B	1	1
	RMB	n2	[M bit n2] ← "0"	68−6B	1	1
	SMB	n2	[M bit n2] ← "1"	78−7B	1	1
	TPBD	p, n2	SKIP IF [Pp bit n2] = "1"	3D p0~3	2	2
	RPBD	p, n2	[Pp bit n2] ← "0"	3D p4~7	2	2
	SPBD	p, n2	[Pp bit n2] ← "1"	3D p8~B	2	2
Branch	JCP	a6	PC ← a6	C0~FF	1	1
	JP	a10	PC ← a10	40~43 00~FF	2	2
	CAL	a10	ST ← PC+2, PC ← a10, SP ← SP−1	A0~A3 00~FF	2	4
	RT		PC ← ST, SP ← SP+1	1E	1	4
Interrupt	MEI		MEIF ← "1"	3E60	2	2
	MDI		MEIF ← "0"	3E61	2	2
	EICT		EICTF ← "1"	3DCB	2	2
	EIEX		EIEXF ← "1"	3DC8	2	2
	DICT		EICTF ← "0"	3DC7	2	2
	DIEX		EIEXF ← "0"	3DC4	2	2
	TICT		SKIP IF EICTF = "1"	3DC3	2	2
	TIEX		SKIP IF EIEXF = "1"	3DC0	2	2
	TQEX		SKIP IF IRQEX = "1"	3D20	2	2
	TQSR		SKIP IF IRQSR = "1"	3DD3	2	2
	RQEX		IRQEX ← "0"	3D24	2	2
	RQSR		IRQSR ← "0"	3DD7	2	2
Shift resistor	ESR		SRF ← "1"	3DBA	2	2
	DSR		SRF ← "0"	3DB6	2	2
	TSR		SKIP IF SRF = "1"	3DB2	2	2
CPU control	STOP		STOP CLOCK	3DB9	2	2
	NOP		NO OPERATION	00	1	1

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Output Voltage	V_O		−0.3 ~ V_{DD}	V
Power Dissipation	P_D	Ta = 25°C per one package	200 max.	mW
		Ta = 25°C per one output	50 max.	mW
Storage Temperature	Tstg		−55 ~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage	V_{DD}	f(OSC) ≦ 1MHz	3 ~ 6	V
		f(OSC) ≦ 4.2MHz	4.5 ~ 5.5	V
Data-Hold Voltage	V_{DDH}	f(OSC) = 0Hz	2 ~ 6	V
Operating Temperature	T_{OP}	—	−40 ~ +85	°C
Fan Out	N	MOS Load	15	—
		TTL Load	1	

DC CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
"H" Input Voltage *1, *2	V_{IH}	———	2.4	–	V_{DD}	V
"H" Input Voltage *3, *4	V_{IH}	———	3.6	–	V_{DD}	V
"L" Input Voltage	V_{IL}	———	−0.3	–	0.8	V
"H" Output Voltage *1, *5	V_{OH}	I_O = −15μA	4.2	–	–	V
"L" Output Voltage *1	V_{OL}	I_O = 1.6mA	–	–	0.4	V
"L" Output Voltage *5	V_{OL}	I_O = 15μA	–	–	0.4	V
Input Current *3	I_{IH} / I_{IL}	$V_I = V_{DD}/0V$	–	–	15 / −15	μA
Input Current *2, *4	I_{IH} / I_{IL}	$V_I = V_{DD}/0V$	–	–	1 / −30	μA
"H" Output Current *1	I_{OH}	V_O = 2.4V	−0.1	–	–	mA
"H" Output Current *1	I_{OH}	V_O = 0.4V	–	–	−1.2	mA
Input Capacitance	C_I	f = 1MHz, Ta = 25°C	–	5	–	pF
Output Capacitance	C_O		–	7	–	
Power Consumption (STOP)	I_{DDS}	V_{DD} = 2V, no load Ta = 25°C	–	0.2	5	μA
		No load	–	1	100	μA
Power Consumption	I_{DD}	Crystal oscillation, No load, 4.2MHz	–	6	12	mA

*1 Applied to P0 and P1.

*2 Applied to P2.

*3 Applied to OSC_0

*4 Applied to $\overline{RESET}$

*5 Applied to $\overline{OSC_1}$

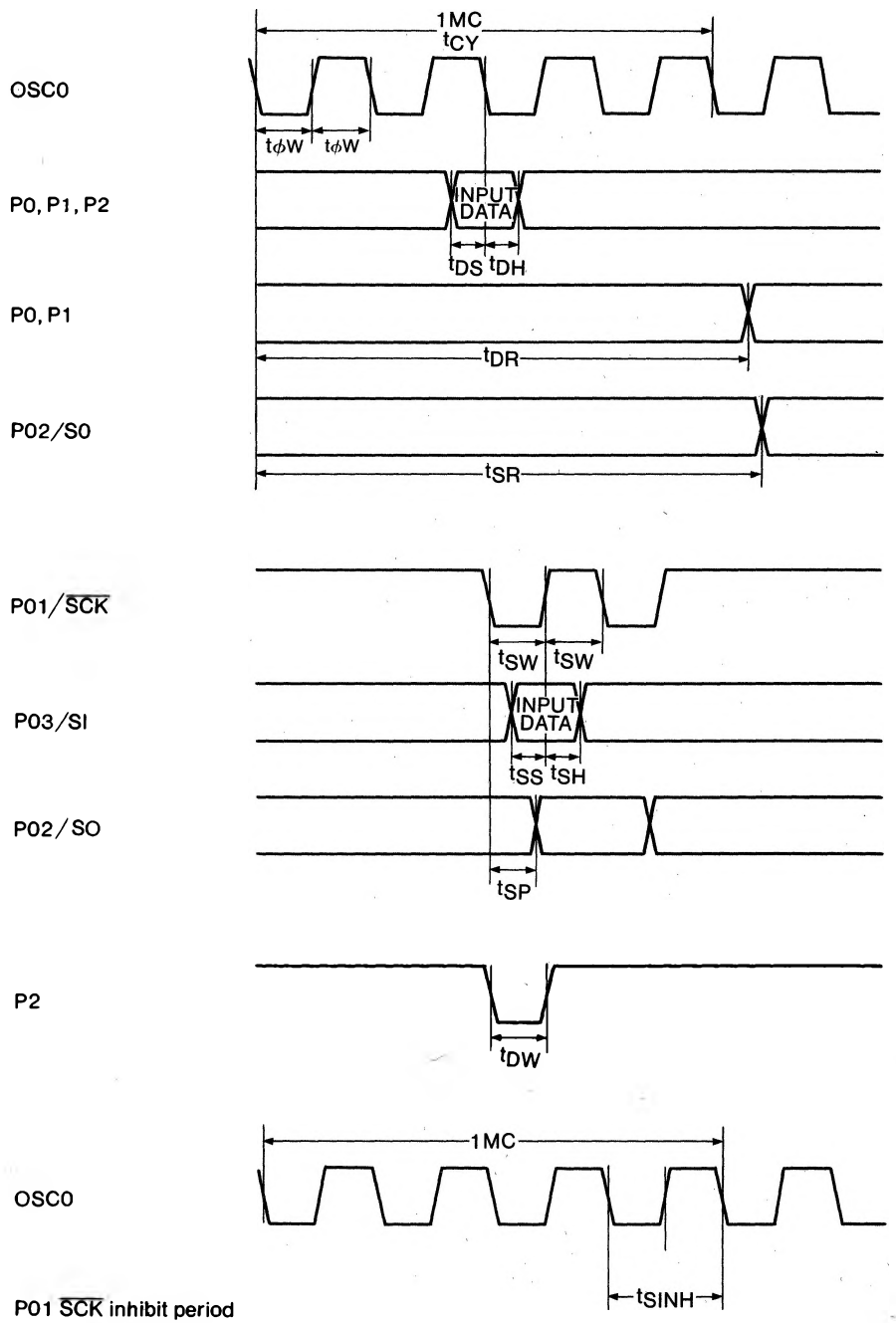
AC CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Clock (OSC_O) Pulse Width	$t_{\phi W}$	–	119	–	–	ns
Cycle Time	t_{CY}	–	952	–	–	ns
Input Data Setup Time	t_{DS}	–	120	–	–	ns
Input Data Hold Time	t_{DH}	–	120	–	–	ns
Input Data/Input Clock Pulse Width	t_{DW}	–	120	–	–	ns
SR Clock Pulse Width	t_{SW}	–	$t_{\phi W}$	–	–	ns
SR Data Setup Time	t_{SS}	–	120	–	–	ns
SR Data Hold Time	t_{SH}	–	120	–	–	ns
Data Delay Time	t_{DR}	C_L=15pF	–	–	t_{CY} +300	ns
SR Data Delay Time*	t_{SR}	C_L=15pF	–	–	t_{CY} +480	ns
SR Data Delay Time Using External Clock	t_{SP}	C_L=15pF	–	–	360	ns
SR Clock Invalid Time	t_{SINH}	–	2/8 t_{CY}	–	–	ns

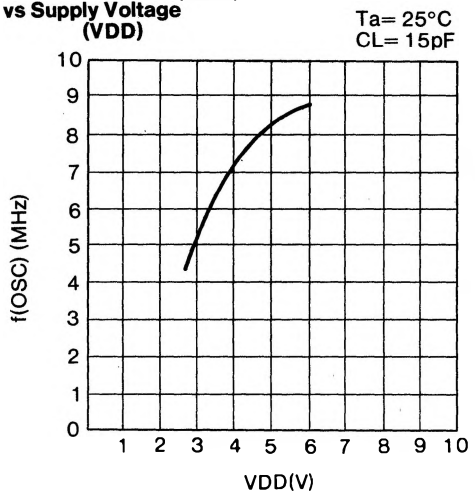
* When SR clock is oscillated by alternate output of "1" or "0" to P01.

TIMING CHART

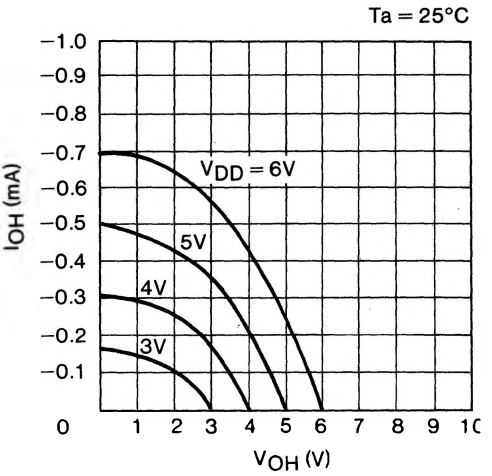


P01 $\overline{SCK}$ inhibit period during LMSR INST.

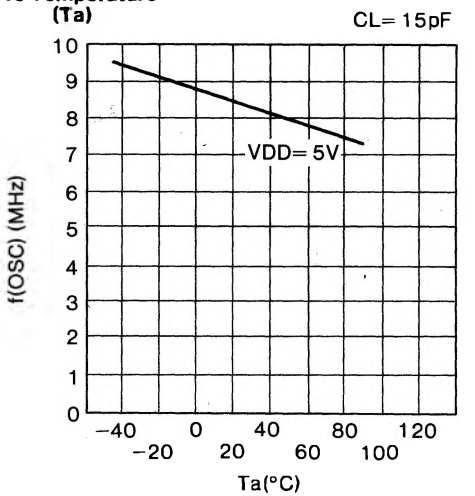
TYP. Maximum Oscillator Frequency f(OSC) vs Supply Voltage (VDD)



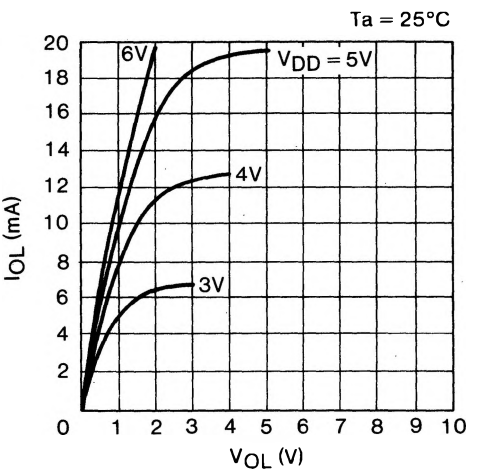
TYP. Current vs Voltage for High State Output (I_{OH}) (V_{OH})



TYP. Maximum Oscillator Frequency f(OSC) vs Temperature (Ta)



TYP. Current vs Voltage for Low State Output (I_{OL}) (V_{OL})



TYP. Supply Current vs Supply Voltage
(I_{DD}) (V_{DD})