OKI semiconductor

MSM66301

OKI ORIGINAL HIGH PERFORMANCE CMOS SINGLE-COMPONENT 8/16-BIT MICROCONTROLLER

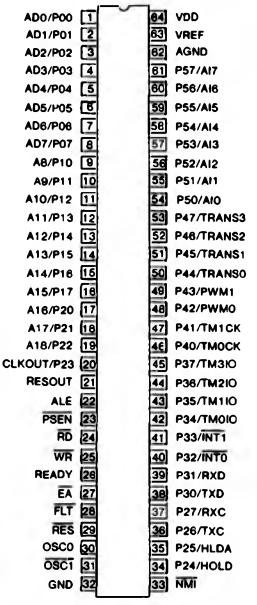
GENERAL DESCRIPTION

The OKI MSM66301 is a an new generation, high performance single component microcontroller inplemented in sillicon gate complementary metal oxide semiconductor technology (CMOS). Integrated within this chip are 16-bit ALU, 16K bytes of mask program ROM, 512 bytes of data RAM, 48 I/O lines, built-in 16-bit timers, 10-bit A/D converter, serial I/O port, pulse width modulator (PWM), and oscillator.

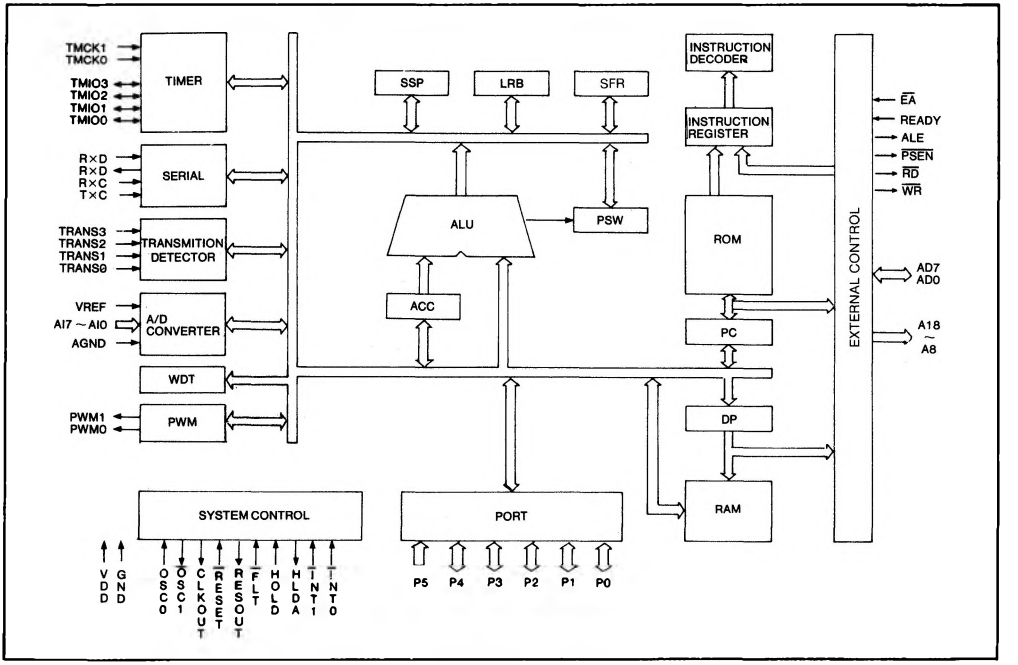
FEATURES

- 8-Bit External Data Bus Interface
- 16-Bit Internal Architecture
- 64K address space for program memory (including 16K bytes onchip ROM)
- 512K address space for data memory (including 512 bytes onchip RAM)
- High speed execution
  Minimum Cycle for Instruction: 400ns (10MHz)
- The Abundance of Powerful Instructions
  8/16 data transfer operation
  8/16 bit arithmetic operation
  16(8) bit × 16(8) bit → 32(16) bit
  32(16) bit/16 (8) bit → 32(16) bit
  16(8) bit ± 16(8) bit → 16(8) bit
  8/16 logic operation
  Bit operation
  String operation
  User stack operation
  ROM table access operation
- The same instruction allows both byte and word width operation according to Data Descriptor.
  That is to say, the same algorithm and the same source program lines are applicable to byte and word width data manipulation with only changing Data Descriptor.
- Many Addressing Modes
- 8 Input lines, $\overline{40}$ Input/Output lines
- Built-in 16 bit timer × 4
  Each timer has the following 4 modes.
  Auto reload timer mode
  Clock out mode
  Capture register mode
  Real time output mode
- Serial Port × 1ch.
  (variable bit length, baud rate generators for transmitter & receiver)
  Asyncronous normal mode
  Asyncronous multi processor communication mode
  Syncronous normal mode
  Syncronous multi processor communication mode
- 16 bit Pulse Width Modulator × 2
- Transition Detector × 4
- 10 bit A/D converter (8 channel)
- 1 non-maskable interrupt, 16 maskable interrupts
- Stand-by Function
  software Clock stop
  software CPU stop
  hardware CPU stop
- 64 pin Shrink DIP/64 pin plastic flat package/68 pin PLCC

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Input/Output	Function
$P_{00} - P_{07}$ / $AD_0 - AD_7$	I/O	P0: 8-bit I/O port. Each bit can be assigned to input or output. AD: Outputs the lower 8 bits of program counter during external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also outputs the address, Outputs or inputs data during an external data memory access instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
$P_{10} - P_{17}$ / $A_8 - A_{15}$	I/O	P1: 8-bit I/O port. Each bit can be assigned to input or output. A: Outputs the middle 8 bits of program counter (PC_{8-15}) during external program memory fetch. Also outputs the middle 8 bits of address during an external data memory access instructions.
$P_{20} - P_{22}$ / $A_{16} - A_{18}$	I/O	P2: 8-bit I/O port. Each bit can be assigned to input or output. A: Outputs the upper 3 bits of address during external data memory access instructions.
P_{23}/CLKOUT		CLKOUT: clock output pin. Output frequency range is equal to or twice the system clock.
P_{24}/HOLD		HOLD: Input pin to request the CPU to enter the hardware power-down state.
P_{25}/HLDA		HLDA: HOLD ACKNOWLEDGE: the HLDA signal appears in reponse to the HOLD signal and indicates that the CPU has entered the power-down state.
P_{26}/TxC		TxC: Transmitter clock input pin.
P_{27}/RxC		RxC: Receiver clock input pin.
P_{30}/TxD	I/O	P3: 8-bit I/O port. Each bit can be assigned to input or output. TxD: Transmitter data output pin. RxD: Receiver data input pin. $\overline{INT}$: Interrupt Request Input pin. Falling edge trigger or level trigger is selectable. TM0IO ~ TM3IO: One of the following signals is output or input: • clock twice the frequency range of the 16 bit timer overflow • load trigger signal to the capture register input • setting value output The signal that is input or output depends on the mode.
P_{31}/RxD		
P_{32}/$\overline{INT0}$		
P_{33}/$\overline{INT1}$		
P_{34}/TM0IO		
P_{35}/TM1IO		
P_{36}/TM2IO		
P_{37}/TM3IO		

PIN DESCRIPTION (Continued)

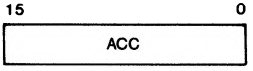
Designation	Input/Output	Function
P_{40}/TM0CK P_{41}/TM1CK P_{42}/PWM0 P_{43}/PWM1 P_{44} – P_{47} / TRANS0 – TRNS3	I/O	P4: 8 bit I/O port. Each bit can be assigned to input or output. TM0CK, TM1CK: clock input pins of timer 0, timer 1. TRNS: Transition Detector. The input pins which sense the falling edge and set the flag. PWM: Pulse Wide Modulator output pin.
P_{50} – P_{57} / AI0 – AI7	INPUT	P5: 8 bit input port. AI: analog sygnal input pin to A/D converter.
RESOUT	OUTPUT	Output 'H' level when the CPU is in RESET cycle. Reset to 'L' level by program.
ALE	OUTPUT	Address Latch Enable: The timing pulse to latch the lower 8 bit of the address output from port 0 when the CPU accesses the external data memory.
$\overline{PSEN}$	OUTPUT	Program Store Enable: The strobe pulse to fetch to external program memory.
$\overline{RD}$	OUTPUT	Output strobe activated during a BUS read. Can be used to enable data on to the bus from the external data memory.
$\overline{WR}$	OUTPUT	Output strobe during a bus write. Used as write strobe to external data memory.
READY	INPUT	Used when the CPU accesses low speed peripherals.
$\overline{EA}$	INPUT	Normaly set to 'H' level. If set to 'L' level, the CPU fetches the code to external program memory.
$\overline{FLT}$	INPUT	If $\overline{FLT}$ is 'H' level, ALE, $\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$ are set 'H' level when reset. If $\overline{FLT}$ is set to 'L', ALE, $\overline{WR}$, $\overline{RD}$ $\overline{PSEN}$ are set to floating level when reset.
$\overline{RESET}$	INPUT	RESET input pin

PIN DESCRIPTION (Continued)

Designation	Input/Output	Function
OSC_0, $\overline{OSC_1}$		Oscillation circuit consists of OSC_0, $\overline{OSC_1}$.
$\overline{NMI}$	INPUT	non maskable interrupt input pin (falling edge)
VREF		reference voltage input pin for A/D converter
AGND		ground for A/D converter
VDD		system power supply
GND		ground

REGISTERS

■ **ACCUMULATOR**



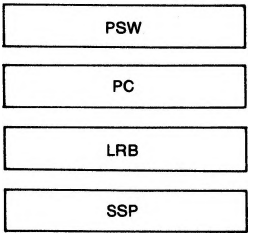
■ **CONTROL REGISTERS (CR)**

PROGRAM STATUS WORD

PROGRAM COUNTER

LOCAL REGISTER BASE

SYSTEM STACK POINTER



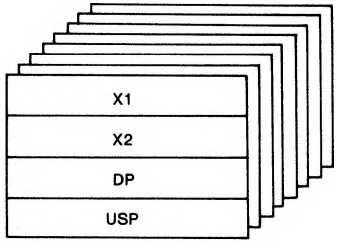
■ **POINTING REGISTERS (PR)**

INDEX REGISTER1

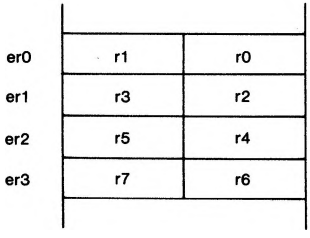
INDEX REGISTER2

DATA POINTER

USER STACK POINTER



■ **LOCAL REGISTERS**



■ **SPECIAL FUNCTION REGISTERS (SFR)**

All of the I/O functions are controlled by SFRs.Also, some of the internal functions (Timer, WDT, etc,...) are controlled by SFRs. SFRs are located in the top of RAM space (000H ~ 007FH).

MSM66301 Special Function Registers [1]

Address	Name	Abbrebiation	R/W	8/16 Operation	When reset
0000	System Stack Pointer	SSPL	R/W	8/16	FF
0001		SSPH			FF
0002	Local Register Base	LRBL	R/W	8/16	unknown
0003		LRBH			
0004	Program Status Word	PSWL	R/W	8/16	00
0005		PSWH			00
0006	Accumulator	ACCL	R/W	8/16	00
0007		ACCH			00
0008	Source Index Register	SI	R/W	16	unknown
0009	for Block Transfer				
000A	Destination Index Register	DI	R/W	16	unknown
000B	for Block Transfer				
000C	Counter Register	CX	R/W	16	unknown
000D	for Block Transfer				
000E	Source/Destination Bank Register	BSDI	R/W	8	unknown
0010	Stand-By Control Register	SBYCON	R/W	8	00
0011	Watch Dog Timer	WDT	W	8	
0012	Peripheral Control Register	PRPHF	R/W	8	01
0016	Work Area for Emulator		R/W	16	unknown
0017					
0018	Interrupt Request Flag	IRQL	R/W	8/16	00
0019		IRQH			00
001A	Interrupt Enable Flag	IEL	R/W	8/16	00
001B		IEH			00
001C	External Interrupt Control Register	EXICON	R/W	8	00

MSM66301 Special Function Registers [2]

Address	Name	Abbrebiation	R/W	8/16 Operation	When reset
0020	Port 0 Data Register	P0	R/W	8	Unknown
0021	Port 0 Mode Register	P0IO	R/W	8	00
0022	Port 1 Data Register	P1	R/W	8	unknown
0023	Port 1 Mode Register	P1IO	R/W	8	00
0024	Port 2 Data Register	P2	R/W	8	unknown
0025	Port 2 Mode Register	P2IO	R/W	8	00
0026	Port 2 Special Function Control Register	P2SF	R/W	8	00
0028	Port 3 Data Register	P3	R/W	8	unknown
0029	Port 3 Mode Register	P3IO	R/W	8	00
002A	Port 3 Special Function Control Register	P3SF	R/W	8	00
002C	Port 4 Data Register	P4	R/W	8	unknown
002D	Port 4 Mode Register	P4IO	R/W	8	00
002E	Port 4 Special Function Control Register	P4SF	R/W	8	00
002F	Port 5	P5	R	8	
0030	Timer 0 Counter	TM0	R/W	16	00
0031					00
0032	Timer 0 Register	TMR0	R/W	16	00
0033					00
0034	Timer 1 Counter	TM1	R/W	16	00
0035					00
0036	Timer 1 Register	TMR1	R/W	16	00
0037					00
0038	Timer 2 Counter	TM2	R/W	16	00
0039					00
003A	Timer 2 Register	TMR2	R/W	16	00
003B					00
003C	Timer 3 Counter	TM3	R/W	16	00
003D					00
003E	Timer 3 Register	TMR3	R/W	16	00
003F					00

MSM66301 Special Function Registers [3]

Address	Name	Abbrebiation	R/W	8/16 Operation	When reset
0040	Timer 0 Control Register	TCON0	R/W	8	00
0041	Timer 1 Control Register	TCON1	R/W	8	00
0042	Timer 2 Control Register	TCON2	R/W	8	00
0043	Timer 3 Control Register	TCON3	R/W	8	00
0046	Transition Detector Reg.	TRNS	R/W	8	00
0013	Stop Mode Buffer Flag		W	8	

MSM66301 Special Function Registers [4]

Address	Name	Abbrebiation	R/W	8/16 Operation	When reset
0046	Transition Detector	TRNS	R/W	8	00
0048	Transmitter Clock Generator	STTM	R/W	8	00
0049	Transmitter Clock Generator Control Register	STTMR	R/W	8	00
004A	Transmitter Control Register	STTMC	R/W	8	00
004C	Receiver Clock Generator	SRTM	R/W	8	00
004D	Receiver Clock Generator Control Register	SRTMR	R/W	8	00
004E	Receiver Control Register	SRTMC	R/W	8	00
0050	Transmitter Mode Control Register	STCON	R/W	8	00
0051	Transmitter Data Buffer	STBUF	W	8	unknown
0054	Receiver Mode Control Register	SRCON	R/W	8	00
0055	Receiver Data Buffer	SRBUF	R	8	unknown
0056	Receiver-Eroor Status Register	SRSTAT	R	8	00
0058	A/D Scanning Mode Register	ADSCAN	R/W	8	00
0059	A/D Select Mode Register	ADSEL	R/W	8	00
0060	A/D Convert Result Register 0	ADCR0L	R	8/16	unknown
0061		ADCR0H			
0062	A/D Convert Result Register 1	ADCR1L	R	8/16	unknown
0063		ADCR1H			
0064	A/D Convert Result Register 2	ADCR2L	R	8/16	unknown
0065		ADCR2H			
0066	A/D Convert Result Register 3	ADCR3L	R	8/16	unknown
0067		ADCR3H			
0068	A/D Convert Result Register 4	ADCR4L	R	8/16	unknown
0069		ADCR4H			
006A	A/D Convert Result Register 5	ADCR5L	R	8/16	unknown
006B		ADCR5H			
006C	A/D Convert Result Register 6	ADCR6L	R	8/16	unknown
006D		ADCR6H			
006E	A/D Convert Result Register 7	ADCR7L	R	8/16	unknown
006F		ADCR7H			

MSM66301 Special Function Registers [5]

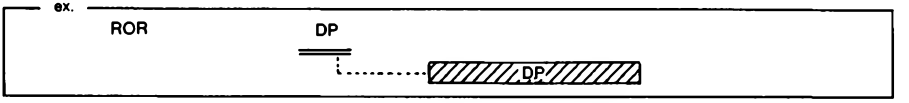
Address	Name	Abbrebiation	R/W	8/16 Operation	When reset
0070	PWM 0 Counter	PWMC0L	R/W	8/16	00
0071		PWMC0H			00
0072	PWM 0 Register	PWMR0L	R/W	8/16	00
0073		PWMR0H			00
0074	PWM 1 Counter	PWMC1L	R/W	8/16	00
0075		PWMC1H			00
0076	PWM 1 Register	PWMR1L	R/W	8/16	00
0077		PWMR1H			00
0078	PWM 0 Control Register	PWCON0	R/W	8	00
007A	PWM 1 Control Register	PWCON1	R/W	8	00

ADDRESSING MODE

The MSM66301 supports 512KB (64KB×8BANKs) 05 data space and 64KB of program space with verious types of addressing methods. These methods divide into the following types.

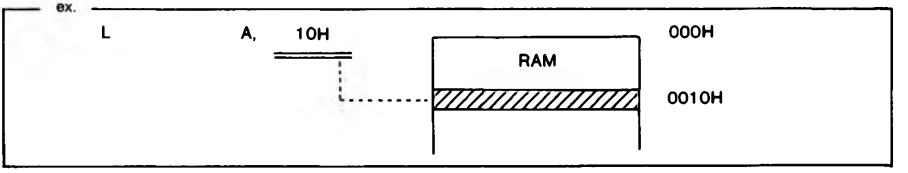
1. RAM ADDRESSING (FOR DATA SPACE)

1.1 Register Direct Addressing

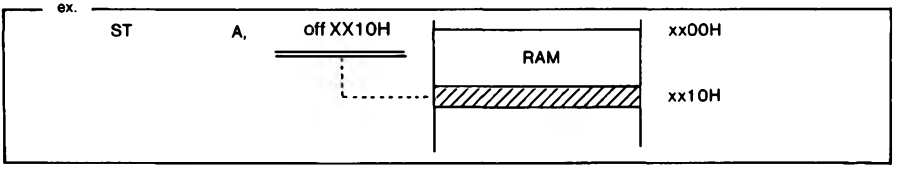


1.2 Displacement Addressing

a) Zero Page

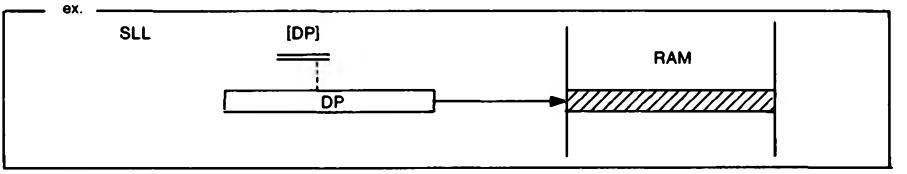


b) Direct Page

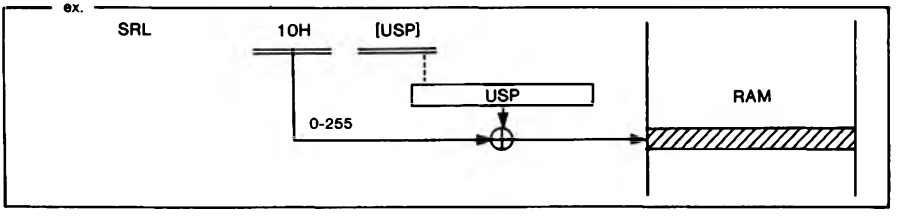


1.3 Pointing Register Indirect Addressing

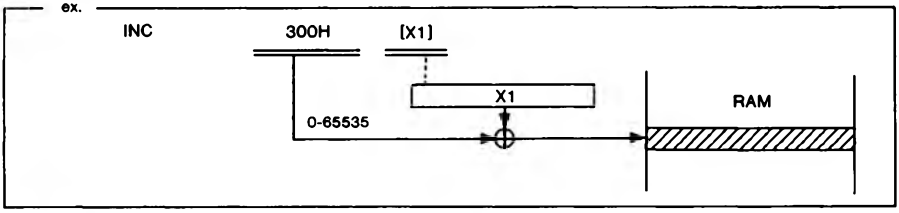
a) Data Pointer (DP) Indirect



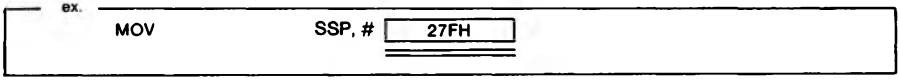
b) User Stack Pointer (USP) Indirect



c) Index register (X1, X2) Indirect

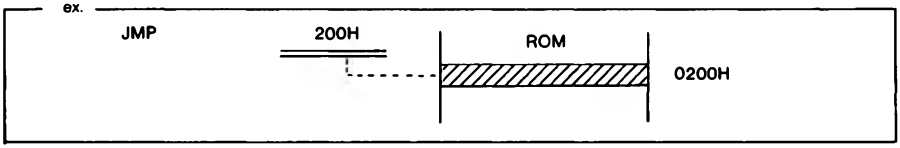


1.4 Immediate Addressing



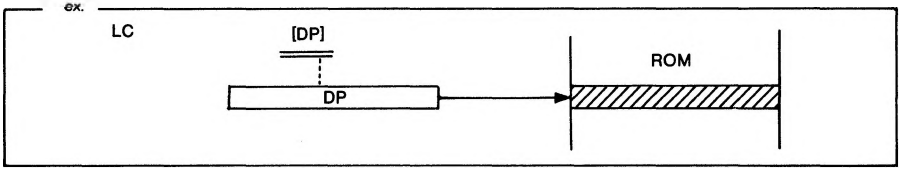
2. ROM ADDRESSING (FOR PROGRAM SPACE)

2.1 Direct Addressing

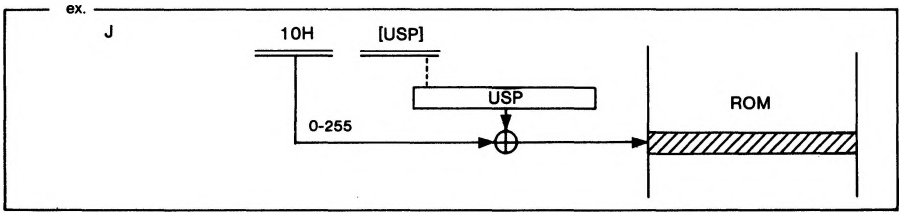


2.2 Pointing Register Indirect Addressing

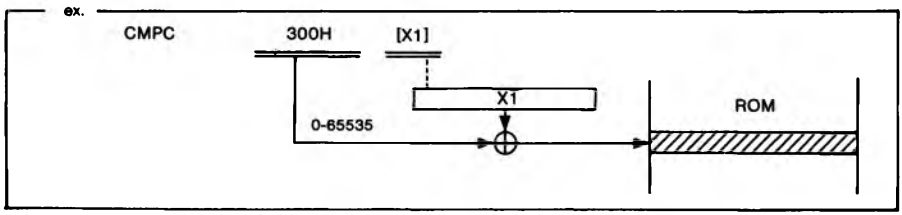
a) Data Pointer (DP) Indirect



b) User Stack Pointer (USP) Indirect



c) Pointing Register (X1, X2, DP, USP) Indirect with 16bit displacement



INSTRUCTIONS

Data Transfer

Instruction	Function
L A,*	A ← *
ST A,*	A → *
MOV *, A	* ← A
MOV *, #	* ← Imme.
MOV er.*	er ← *
MOV d,*	(d) ← *
MOV DP,*	DP ← *
MOV X1,*	X1 ← *
MOV X2,*	X2 ← *
MOV USP,*	USP ← *
MOV PSW,*	PSW ← *
MOV SSP,*	SSP ← *
MOV LRB,*	LRB ← *
CLR *	* ← 0
SWAP	$A_{15-8} \longleftrightarrow A_{7-0}$
XCHG A,*	A ⟷ *
XNBL A,*	$A_{3-0} \longleftrightarrow *_{3-0}$
TRNS USP, LRB	$USP_{15-3} \leftarrow LRB_{12-0}$ $USP_{2-0} \leftarrow 0$
TRNS LRB, USP	$LRB_{12-0} \leftarrow USP_{15-3}$ $LRB_{15-13} \leftarrow 0$

Instruction	Function
LB A,*	$A_L \leftarrow *$
STB A,*	$A_L \rightarrow *$
MOVB A,*	$A_L \leftarrow *$
MOVB *, A	* ← AL
MOVB *, #	* ← Imme.
MOVB r,*	r ← *
MOVB d,*	(d) ← *
MOVB PSW0,*	PSW0 ← *
MOVB SCB,*	SCB ← *
CLRB *	* ← 0
SWAPB	$A_{7-4} \longleftrightarrow A_{3-0}$
XCHGB	A_L ⟷ *

Push & Pop

Instruction	Function
PUSHU *	* → USER STACK
POPU A	A ← USER STACK
PUSHS *	* → SYSTEM STACK
POPS *	* ← SYSTEM STACK

Instruction	Function
PUSHUB *	* → USER STACK
POPUB A	A_L ← USER STACK

Rotate & Shift

Instruction	Function
ROL *	Rotate ←
ROR *	Rotate →
SLL *	Shift ← Logical
SRL *	Shift → Logical
SRA *	Shift → Arithmetic

Instruction	Function
ROLB *	Rotate ←
RORB *	Rotate →
SLLB *	Shift ← Logical
SRLB *	Shift → Logical
SRAB *	Shift → Arithmetic

Increment & Decrement

Instruction	Function
INC *	* ← *+1
DEC *	* ← *−1

Instruction	Function
INCB *	* ← * + 1
DECB *	* ← * − 1

ROM Table Reference

Instruction	Function
LC A,*	A ← * (ROM)
CMPC A,*	A − * (ROM)

Instruction	Function
LCB A, *	A_L ← * (ROM)
CMPCB A, *	A_L − * (ROM)

Arithmetic Operation

Instruction		Function
MUL		er1: A ← A×er0
DIV		er0: A ← er0: A/er2
ADD	A, *	A ← A+*
ADD	*, A	* ← *+A
ADD	*, d	* ← *+(d)
ADD	*, #	* ← *+Imme.
ADC	A, *	A ← A+*+C
ADC	*, A	* ← *+A+C
ADC	*, d	* ← *+(d)+C
ADC	*, #	* ← *+Imme.+C
SUB	A, *	A ← A−*
SUB	*, A	* ← *−A
SUB	*, d	* ← *−(d)
SUB	*, #	* ← *−Imme.
SBC	A, *	A ← A−*−C
SBC	*, A	* ← *−A−C
SBC	*, d	* ← *−(d)−C
SBC	*, #	* ← *−Imme.−C

Instruction		Function
MULB		A ← A_L×r0
DIVB		A ← A/r0
ADDB	A, *	A_L ← A_L+*
ADDB	*, A	* ← *+A_L
ADDB	*, d	* ← *+(d)
ADDB	*, #	* ← *+Imme.
ADCB	A, *	A_L ← A_L+*+C
ADCB	*, A	* ← *+A_L+C
ADCB	*, d	* ← *+(d)+C
ADCB	*, #	* ← *+Imme.+C
SUBB	A, *	A_L ← A_L−*
SUBB	*, A	* ← *−A_L
SUBB	*, d	* ← *−(d)
SUBB	*, #	* ← *−Imme.
SBCB	A, *	A_L ← A_L−*−C
SBCB	*, A	* ← *−A_L−C
SBCB	*, d	* ← *−(d)−C
SBCB	*, #	* ← *−Imme.−C

Logical Operation

Instruction		Function
AND	A,*	A ← A and *
AND	*, A	* ← * and A
AND	*, d	* ← * and (d)
AND	*, #	* ← * and Imme.
OR	A, *	A ← A or *
OR	*, A	* ← * or A
OR	*, d	* ← * or (d)
OR	*, #	* ← * or Imme.
XOR	A, *	A ← A xor *
XOR	*, A	* ← * xor A
XOR	*, d	* ← * xor (d)
XOR	*, #	* ← * xor Imme.

Instruction		Function
ANDB	A, *	A_L ← A_L and *
ANDB	*, A	* ← * and A_L
ANDB	*, d	* ← * and (d)
ANDB	*, #	* ← * and Imme.
ORB	A, *	A_L ← A_L or *
ORB	*, A	* ← * or A_L
ORB	*, d	* ← * or (d)
ORB	*, #	* ← * or Imme.
XORB	A, *	A_L ← A_L xor *
XORB	*, A	* ← * xor A_L
XORB	*, d	* ← * xor (d)
XORB	*, #	* ← * xor Imme.

Comparison

Instruction		Function
CMP	A, *	A − *
CMP	*, A	* − A
CMP	*, d	* − (d)
CMP	*, #	* − Imme.

Instruction		Function
CMPB	A, *	A_L − *
CMPB	*, A	* − A_L
CMPB	*, d	* − (d)
CMPB	*, #	* − Imme.

Stack Operation

Instruction	Function
ADD A. [+USP]	USP ← USP + 2, A ← A + [USP]
ADC A. [+USP]	USP ← USP + 2, A ← A + [USP] + C
SUB A. [+USP]	USP ← USP + 2, A ← A – [USP]
SBC A. [+USP]	USP ← USP + 2, A ← A – [USP] – C
AND A. [+USP]	USP ← USP + 2, A ← A and [USP]
OR A. [+USP]	USP ← USP + 2, A ← A_{or} [USP]
XOR A. [+USP]	USP ← USP + 2, A ← A_{xor} [USP]
CMP A. [+USP]	USP ← USP + 2, A – [USP]

Decimal Adjust

Instruction	Function
DAA	Decimal Adjust for Addition
DAS	Decimal Adjust for Substruct

Bit Operation

Instruction		Function
SBR	*	bit ← 1
RBR	*	bit ← 0
MBR	C, *	C ← bit
MBR	*, C	bit ← C
TRB	*	Z ← bit

Instruction		Function
SB	*	bit ← 1
RB	*	bit ← 0
MB	C, *	C ← bit
MB	*, C	bit ← C

Execute

Instruction		Function
EX	*	Execute Specified Data as the Instruction

Jump & Call

Instruction	Function
SJ adrs	Short Jump
J *	Jump
JC EQ, adrs	Jump if '='
JC LE, adrs	Jump if '< ='
JC GE, adrs	Jump if '> ='
JBS bit, adrs	Jump if bit-on
JRNZ, DP, adrs	Loop Function

Instruction	Function
SCAL adrs	Short Call
CAL *	Call Subroutine
JC NE, adrs	Jump if '≠'
JC LT, adrs	Jump if '<'
JC GT, adrs	Jump if '<'
JBR bit, adrs	Jump if bit-off
VCAL adrs	Vector Call

Return

Instruction	Function
RT	Return from Subroutine
RTI	Return from Interrupt

String Operation

Instruction	Function
SMOVI	String Transfer with Increasing Pointers
SMOVD	String Transfer with Decreasing Pointers
SCMP	String Compare

Others

Instruction	Function
SC	C ← 1
SS	STACK FLAG ← 1
NOP	No Operation

Instruction	Function
RC	C ← 0
BRK	Software Reset

(Note)

'*'	Addressing expression (See Addressing mode)
'#' and 'imme.'	Immediate value
'←' and '→'	Bit-shift direction

ABSOLUTE MAXIMUM RATING (TARGET SPECIFICATION)

Item	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7.0	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Output Voltage	V_O		−0.3 ~ V_{DD}	V
Analog Reference Voltage	V_R		−0.3 ~ V_{DD}	V
Analog Input Voltage	V_{AI}		−0.3 ~ V_R	V
Power Desipation	P_D	Ta = 25°C, per Package	400 Max.	mW
		Ta = 25°C, per Output	50 Max.	mW
Storage Temperature	T_{STG}	–	−55 ~ 150	°C

OPERATING RANGE

Item	Symbol	Condition		Value	Unit
Power Supply Voltage	V_{DD}	f (OSC) ≦ 10 MHz		4.5 ~ 5.5	V
Data Retention Voltage	V_{DDH}	f (OSC) = 0 Hz		2 ~ 6	V
Analog Reference Voltage	V_R	–		4.5 ~ V_{DD}	V
Analog Ground Voltage	V_{AG}			0 ~ 0.2	V
Analog Input Voltage	V_{AI}			V_{AG} ~ V_R	V
Fan Out	N	MOS Load		30	
		TTL Load	P_{00} ~ P_{07}	2	
			P_{10} ~ P_{47}	1	

DC CHARACTERISTICS (TARGET SPECIFICATION)

(V_{DD} = 5V ±10%, Ta = –40 ~ +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage *1,*2,*3,*7	V_{IH}	–	2.4		V_{DD}	V
"H" Input Voltage *6,*7,*9	V_{IH}	–	4.0		V_{DD}	V
"L" Input Voltage *1,*2,*3,*7	V_{IL}	–	–3.0		0.8	V
"L" Input Voltage *6,*8,*9	V_{IL}	–	–0.3		0.8	V
"H" Output Voltage *1,*2,*4,*5	V_{OH}	I_O = –30 μA	4.2			V
"H" Output Voltage *10	V_{OH}	I_O = –15 μA	4.2			V
"L" Output Voltage *1,*4	V_{OL}	I_O = 3.2 mA			0.45	V
"L" Output Voltage *2,*5	V_{OL}	I_O = 1.6 mA			0.45	V
"L" Output Voltage *10	V_{OL}	I_O = –15 μA			0.4	V
Input Current *1,*2,*3,*7,*8	I_{IH}/I_{ILI}	V_I = VDD/0V			1/–1	μA
Input Current *6	I_{IH}/I_{IL}	V_I = VDD/0V			1/–20	μA
Input Current *9	I_{IH}/I_{IL}	V_I = VDD/0V			10/–10	μA
"H" Output Current *1,*2,*4,*5	I_{OH}	V_O = 2.4V	–0.2			mA
Analog Reference Voltage Supply Resistance	R_R	V_{AG} = 0V		16		KΩ
Analog Input Leak Current	R_{LAI}	V_{AG} = 0V			±1	μA
Analog Input Impedance	R_{AI}	A/D Converter Active and In Sampling Condition		1		MΩ
	C_{AI}			10		pF
Input Capacity	C_I	f = 1MHz, Ta = 25°C		5		pF
Output Capacity	C_O	f = 1MHz, Ta = 25°C		7		pF
Current Consumption (Stop)	I_{DDS}	V_{DD} = 2V, No Load, Ta = 25°C		0.2		μA
		No Load		1		μA
Current Consumption	I_{DD}	f (OSC) = 10MHz, No Load		20		mA

*1 Specification applied to P0
*2 Specification applied to P1, P2, P3, P4
*3 Specification applied to P5
*4 Specification applied to ALE, PSEN, RD, WR
*5 Specification applied to RESOUT
*6 Specification applied to RES, NMI
*7 Specification applied to READY, EA
*8 Specification applied to FLT
*9 Specification applied to OSC_0
*10 Specification applied to OSC_1

AC CHARACTERISTICS (TARGET SPECIFICATION)

External Program Memory Control

(V_{DD} = 5V ±10%, Ta = –40 ~ +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OSC Clock Pulse Width	$t_{\phi W}$	–	50			nS
ALE Pulse Width	t_{AW}	–	100			nS
PSEN Pulse Width	t_{PW}	–	250			nS
PSEN Pulse Delay Time	t_{PAD}	C_L = 50pF			$t_{\phi W}$+20	nS
"L" Address Set Up Time	t_{AAS}		$t_{\phi W}$-30		$t_{\phi W}$+30	nS
"L" Address Hold Time	t_{AAH}		$t_{\phi W}$-30		$t_{\phi W}$+30	nS
"H" Address Delay Time	t_{AAD}				$t_{\phi W}$+30	nS
"H" Address Hold Time	t_{APH}		$t_{\phi W}$-10		$t_{\phi W}$+40	nS
Instruction Set Up Time	t_{IS}		80			nS
Instruction Hold Time	t_{IH}		50			nS

External Data Memory Control

(V_{DD} = 5V ±10%, Ta = –40 ~ +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OSC Clock Pulse Width	$t_{\phi W}$	–	50			nS
ALE Pulse Width	t_{AW}	–	100			nS
RD Pulse Width	t_{RW}	–	250			nS
WR Pulse Width	t_{WW}	–	200			nS
RD Pulse Delay Time	t_{RAD}	C_L = 50pF			$t_{\phi W}$+20	nS
WR Pulse Delay Time	t_{WAD}				$t_{\phi W}$+20	nS
"L" Address Set Up Time	t_{AAS}		$t_{\phi W}$-30		$t_{\phi W}$+30	nS
"L" Address Hold Time	t_{AAH}		$t_{\phi W}$-30		$t_{\phi W}$+30	nS
"H" Address Delay Time	t_{AAD}				$t_{\phi W}$+30	nS
"H" Address Hold Time (RD)	t_{ARH}		$t_{\phi W}$-10		$t_{\phi W}$+40	nS
"H" Address Hold Time (WR)	t_{AWH}		$2t_{\phi W}$-10		$2t_{\phi W}$+40	nS
Memory Data Set Up Time	t_{MS}		80			nS
Memory Data Hold Time	t_{MH}		50			nS
Data Delay Time	t_{DD}				$t_{\phi W}$+30	nS
Data Hold Time	t_{DH}		$2t_{\phi W}$-10		$2t_{\phi W}$+40	nS

A/D CONVERSION CHARACTERISTICS (TARGET SPECIFICATION)

(V_{DD} = 5V ±10%,)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	$V_R = V_{DD}$ V_{AG} = GND = 0V Analog Input Impedance ≦ 5KΩ Ta = 25°C		10		Bits
Zero Point Error	E_{ZS}			±2		LSB
Full Scale Error	E_{FS}			±2		LSB
Linearity Error	E_L			±3		LSB
Input Crosstalk				±2		LSB
Channel Conversion Speed	t_C		64		320	μs/CH

TIMING CHART