OKI semiconductor

MSM81C55RS/GS

2048 BIT CMOS STATIC RAM WITH I/O PORTS AND TIMER

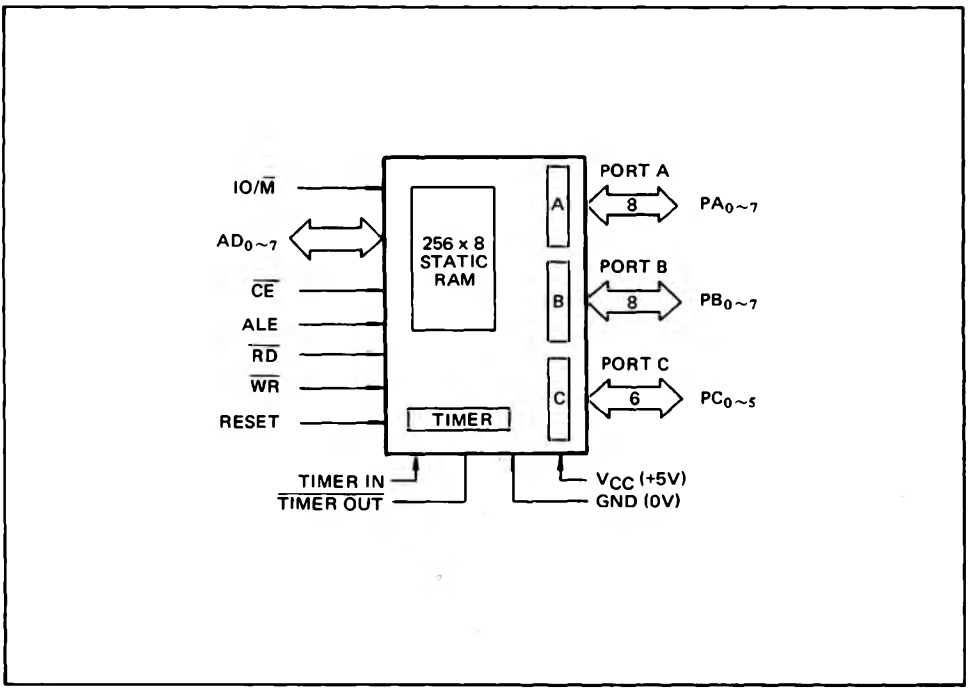
GENERAL DESCRIPTION

The MSM81C55RS/GS is a 2k bit static RAM (256 byte) with parallel I/O ports and timer. It uses silicon gate CMOS technology and consumes a standby current of 100 micro ampere maximum while the chip is not selected. Featuring a maximum access time of 400 ns, the MSM81C55RS/GS can be used in an 80C85A system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose). The MSM81C55RS also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal count-pulsing.

FEATURES

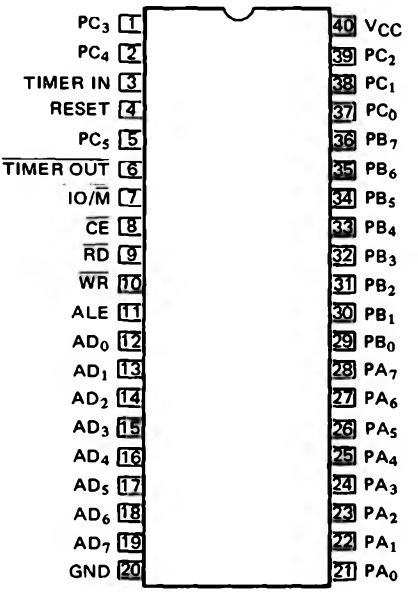
- High speed and low power achieved with silicon gate CMOS technology.
- 256 words x 8 bits
- Single power supply, 3 to 6V
- Completely static operation
- On-chip address latch
- 8-bit programmable I/O ports (port A and B)
- TTL Compatible
- RAM data hold characteristic at 2V
- 6-bit programmable I/O port (port C)
- 14-bit programmable binary counter/timer
- Multiplexed address/data bus
- 40 pin DIP package (MSM81C55RS)
- 44 pin flat package (MSM81C55GS)
- Direct interface with MSM80C85A (3MHz)

FUNCTIONAL BLOCK DIAGRAM

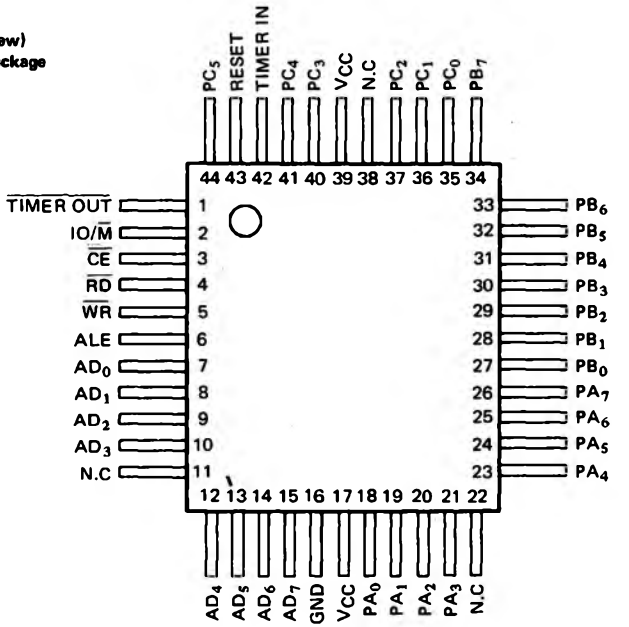


PIN CONFIGURATION

MSM81C55RS (Top View)
40 Lead Plastic DIP



MSM81C55GS (Top View)
44 Lead Plastic Flat Package



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM81C55RS	MSM81C55GS	
Supply Voltage	V_{CC}	Referenced to GND	−0.5 to +7		V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5		V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5		V
Storage Temperature	T_{stg}		−55 to + 150		°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	W

OPERATING CONDITION

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Level Input	V_{IL}	−0.3		+0.8	V
"H" Level Input	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Level Output Voltage	V_{OL}	I_{OL} = 2mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to 85°C			0.45	V
"H" Level Output Voltage	V_{OH}	I_{OH} = −400μA		2.4			V
		I_{OH} = −40μA		4.2			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Standby Current	I_{CCS}	$\overline{CE} \geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$ $V_{IL} \leqq V_{CC}-0.2V$			0.1	100	μA
Mean Operating Current	I_{CC}	Memory cycle time: 1μs				5	mA

AC CHARACTERISTICS

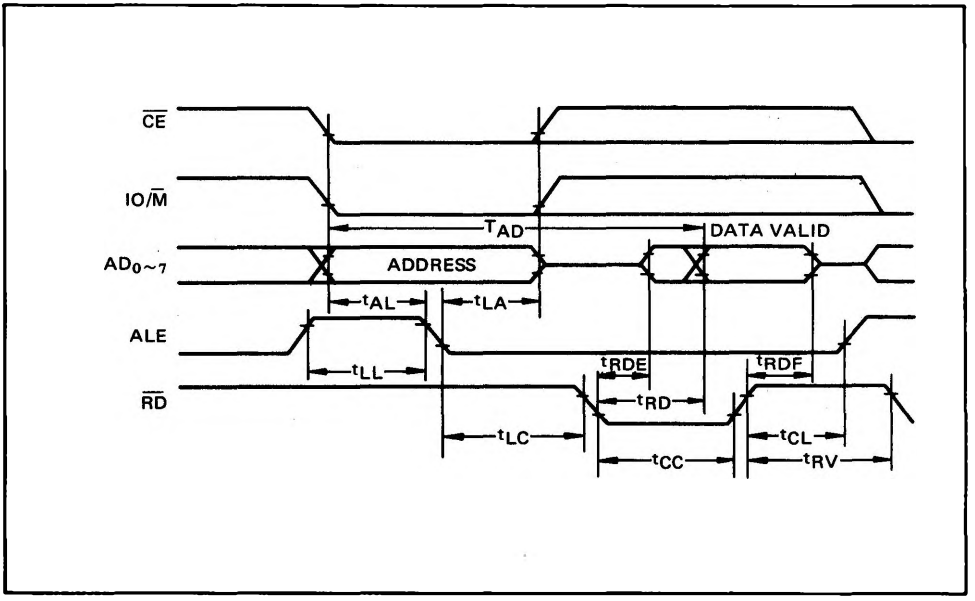
(V_{CC} = 4.5 to 5.5V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address/latch Set-up Time	t_{AL}	50		ns	
Latch/address Hold Time	t_{LA}	30		ns	
Latch/read (write) Delay Time	t_{LC}	100		ns	
Read/output Delay Time	t_{RD}		170	ns	
Address/output Delay Time	t_{AD}		400	ns	
Latch Width	t_{LL}	100		ns	
Read/data Bus Floating Time	t_{RDF}	0	100	ns	
Read (write)/latch Delay Time	t_{CL}	20		ns	
Read (write) Width	t_{CC}	250		ns	
Data In/write Set-up Time	t_{DW}	150		ns	
Write/data-in Hold Time	t_{WD}	0		ns	
Recovery Time	t_{RV}	300		ns	
Write/port Output Delay Time	t_{WP}		400	ns	
Port Input/read Set-up Time	t_{PR}	70		ns	Load capacitance: 150pF
Read/port Input Hold Time	t_{RP}	50		ns	
Strobe/buffer Full Delay Time	t_{SBF}		400	ns	
Strobe Width	t_{SS}	200		ns	
Strobe/buffer Empty Delay Time	t_{RBE}		400	ns	
Strobe/interrupt-on delay time	t_{SI}		400	ns	
Read/interrupt-off Delay Time	t_{RDI}		400	ns	
Port Input/strobe Set-up Time	t_{PSS}	50		ns	
Strobe/port-input Hold Time	t_{PHS}	120		ns	
Strobe/buffer-empty Delay Time	t_{SBE}		400	ns	
Write/buffer-full Delay Time	t_{WBF}		400	ns	
Write/interrupt-off Delay Time	t_{WI}		400	ns	
Timer Output Delay Time Low	t_{TL}		400	ns	
Timer Output Delay Time High	t_{TH}		400	ns	
Read/data Bus Enable Delay Time	t_{RDE}	10		ns	
Timer Cycle Time	t_{CYC}	320		ns	
Timer Input Rise and Fall Times	t_r, t_f		80	ns	
Timer Input Low Level Time	t_1	80		ns	
Timer Input High Level Time	t_2	120		ns	

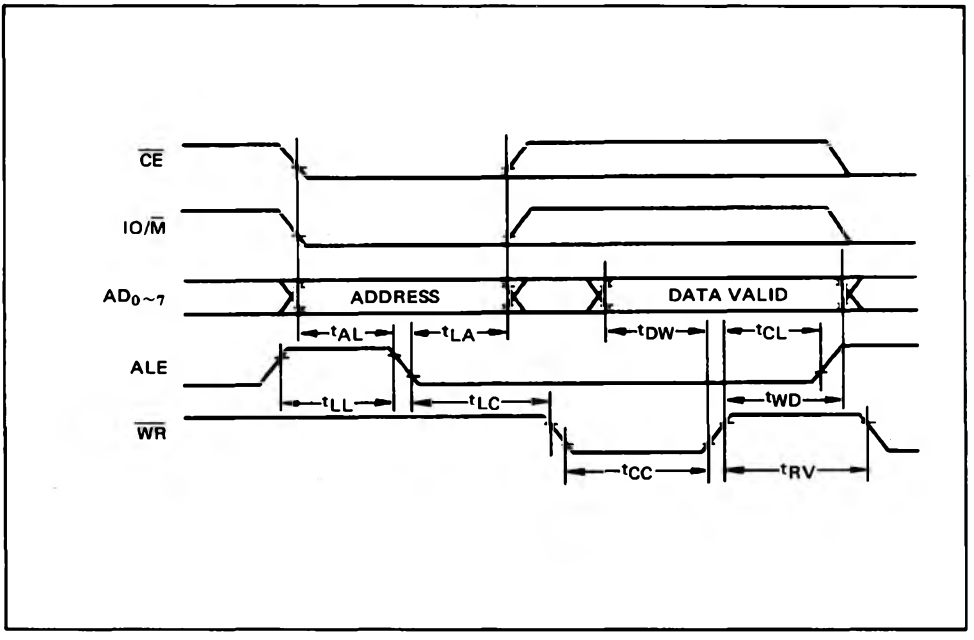
Note: Timing are measured with V_L = 0.8V and V_H = 2.2V for both input and output.

TIMING

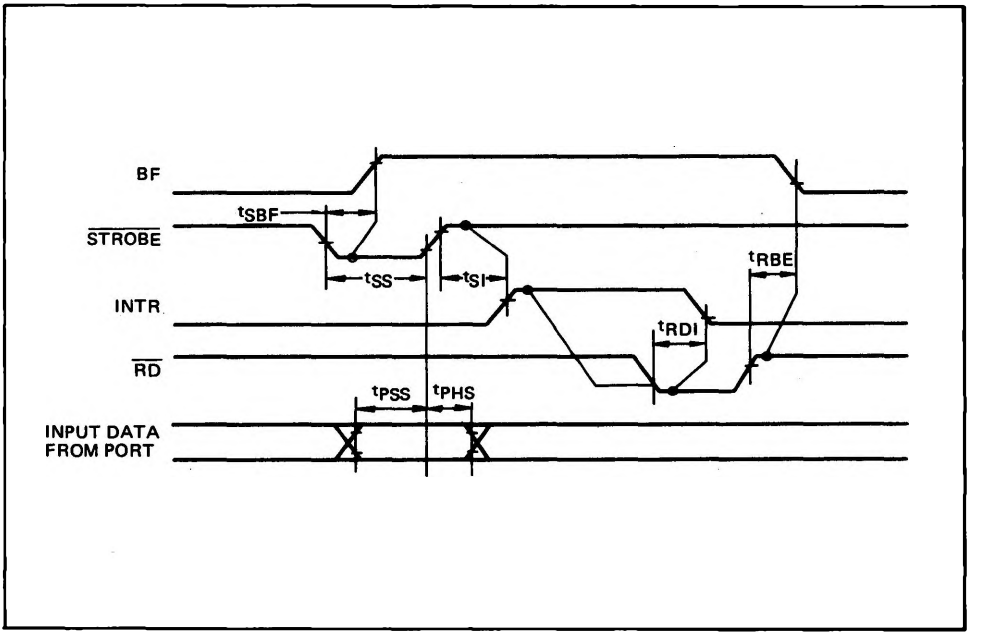
Read Cycle



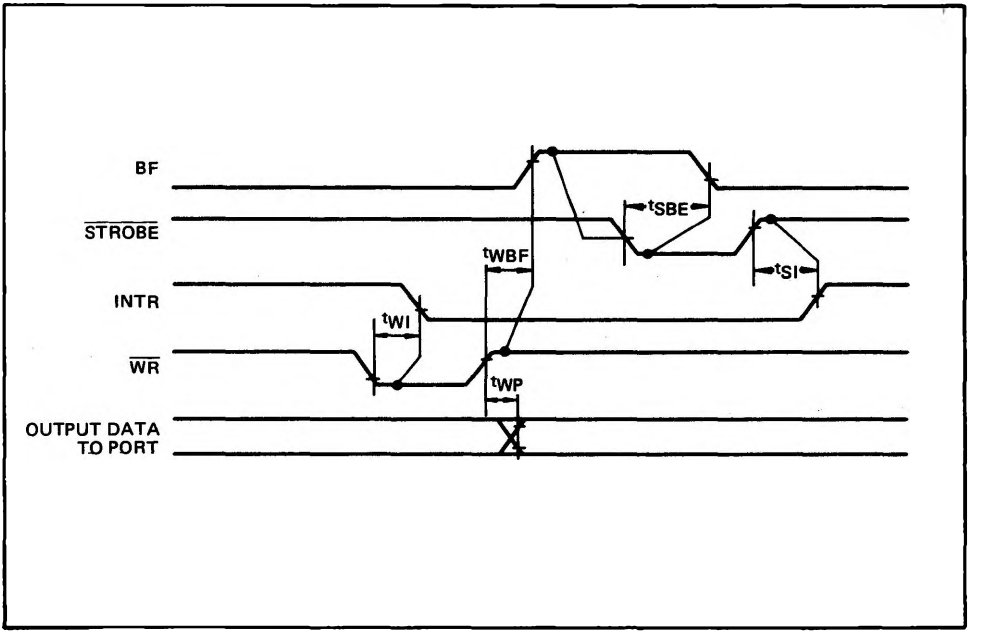
Write Cycle



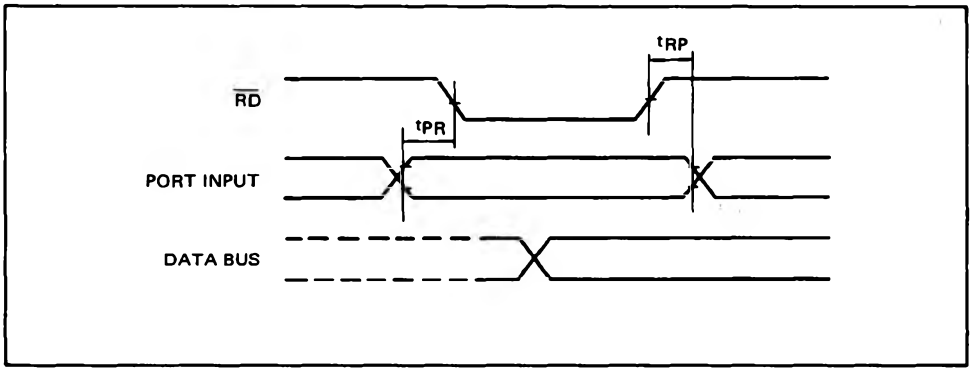
Strobe Input Mode



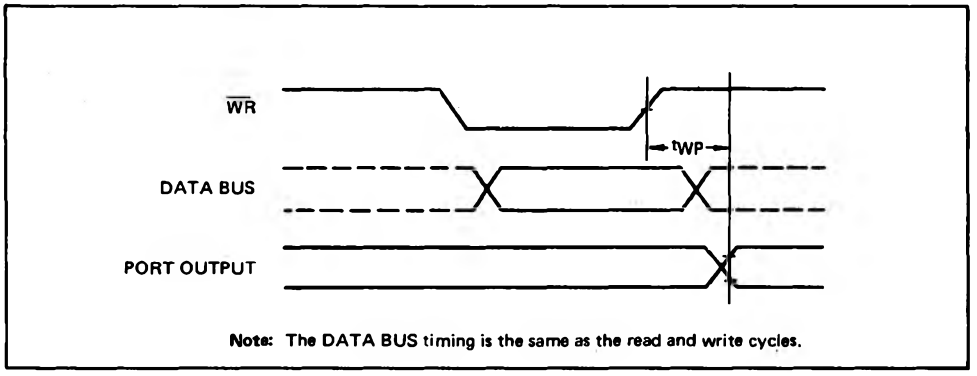
Strobe Output Mode



Basic Input Mode

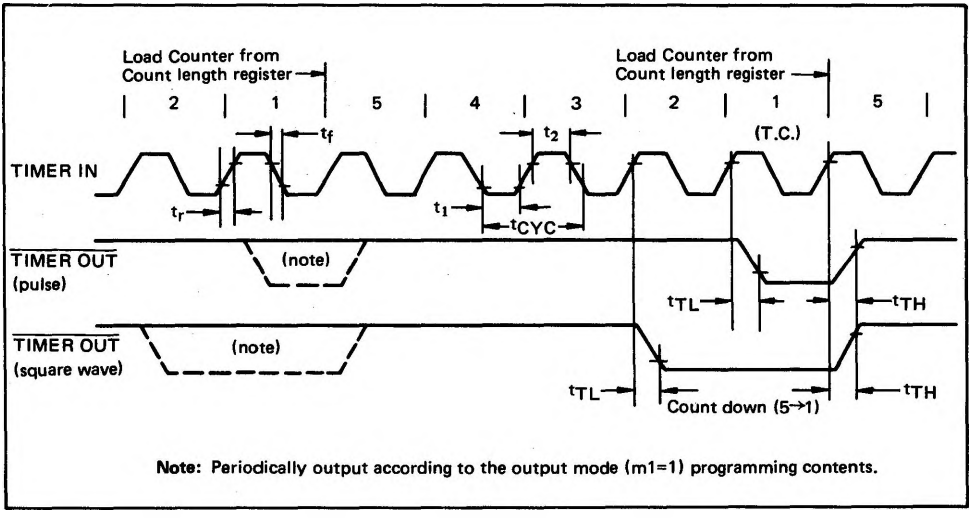


Basic Output Mode



Note: The DATA BUS timing is the same as the read and write cycles.

Timer Waveforms



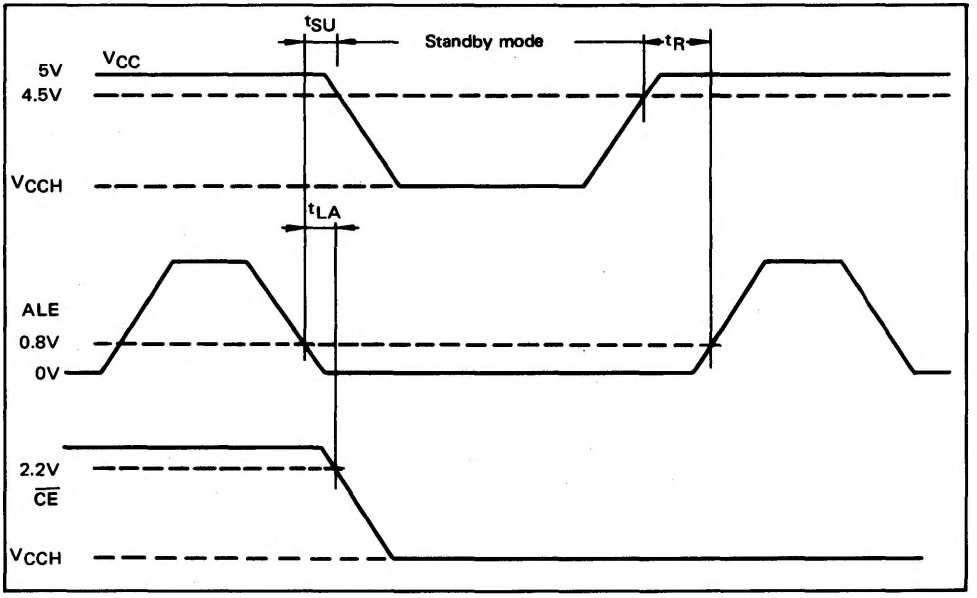
Note: Periodically output according to the output mode (m1=1) programming contents.

RAM DATA HOLD CHARACTERISTICS AT LOW SUPPLY VOLTAGE

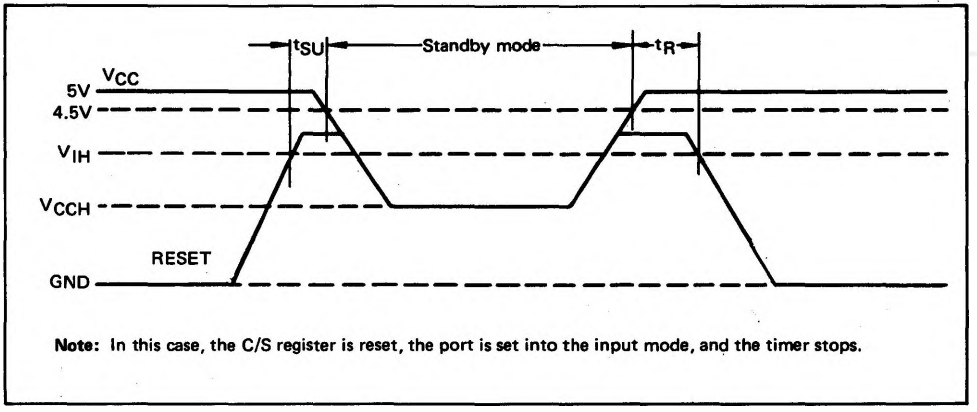
Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Data Holding Supply Voltage	V_{CCH}	V_{IN} = 0V or V_{CC}, ALE = 0V	2.0	–	–	V
Data Holding Supply Current	I_{CCH}	V_{CC} = V_{CCH}, ALE = 0 V_{IN} = 0V or V_{CC}	–	0.05	20	μ
Set-up Time	t_{SU}		30	–	–	ns
Hold Time	t_R		20	–	–	ns

Two ways to place device in standby mode:

(1) Method using $\overline{CE}$



(2) Method using RESET



Note: In this case, the C/S register is reset, the port is set into the input mode, and the timer stops.

PIN FUNCTIONS

Symbol	Function
RESET	A high level input to this pin resets the chip, places all three I/O ports in the input mode, resets all output latches and stops timer.
ALE	Negative going edge of the ALE (Address Latch Enable) input latches $AD_{0\sim7}$, IO/$\overline{M}$, and CE signals into the respective latches.
$AD_{0\sim7}$	Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus depending on the state of the WRITE or READ input.
$\overline{CE}$	When the CE input is high, both read and write operations to the chip are disabled.
IO/$\overline{M}$	A high level input to this pin selects the internal I/O functions, and a low level selects the memory.
$\overline{RD}$	If this pin is low, data from either the memory or ports is read onto the $AD_{0\sim7}$ lines depending on the state of the IO/$\overline{M}$ line.
$\overline{WR}$	If this pin is low, data on lines $AD_{0\sim7}$ is written into either the memory or into the selected port depending on the state of the IO/$\overline{M}$ line.
$PA_{0\sim7}$ ($PB_{0\sim7}$)	General-purpose I/O pins. Input/output directions can be determined by programming the command/status (C/S) register.
$PC_{0\sim5}$	Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions: PC0: A INTR (port A interrupt) PC1: A $\overline{BF}$ (port A full) PC2: $\overline{A\ STB}$ (port A strobe) PC3: B INTR (port B interrupt) PC4: B $\overline{BF}$ (port B buffer full) PC5: $\overline{B\ STB}$ (port B strobe)
TIMER IN	Input to the counter/timer
$\overline{TIMER\ OUT}$	Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output depending on the programmed control status.
V_{CC}	3—6V power supply
GND	GND

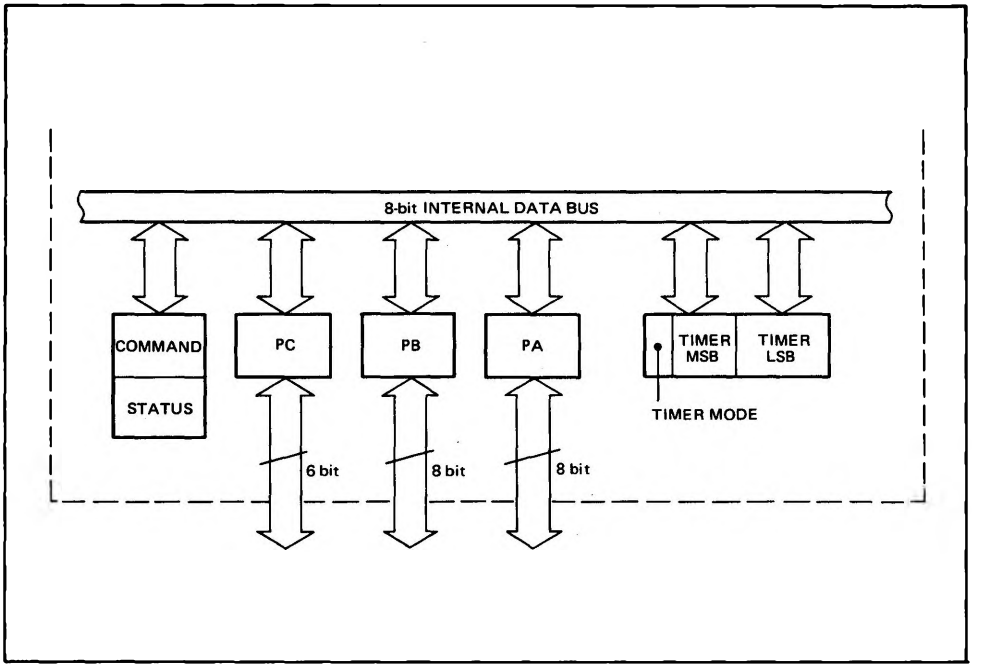
OPERATION

Description

MSM81C55RS/GS has 3 functions as described below.

- 2K bit static RAM (256 words x 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

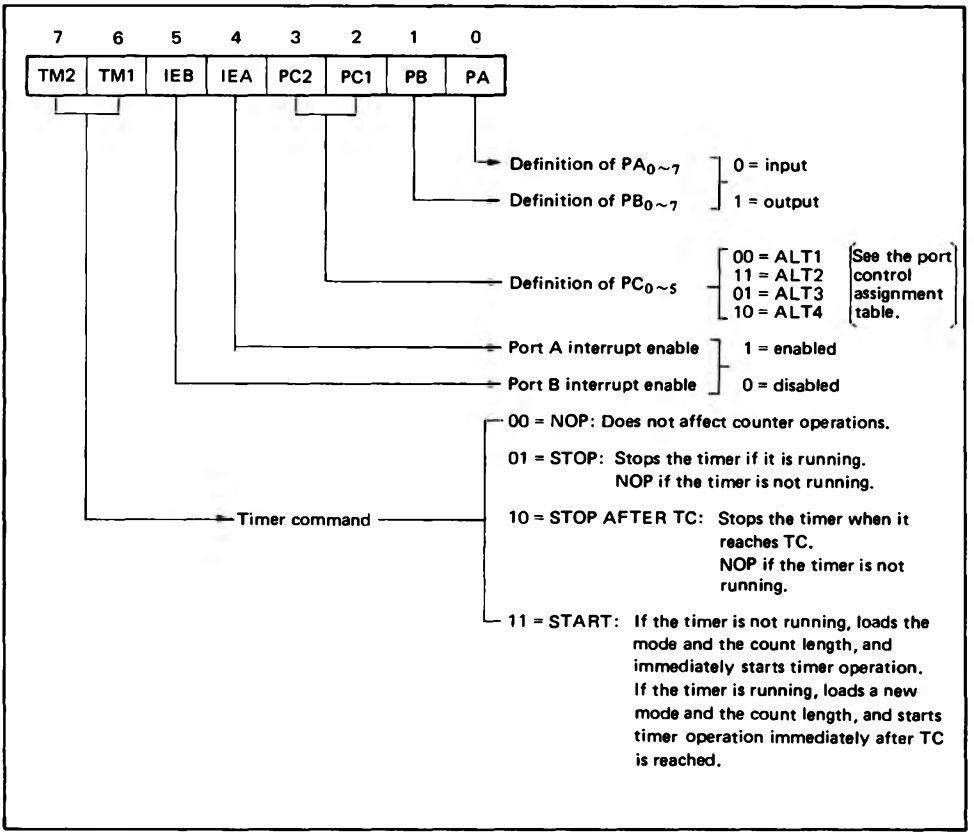
The internal register is shown in the figure below, and the I/O addresses are described in the table below.



I/O Address								Selecting Register
A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	x	x	0	0	0	Internal command/status register
x	x	x	x	x	0	0	1	Universal I/O port A (PA)
x	x	x	x	x	0	1	0	Universal I/O port B (PB)
x	x	x	x	x	0	1	1	I/O port C (PC)
x	x	x	x	x	1	0	0	Timer count lower position 8 bits (LSB)
x	x	x	x	x	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

x: Don't care.

(1) Programming the Command/Status (C/S) Register
The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:

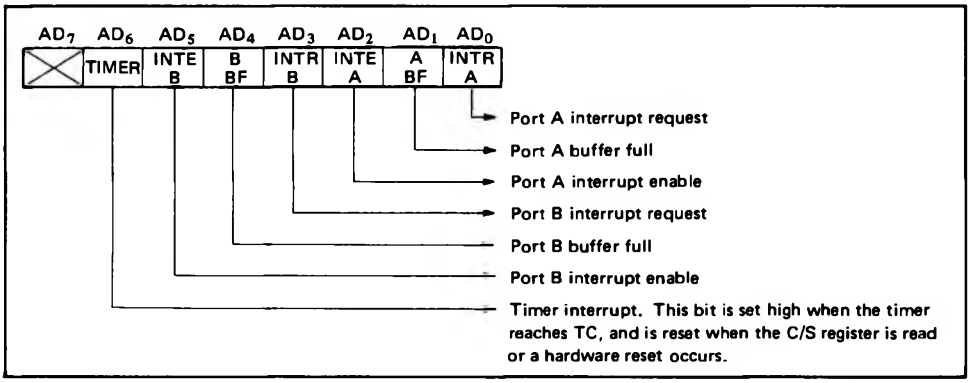


Port Control Assignment Table

Pin	ALT1	ALT2	ALT3	ALT4
PC_0	Input port	Output port	A INTR	A INTR
PC_1	Input port	Output port	A BF	A BF
PC_2	Input port	Output port	A STB	A STB
PC_3	Input port	Output port	Output port	B INTR
PC_4	Input port	Output port	Output port	B BF
PC_5	Input port	Output port	Output port	B STB

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:



(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register: xxxxx001

I/O address of the PB register: xxxxx010

(4) PC Register

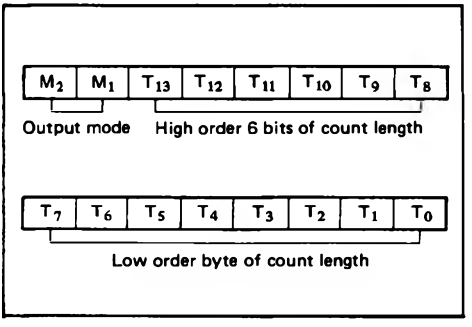
The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit down counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length and bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.



M_2	M_1	
0	0	Outputs a low-level signal in the latter half (Note 1) of a count period.
0	1	Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached.
1	0	Outputs a pulse when the TC value is reached.
1	1	Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning.

Note 1: When counting an asymmetrical value such as (9), a high level is output during the first period of five, and a low level is output during the second period of four.

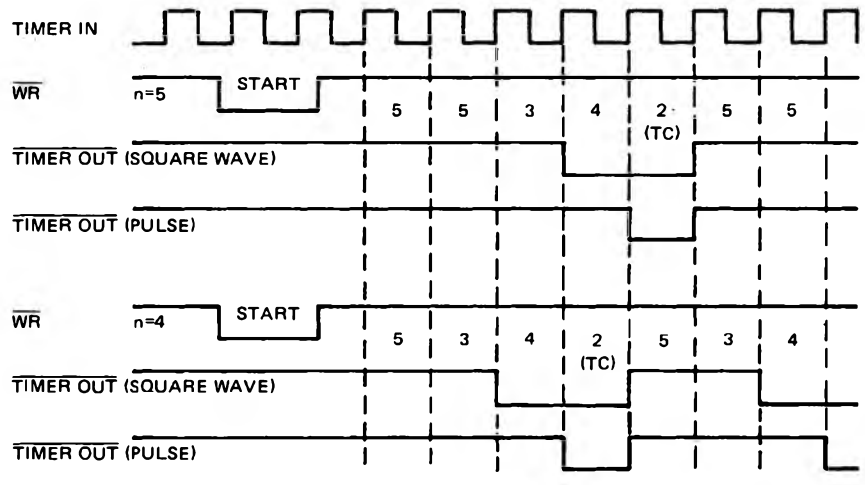
Note 2: If an internal counter of the MSM81C-55RS/GS receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

Note that while the counter is counting, you may load a new count and mode into the CLR. Before the new count and mode will be used by the counter, you must issue a START command to the counter.

Please note the timer circuit on the 81C55 is designed to be a square-wave timer, not a event counter. To achieve this, it counts down by twos twis in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulse received. After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulse required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. STOP the counter
2. Read in the 16 bit value from the count registers.
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add ½ of the full original count (½ full count-1 if full count is odd).

Note: If you started with an odd count and you read the count registers before the third count pulse occurs, you will not be able to recognize whether one or two counts has occurred. Regardless of this, the 81C55 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.



Note: n is the value set in the CLR.
Figures in the diagram refer to counter value.

(6) Standby Mode (see page 7)

The MSM81C55RS/GS is placed in standby mode when the high level at $\overline{\text{CE}}$ input is latched during the negative going edge of ALE. All input ports and the timer input should be pulled up or down to either V_{CC} or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.