OKI semiconductor

MSM82C37A-5RS/GS/JS

PROGRAMMABLE DMA CONTROLLER

GENERAL DESCRIPTION

The MSM82C37A-5RS/GS/JS, DMA (Direct Memory Access) controller is capable of high-speed data transfer without CPU intervention and is used as a peripheral device in microcomputer systems. The device features four independent programmable DMA channels.

Due to the use of silicon gate CMOS technology, standby current is 10 μA (max.), and power consumption is as low as 10 mA (max.) when a 5 MHz clock is generated.

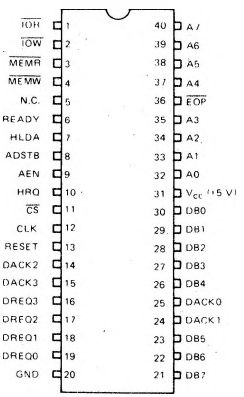
All items of AC characteristics are compatible with intel 8237A-5.

FEATURES

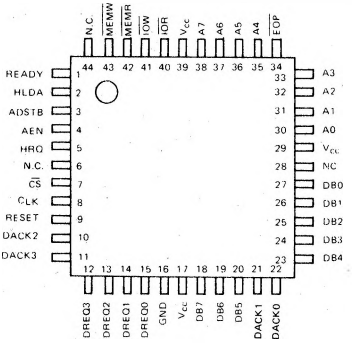
- Maximum operating frequency of 5 MHz(V_{CC}= 5 V ± 10%)
- High-speed operation at very low power consumption due to silicon gate CMOS technology
- Wide power supply voltage range of 3 to 6 V
- Wide operating temperature range from −40° to +85°C
- 4-channels independent DMA control
- DMA request masking and programming
- DMA request priority function
- DREQ and DACK input/output logic inversion
- DMA address increment/decrement selection
- Memory-to-Memory Transfers
- Channel extension by cascade connection
- DMA transfer termination by $\overline{EOP}$ input
- 40-pin DIP (MSM82C37A-5RS)
- 44-pin PLCC package (MSM82C37A-5JS)
- Intel 8237A-5 compatibility
- TTL Compatible

PIN CONNECTIONS

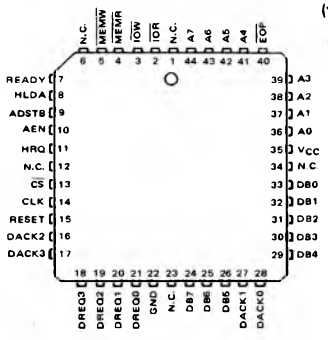
40-pin plastic DIP (top view)



44-pin plastic flat-package (top view)

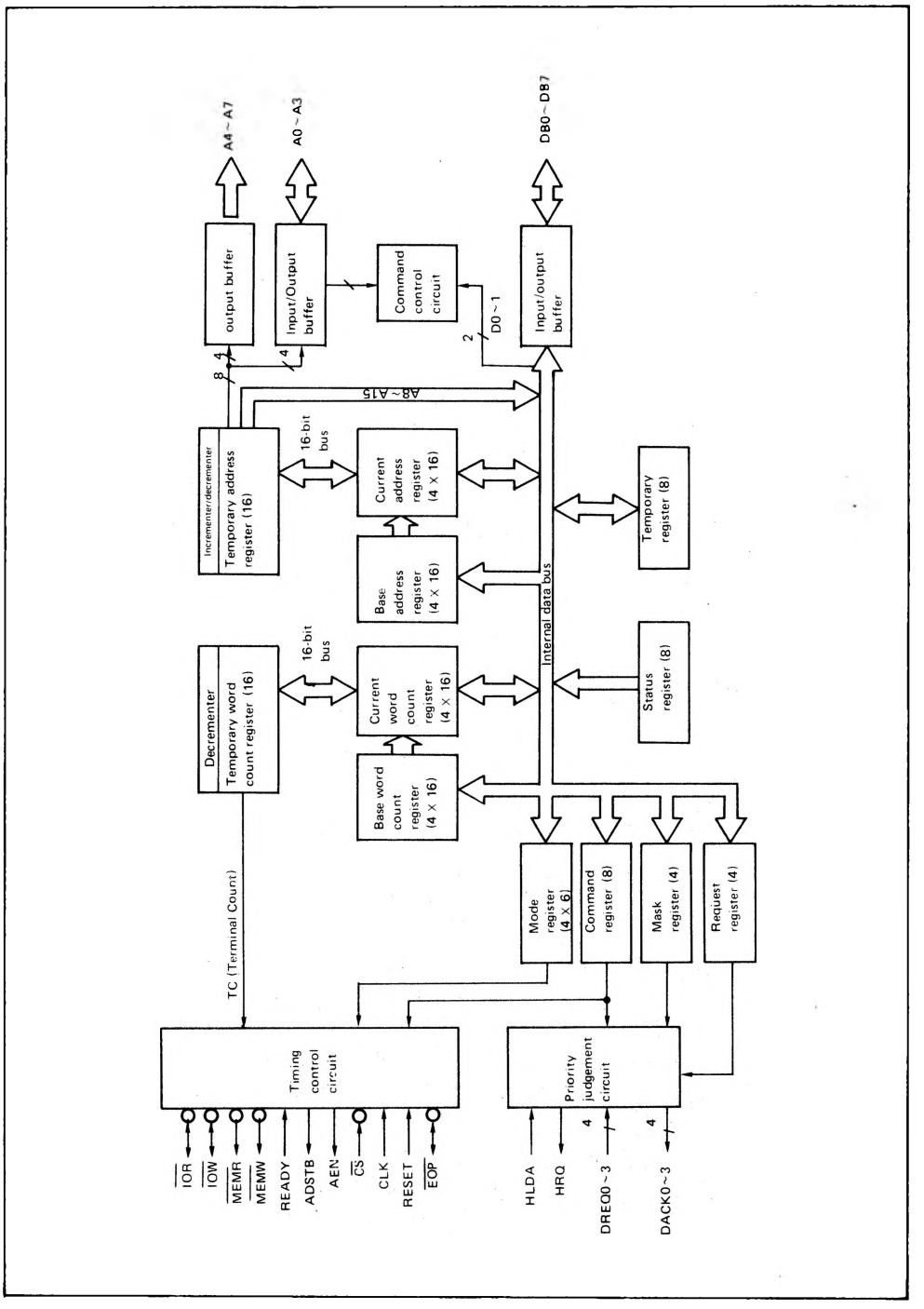


44-PIN PLCC PACKAGE (top view)



Note: N.C. (No Connection)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating			Unit
			MSM82C37A-5RS	MSM82C37A5GS	MSM82C37A-5JS	
Power supply voltage	V_{CC}	with respect to GND	−0.5 ~ +7			V
Input voltage	V_{IN}		−0.5 ~ V_{CC} + 0.5			V
Output voltage	V_{OUT}		−0.5 ~ V_{CC} + 0.5			V
Storage temperature	T_{stg}		−55 ~ +150			°C
Power dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGES

Parameter	Symbol	Range	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Maximum	Typical	Minimum	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature	T_{OP}	−40	+25	+85	°C
"L" input voltage	V_{IL}	-0.5	–	+0.8	V
"H" input voltage	V_{IH}	2.2	–	V_{CC} + 0.5	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Maximum	Typical	Minimum	Unit
"L" output voltage	V_{OL}	IOL = 3.2 mA	V_{CC} = 4.5 V ~ 5.5V, Ta = −40°C ~ +85°C	—	—	0.4	V
"H" output voltage	V_{OH}	IOH = −1.0 mA		3.7	—	—	V
Input leak current	ILI	0 V ≦ V_{IN} ≦ V_{CC}		−10	—	10	μA
Output leak current	ILO	0 V ≦ V_{OUT} ≦ V_{CC}		−10	—	10	μA
Average power supply current during operations	ICC	Input frequency 5 MHz, whenRESET V_{IN} = 0 V/V_{CC}, C_L = 0 pF		—	—	10	mA
Power supply current in standby mode	ICCS	HLDA = 0 V, VIL = 0 V, VIH = VCC		—	—	10	μA

AC CHARACTERISTICS

DMA (MASTER) MODE

(Ta = -40 ~ +85°C, V_{CC} = 4.5 ~ 5.5V)

Symbol	Item	MIN	MAX	Unit	Comments
TAEL	Delay time from CLK falling edge up to AEN leading edge	—	200	ns	—
TAET	Delay time from CLK rising edge up to AEN trailing edge	—	130	ns	—
TAFAB	Delay time from CLK rising edge up to address floating status	—	90	ns	—
TAFC	Delay time from CLK rising edge up to read/write signal floating status	—	120	ns	—
TAFDB	Delay time from CLK rising edge up to data bus floating status	—	170	ns	—
TAHR	Address valid hold time to read signal trailing edge	TCY-100	—	ns	—
TAHS	Data valid hold time to ADSTB trailing edge	30	—	ns	—
TAHW	Address valid hold time to write signal trailing edge	TCY-50	—	ns	—
TAK	Delay time from CLK falling edge up to active DACK	—	170	ns	(Note 3)
	Delay time from CLK rising edge up to $\overline{EOP}$ leading edge	—	170	ns	(Note 5)
	Delay time from CLK rising edge up to $\overline{EOP}$ trailing edge	—	170	ns	—
TASM	Time from CLK rising edge up to address valid	—	170	ns	—
TASS	Data set-up time to ADSTB trailing edge	100	—	ns	—
TCH	Clock high-level time	68	—	ns	(Note 6)

Symbol	Item	MIN	MAX	Unit	Comments
TCL	Clock low-level time	68	—	ns	(Note 6)
TCY	CLK cycle time	200	—	ns	
TDCL	Delay time from CLK rising edge to read/write signal leading edge	—	190	ns	(Note 2)
TDCTR	Delay time from CLK rising edge to read signal trailing edge	—	190	ns	(Note 2)
TDCTW	Delay time from CLK rising edge to write signal trailing edge	—	130	ns	(Note 2)
TDQ	Delay time from CLK rising edge to HRQ valid	—	120	ns	—
TEPS	$\overline{EOP}$ leading edge set-up time to CLK falling edge	40	—	ns	—
TEPW	$\overline{EOP}$ pulse width	220	—	ns	—
TFAAB	Delay time from CLK rising edge to address valid	—	170	ns	—
TFAC	Time from CLK rising edge up to active read/write signal	—	150	ns	—
TFADB	Delay time from CLK rising edge to data valid	—	200	ns	—
THS	HLDA valid set-up time to CLK rising edge	75	—	ns	—
TIDH	Input data hold time to $\overline{MEMR}$ trailing edge	0	—	ns	—
TIDS	Input data set-up time to $\overline{MEMR}$ trailing edge	170	—	ns	—
TODH	Output data hold time to $\overline{MENW}$ trailing edge	10	—	ns	—
TODV	Time from output data valid to $\overline{MEMW}$ trailing edge	125	—	ns	—
TQS	DREQ set-up time to CLK falling edge	0	—	ns	(Note 3)
TRH	READY hold time to CLK falling edge	20	—	ns	—
TRS	READY set-up time to CLK falling edge	60	—	ns	—
TSTL	Delay time from CLK rising edge to ADSTB leading edge	—	130	ns	—
TSTT	Delay time from CLK rising edge to ADSTB trailing edge	—	90	ns	—

SLAVE MODE

($Ta = -40 \sim +85°C$, $V_{CC} = 4.5 \sim 5.5V$)

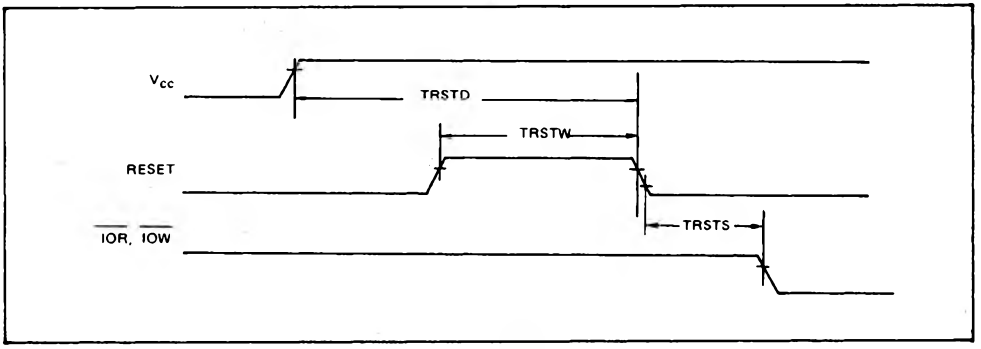
Symbol	Item	MIN	MAX	Unit	Comments
TAR	Time from address valid or $\overline{CS}$ leading edge to $\overline{IOR}$ leading edge	50	—	ns	—
TAW	Address valid set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TCW	$\overline{CS}$ leading edge set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TDW	Data valid set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TRA	Address or $\overline{CS}$ hold time to $\overline{IOR}$ trailing edge	0	—	ns	—
TRDE	Data access time to $\overline{IOR}$ leading edge	—	140	ns	—
TRDF	Delay time to data floating status from $\overline{IOR}$ trailing edge	0	70	ns	—
TRSTD	Supply power leading edge set-up time to RESET trailing edge	500	—	ns	—
TRSTS	Time to first active $\overline{IOR}$ or $\overline{IOW}$ from RESET trailing edge	2TCY	—	ns	—
TRSTW	RESET pulse width	300	—	ns	—
TRW	$\overline{IOR}$ pulse width	200	—	ns	—
TWA	Address hold time to $\overline{IOW}$ trailing edge	20	—	ns	—
TWC	$\overline{CS}$ trailing edge hold time to $\overline{IOW}$ trailing edge	20	—	ns	—
TWD	Data hold time to $\overline{IOW}$ trailing edge	30	—	ns	—
TWWS	$\overline{IOW}$ pulse width	160	—	ns	—

Note:

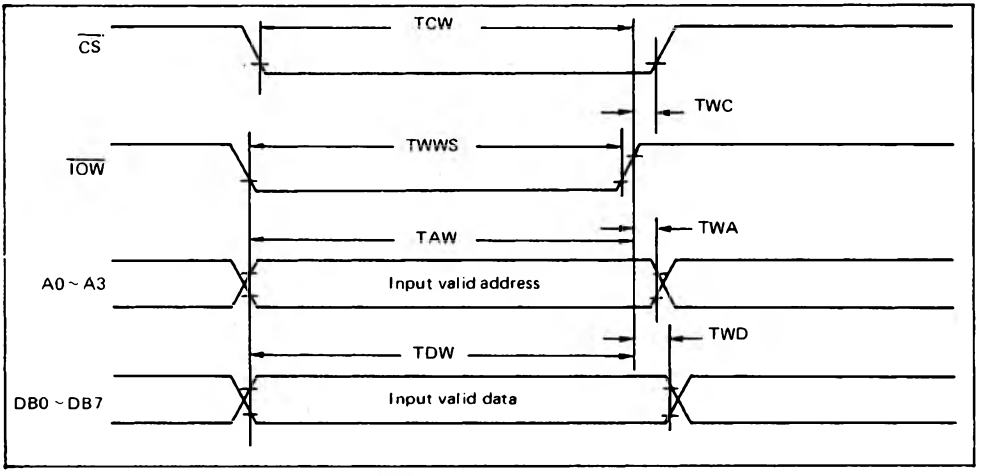
1. Output load capacitance of 150 (pF).
2. $\overline{IOW}$ and $\overline{MEMW}$ pulse widths of TCY-100 (ns) for normal writing, and 2TCY-100 (ns) for extended writing. $\overline{IOR}$ and $\overline{MEMR}$ pulse widths of 2TCY-50 (ns) for normal timing, and TCY-50 (ns) for compressed timing.
3. DREQ and DACK signal active level can be set to either low or high. In the timing chart, the DREQ signal has been set to active-high, and the DACK signal to active-low.
4. When the CPU executes continuous read or write in programming mode, the interval during which the read or write pulse becomes active must be set to at least 400 ns.
5. $\overline{EOP}$ is an open drain output. The value given is obtained when a 2.2 kohm pull-up resistance is connected to VCC.
6. Rise time and fall time is less than 10 ns.
7. Waveform measurement points for both input and output signals are 2.2 V for HIGH and 0.8 V for LOW, unless otherwise noted.

TIME CHART

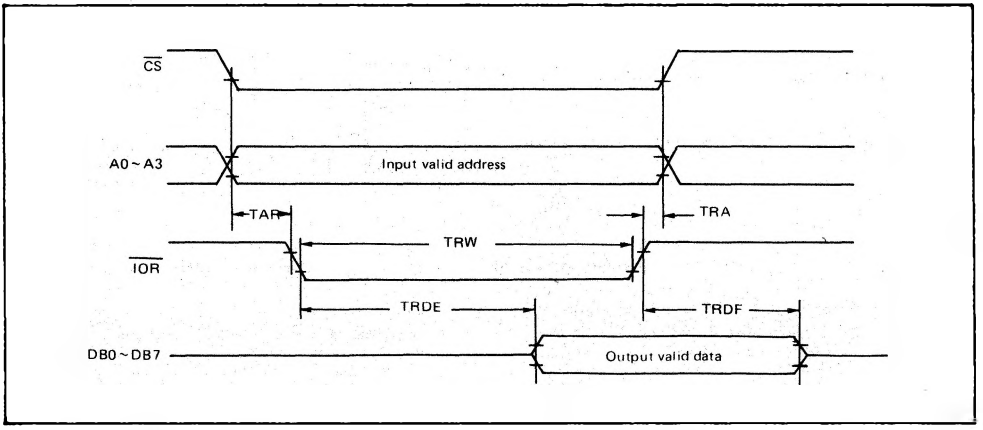
RESET TIMING



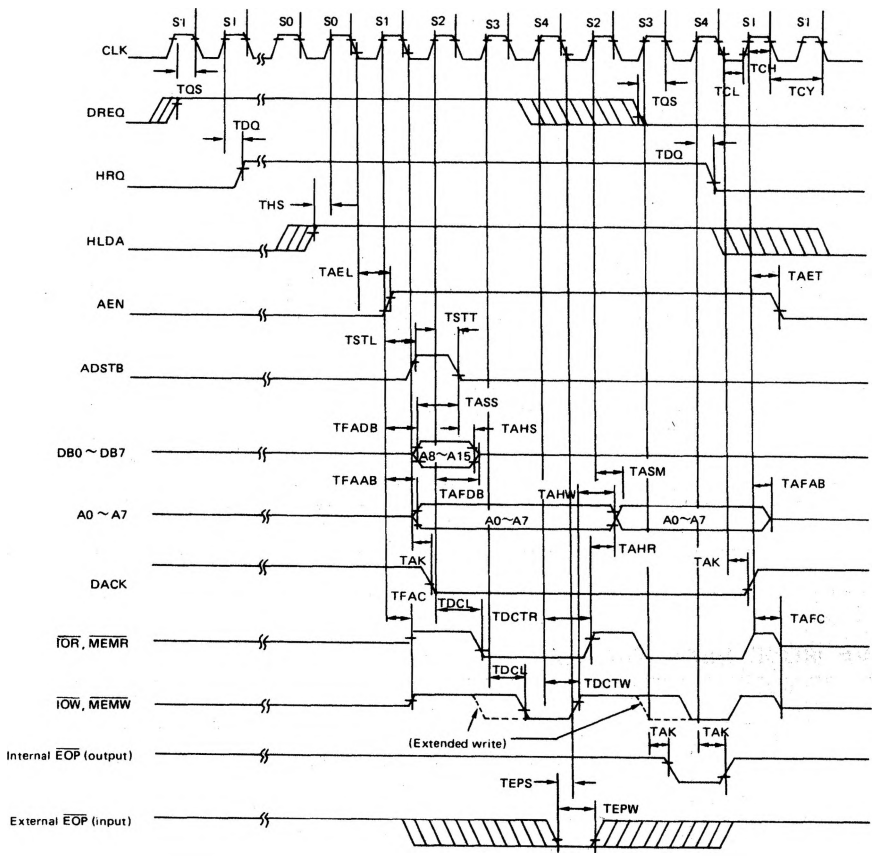
SLAVE MODE WRITE TIMING



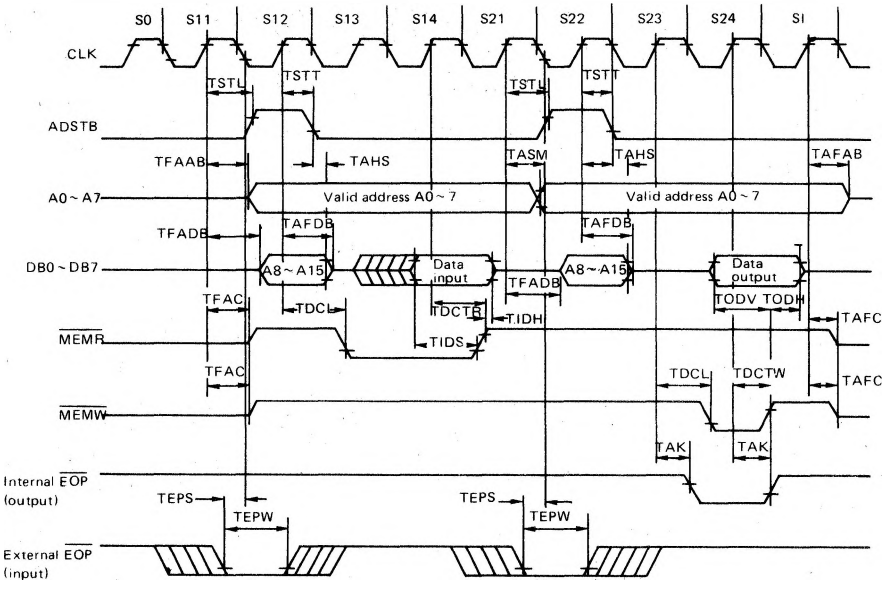
SLAVE MODE READ TIMING



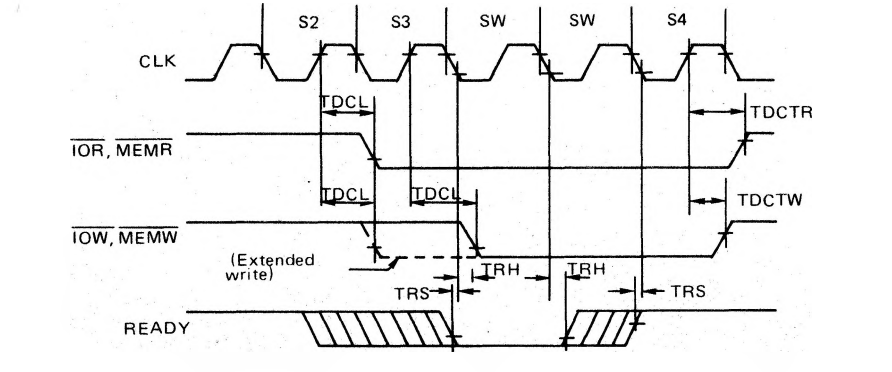
DMA TRANSFER TIMING



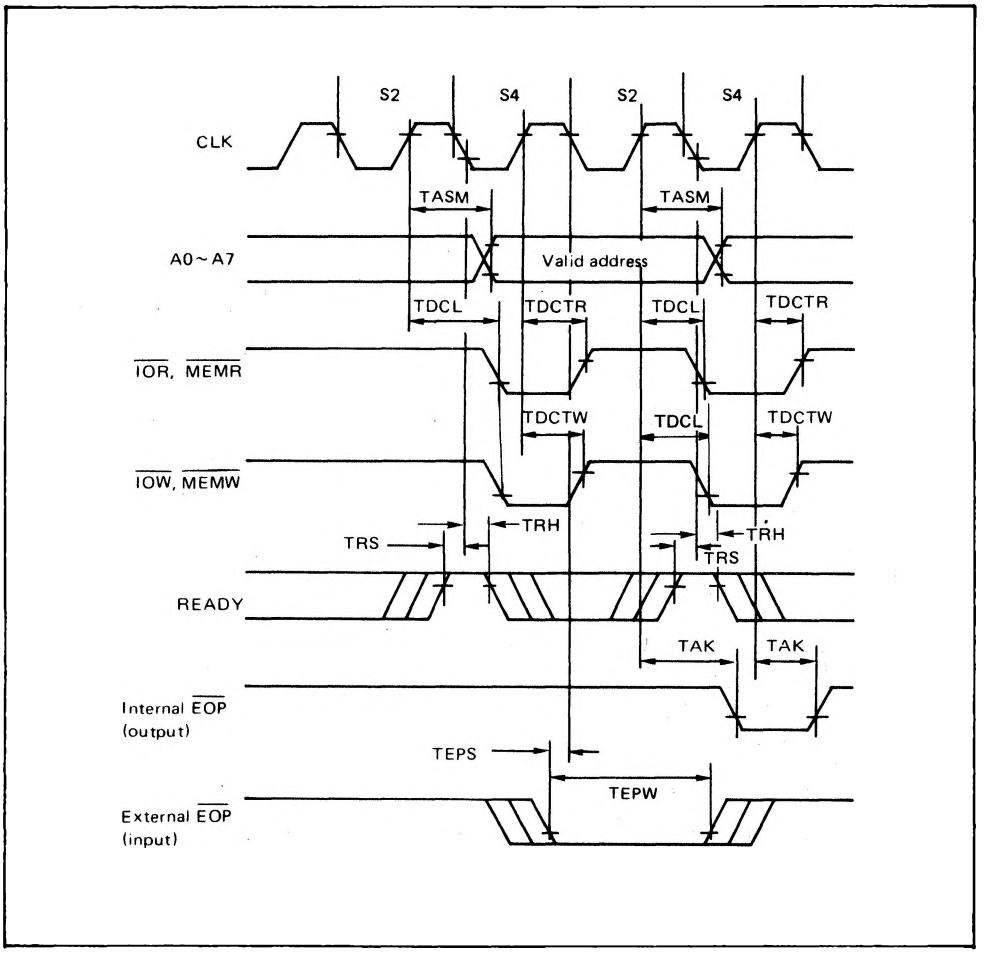
MEMORY TO MEMORY TRANSFER TIMING



READY TIMING



COMPRESSED TRANSFER TIMING



PIN FUNCTIONS

Symbol	Pin name	Input/ output	Function
V_{CC}	Power		+5 V power supply.
GND	Ground		Ground (0 V) connection.
CLK	Clock	Input	Control of MSM82C37A-5 internal operations and data transfer speed.
$\overline{CS}$	Chip select	Input	$\overline{CS}$ is active-low input signal used for the CPU to select the MSM82C37A-5 as an I/O device in an idle cycle.
RESET	Reset	Input	RESET is active-high asynchronous input signal used to clear command, status, request, temporary registers, and first/last F/F, and to set mask register. The MSM82C37A-5 enters an idle cycle following a RESET.
READY	Ready	Input	The read or write pulse width can be extended to accomodate slow access memories and I/O devices when this input is switched to low level. Note this input must not change within the prescribed set-up/hold time.
HLDA	Hold acknowledge	Input	HLDA is active-high input signal used to indicate that system bus control has been released when a hold request is received by the CPU.
DREQ0 ~ DREQ3	DMA request 0 ~ 3 channels	Input	DREQ is asychronous DMA transfer request input signals. Although these pins are switched to active-high by reset, they can be programmed to become active-low. DMA requests are received in accordance with a prescribed order of priority. DREQ must be held until DACK becomes active.
DB0 ~ DB7	Data bus 0 ~ 7	Input/ output	DB is bidirectional three-state signals connected to the system data bus, and which is used as an input/output of MSM82C37A-5 internal registers during idle cycles, and as an output of the eight higher order bits of transfer addresses during active cycles. Also used as input and output of transfer data during memory-memory transfers.
$\overline{IOR}$	I/O read	Input/ output	$\overline{IOR}$ is active-low bidirectional three-state signal used as an input control signal for CPU reading of MSM82C37A-5 internal registers during idle cycles, and as an output control signal for reading I/O device transfer data in writing transfers during active cycles.
$\overline{IOW}$	I/O write	Input/ output	$\overline{IOW}$ is active-low bidirectional three-state signal used as an input control signal for CPU writing of MSM82C37A-5 internal registers during idle cycles, and as an output control signal for writing I/O device transfer data in writing transfers during active cycles.

Symbol	Pin name	Input/ output	Function
$\overline{EOP}$	End of process	Input/ output	$\overline{EOP}$ is active-low bidirectional three-state signal. Unlike other pins, this pin is an N-channel open drain. During DMA operations, a low-level output pulse is obtained from this pin if the channel word count changes from 0000H to FFFFH. And DMA transfers can be terminated by pulling the $\overline{EOP}$ input to low level. Both of these actions are called terminal count (TC). When an internal or external $\overline{EOP}$ is generated, the MSM82C37A-5 terminates the transfer and resets the DMA request. When the $\overline{EOP}$ pin is not used, it is necessary to hold the pin at high level by pull-up resistance to prevent the input of an $\overline{EOP}$ by error. Also note that the $\overline{EOP}$ function cannot be satisfied in cascade mode.
A0 ~ A3	Address 0 ~ 3	Input/ output	A0~A3 is bidirectional three-state signals used as input signals for specifying the MSM82C37A-5 internal register to be accessed by the CPU during idle cycles, and as an output the four lower order bits of the transfer address during active cycles.
A4 ~ A7	Address 4 ~ 7	Output	A4~A7 is three-state signals used as an output the four higher order bits of the transfer address during active cycles.
HRQ	Hold request	Output	HRQ is active-high signal used as an output of hold request to the CPU for system data bus control purposes. After HRQ has become active, at least one clock cycle is required before HLDA becomes active.
DACK0 ~ DACK3	DMA acknowledge 0 ~ 3 channels	Output	DACK is output signals used to indicate that DMA transfer to peripheral devices has been permitted. (Available in each channel.) Although these pins are switched to active-low when reset, they can be programmed to become active-high. Note that there is no DACK output signal during memory-memory transfers.
AEN	Address enable	Output	AEN is active-high output signal used to indicate that output signals sent from the MSM82C37A-5 to the system are valid. And in addition to enabling external latch to hold the eight higher order bits of the transfer address, this signal is also used to disable other system bus buffers.

Symbol	Pin name	Input/ output	Function
ADSTB	Address strobe	Output	ADSTB is active-high signal used to strobe the eight higher order bits of the transfer address by external latch.
$\overline{\text{MEMR}}$	Memory read	Output	$\overline{\text{MEMR}}$ is active-low three-state output signal used as a control signal in reading data from memory during read transfers and memory-memory transfers.
$\overline{\text{MEMW}}$	Memory write	Output	$\overline{\text{MEMW}}$ is active-low three-state output signal used as a control signal in writing data into memory during write transfers and memory-memory transfers.

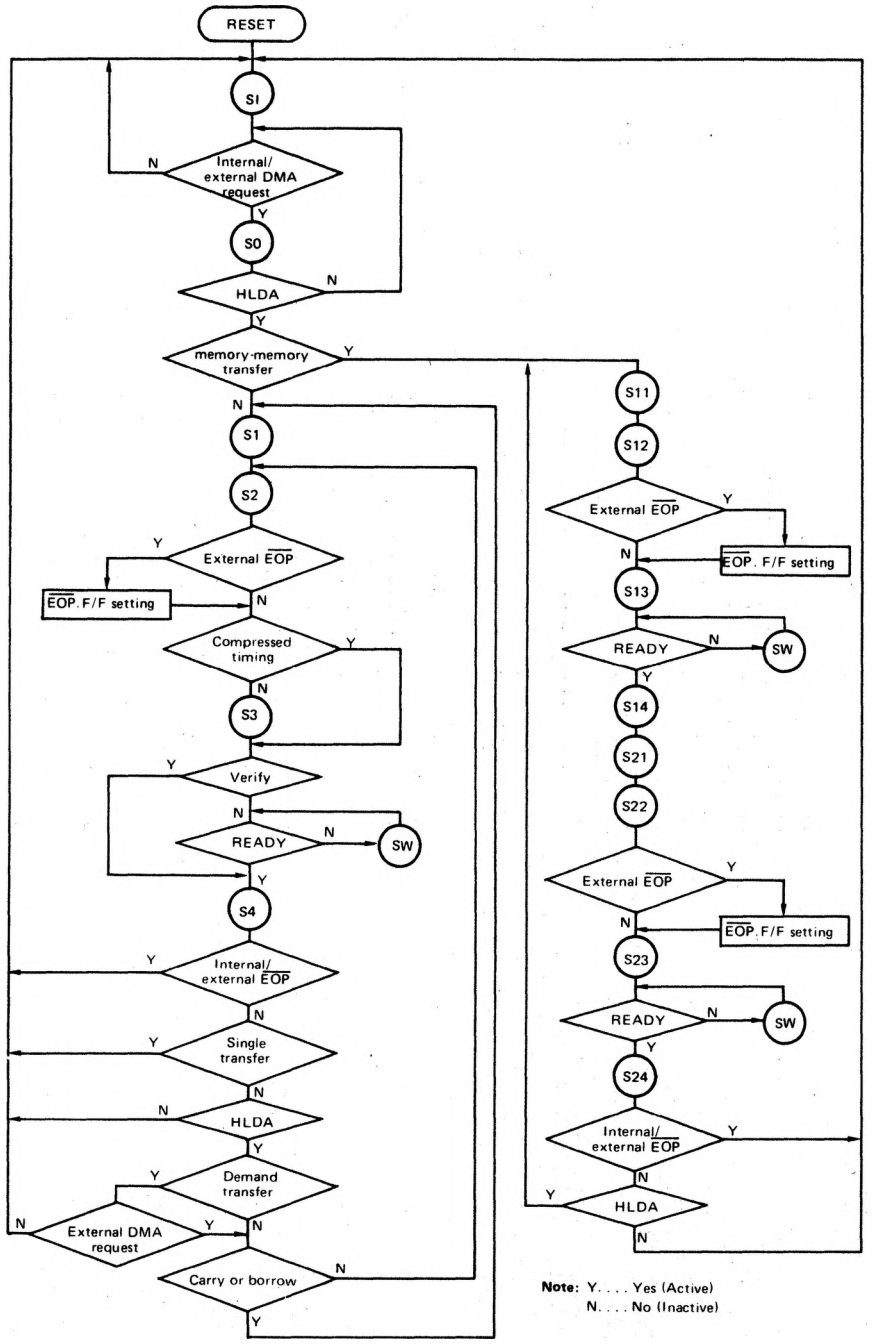


Fig. 1 DMA operation state transition diagram

OUTLINE OF FUNCTIONS

The MSM82C37A-5 consists of five blocks = three logic sections, an internal register section, and a counter section.

The logic sections include a timing control block where the internal timing and external control signals are generated, a command control block where each instruction from the CPU is decoded, and a priority decision block where the order of DMA channel priority is determined. The purpose of the internal register section is to hold internal states and instructions from the CPU, while the counter section computes addresses and word counts.

DESCRIPTION OF OPERATIONS

The MSM82C37A-5 operates in two cycles (called the idle and active cycles) which are divided into independent states. Each state is commenced by a clock falling edge and continues for a single clock cycle. The transition from one state to the next in DMA operations is outlined in Figure 1.

IDLE CYCLE

The idle cycle is entered from the SI state when there is no valid DMA request on any MSM82C37A-5 channel. During this cycle, DREQ and $\overline{CS}$ inputs are monitored during each cycle. When a valid DMA request is then received, an active cycle is commenced. And if the HLDA and $\overline{CS}$ inputs are at low level, a programming state is started with MSM82C37A-5 reading or writing executed by $\overline{IOR}$ or $\overline{IOW}$. Programming details are described later.

ACTIVE CYCLE

If a DMA request is received in an unmasked channel while the MSM82C37A-5 is in an idle cycle, or if a software DREQ is generated, the HRQ is changed to high level to commence an active cycle. The initial state of an active cycle is the S0 state which is repeated until the HLDA input from the CPU is changed to high level. (But because of internal operational reasons, a minimum of one clock cycle is required for the HLDA is be changed to high level by the CPU after the HRQ has become high level. That is, the S0 state must be repeated at least twice.)

After the HLDA has been changed to high level, the S0 state proceeds to operational states S1 thru S4 during I/O-memory transfers, or to operational states S11 thru S14 and S21 thru S24 during memory-memory transfers.

If the memory or I/O device cannot be accessed within the normal timing, an SW state (wait state) can be inserted by a READY input to extend the timing.

DESCRIPTION OF TRANSFER TYPES

MSM82C37A-5 transfers between an I/O and memory devices, or transfers between memory devices. The three types of transfers between I/O and memory devices are read, write, and verify.

I/O-MEMORY TRANSFERS

The operational states during an I/O-memory transfer are S1, S2, S3, and S4.

In the S1 state, an AEN output is changed to high level to indicate that the control signal from the MSM82C37A-5 is valid. The eight lower order bits of the transfer address are obtained from A0 thru A7, and the eight higher order bits are obtained from DB0 thru DB7. The ADSTB output is changed to high level at this time to set the eight higher order bits in an external address latch, and the DACK output is made active for the channel where the DMA request is acknowledged. Where there is no change in the eight higher bit transfer address during demand and block mode transfers, however, the S1 state is omitted.

In the S2 state, the $\overline{IOR}$ or $\overline{MEMR}$ output is changed to low level.

In the S3 state, $\overline{IOW}$ or $\overline{MEMW}$ is changed to low level. Where compressed timing is used, however, the S3 state is omitted.

The S2 and S3 states are I/O or memory input/output timing control states.

In the S4 state, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, and $\overline{MEMW}$ are changed to high level, and the word count register is decremented by 1 while the address register is incremented (or decremented) by 1. This completes the DMA transfer of one word.

Note that in I/O-memory transfers, data is transferred directly without being taken in by the MSM82C37A-5. The differences in the three types of I/O-memory transfers are indicated below.

READ TRANSFER

Data is transferred from memory to the I/O device by changing $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ to low level. $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$ are kept at high level during this time.

WRITE TRANSFER

Data is transferred from the I/O device to memory by changing $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$ to low level. $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ are kept at high level during this time.

Note that writing and reading in these write and read transfers are with respect to the memory.

VERIFY TRANSFER

Although verify transfers involve the same operations as write and read transfers (such as transfer address generation and $\overline{\text{EOP}}$ input responses), they are in fact pseudo transfers where all I/O and memory reading/writing control signals are kept inactive. READY inputs are disregarded in verify transfers.

MEMORY-MEMORY TRANSFERS

Memory-memory transfers are used to transfer data blocks from one memory area to another.

Memory-memory transfers require a total of eight states to complete a single transfer four states (S11 thru S14) for reading from memory, and four states (S21 thru S24) for writing into memory. These states are similar to I/O-memory transfer states, and are distinguished by using two-digit numbers.

In memory-memory transfers, channel 0 is used for reading data from the source area, and channel 1 is used for writing data into the destination area. During the initial four states, data specified by the channel 0 address is read from the memory when MEMR is made active, and is taken in the MSM82C37A-5 temporary register. Then during the latter four states, the data in the temporary register is written in the address specified by channel 1. This completes the transfer of one byte of data. With channel 0 and channel 1 addresses subsequently incremented (or decremented) by 1, and channel 0, 1 word count decremented by 1, this operation is repeated. The transfer is terminated when the word count reaches FFFF(H) from OOOO(H), or when an $\overline{\text{EOP}}$ input is applied from an external source. Note that there is no DACK output signal during this transfer.

The following preparations in programming are requiring to enable memory-memory transfers to be started.

COMMAND REGISTER SETTING

Memory-memory transfers are enabled by setting bit 0. Channel 0 address can be held for all transfers by setting bit 1. This setting can be used to enable 1-word contents of the source area to be written into the entire destination area.

MODE REGISTER SETTING

The transfer type destination is disregarded in channels 0 and 1. Memory-memory transfers are always executed in block transfer mode.

REQUEST REGISTER SETTING

Memory-memory transfers are started by setting the channel 0 request bit.

MASK REGISTER SETTING

Mask bits for all channels are set to prevent selection of any other channel apart from channel 0.

WORD COUNT REGISTER SETTING

The channel 1 word count is validated, while the channel 0 word count is disregarded.

In order to autoinitialize both channels, it is necessary to write the same values into both word count registers.

DESCRIPTION OF OPERATION MODES

SINGLE TRANSFER MODE

In single transfer mode, only one word is transferred, and the addresses are incremented (or decremented) by 1 while the word count is decremented by 1. The HRQ is then changed to low level to return the bus control to the CPU. If DREQ remains active after completion of a transfer, the HRQ is changed to low level. After the HLDA is changed to low level by the CPU, and then changes the HRQ back to high level to commence a fresh DMA cycle. For this reason, a machine cycle can be inserted between DMA cycles by the CPU.

BLOCK TRANSFER MODE

Once a DMA transfer is started in block mode, the transfer is continued until terminal count (TC) status is reached.

If DREQ remains active until DACK becomes active, the DMA transfer is continued even if DREQ becomes inactive.

DEMAND TRANSFER MODE

The DMA transfer is continued in demand transfer mode until DREQ is no longer active, or until TC status is reached.

During a DMA transfer, intermediate address and word count values are held in the current address and current word count registers. Consequently, if the DMA transfer is suspended as a result of DREQ becoming inactive before TC status is reached, and the DREQ for that channel is then made active again, the suspended DMA transfer is resumed.

CASCADE TRANSFER MODE

When DMA transfers involving more than four channels are required, connecting a multiple number of MSM82C37A-5 devices in a cascade connection (see Figure 2) enables a simple system extension. This mode is set by setting the first stage MSM82C37A-5 channel to cascade mode. The DREQ and DACK lines for the first stage MSM82C37A-5 channel set to cascade mode are connected to the HRQ and HLDA lines of the respective MSM82C37A-5 devices in the second stage. The first stage MSM82C37A-5 DACK signal must be set to active-high, and the DREQ signal to active-low.

Since the first stage MSM82C37A-5 is only used functionally in determining the order of priority of each channel when cascade mode is set, only DREQ and DACK are used — all other inputs are disregarded. And since the system may be hung up if the DMA transfer is activated by software DREQ, do not set a software DREQ for channels where cascade mode has been set.

In addition to the dual stage cascade connection shown in Figure 2, triple stage cascade connections are possible with the second stage also set to cascade mode.

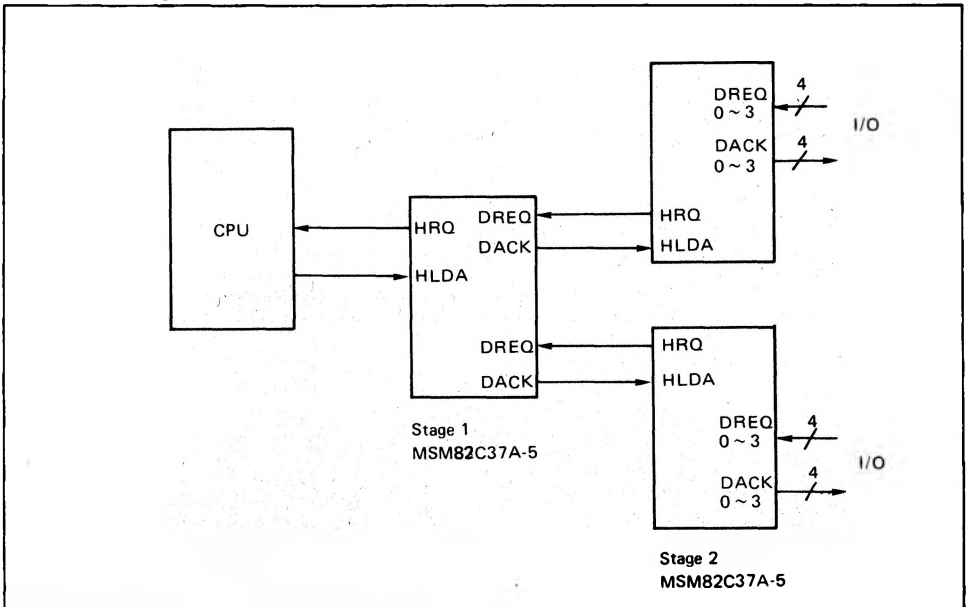


Fig. 2 MSM82C37A-5 cascade connection system

AUTOINITIALIZE MODE

Setting bit 4 of the mode register enables autoinitialization of that channel. Following TC generation, autoinitialize involves writing of the base address and the base word count register values in the respective current address and current word count registers. The same values as in the current registers are written in the base registers by the CPU, and are not changed during DMA transfers.

When a channel has been set to autoinitialize, that channel may be used in a second transfer without involving the CPU and without the mask bit being reset after the TC generation.

PRIORITY MODES

The MSM82C37A-5 makes use of two priority decision modes, and acknowledges the DMA channel of highest priority among the DMA requesting channels.

FIXED PRIORITY MODE

In fixed priority mode, channel 0 has the highest priority, followed by channel 1, 2, and 3 in that order.

ROTATING PRIORITY MODE

In rotating priority mode, the order of priority is changed so that the channel where the current DMA transfer has been completed is given lowest priority. This is to prevent any one channel from monopolizing the system. The fixed priority is regained immediately after resetting.

Table 1 MSM82C37A-5 priority decision modes

Priority mode		Fixed	Rotating			
Service terminated channel		–	CH0	CH1	CH2	CH3
Order of priority for next DMA	Highest	CH0	CH1	CH2	CH3	CH0
	↑	CH1	CH2	CH3	CH0	CH1
	↓	CH2	CH3	CH0	CH1	CH2
	Lowest	CH3	CH0	CH1	CH2	CH3

COMPRESSED TIMING

Setting the MSM82C37A-5 to compressed timing mode enables the S3 state used in extension of the read pulse access time to be omitted (if permitted by system structure) for two or three clock cycle DMA transfers. If the S3 state is omitted, the read pulse width becomes the same as the write pulse width with the address updated in S2 and the read or write operation executed in S4. This mode is disregarded if the transfer is a memory-memory transfer. transfer.

EXTENDED WRITING

When this mode is set, the $\overline{IOW}$ or $\overline{MEMW}$ signal which normally appears during the S3 state is obtained during the S2 state, thereby extending the write pulse width. The purpose of this extended write pulse is to enable the system to accomodate memories and I/O devices where the access time is slower. Although the pulse width can also be extended by using READY, that involves the insertion of a SW state to increase the number of states.

DESCRIPTION OF INTERNAL REGISTERS

CURRENT ADDRESS REGISTER

Each channel is equipped with a 16-bit long current address register where the transfer address is held during DMA transfers. The register value is incremented (or decremented) in each DMA cycle. Although this register is 16 bits long, the CPU is accessed by the MSM82C37A-5 eight bits at a time, therefore necessitating two successive 8-bit (lower and higher order bits) reading or writing operations using internal first/last flip-flops.

When autoinitialize has been set, the register is automatically initialized to the original value after TC.

CURRENT WORD COUNT REGISTER

Each channel is also equipped with a 16 bit-long current word count register where the transfer count is held during DMA transfers. The register value is decremented in each DMA cycle. When the word count value reaches FFFF(H) from OOOO(H), a TC is generated. Therefore, a word count vaue which is one less than the actual number of transfers must be set.

Since this register is also 16 bits long, it is accessed by first/last flip-flops control in the same way as the address register. And if autoinitialize has been set, the register is automatically initialized to the original value after TC.

BASE ADDRESS REGISTER AND BASE WORD COUNT REGISTER

Each channel is equipped with a 16-bit long base address register and base word count register where the initial value of each current register is held. The same values are written in each base register and the current register by the CPU. The contents of the current register can be made ready by the CPU, but the content of the base register cannot be read.

COMMAND REGISTER

This 8-bit write-only register prescribes DMA operations for all MSM82C37A-5 channels. An outline of all bits is given in Figure 3. When the controller is disabled by setting DB2, there is no HRQ output even if DMA request is active.

DREQ and DACK signals may be active high or active low by setting DB6 and DB7.

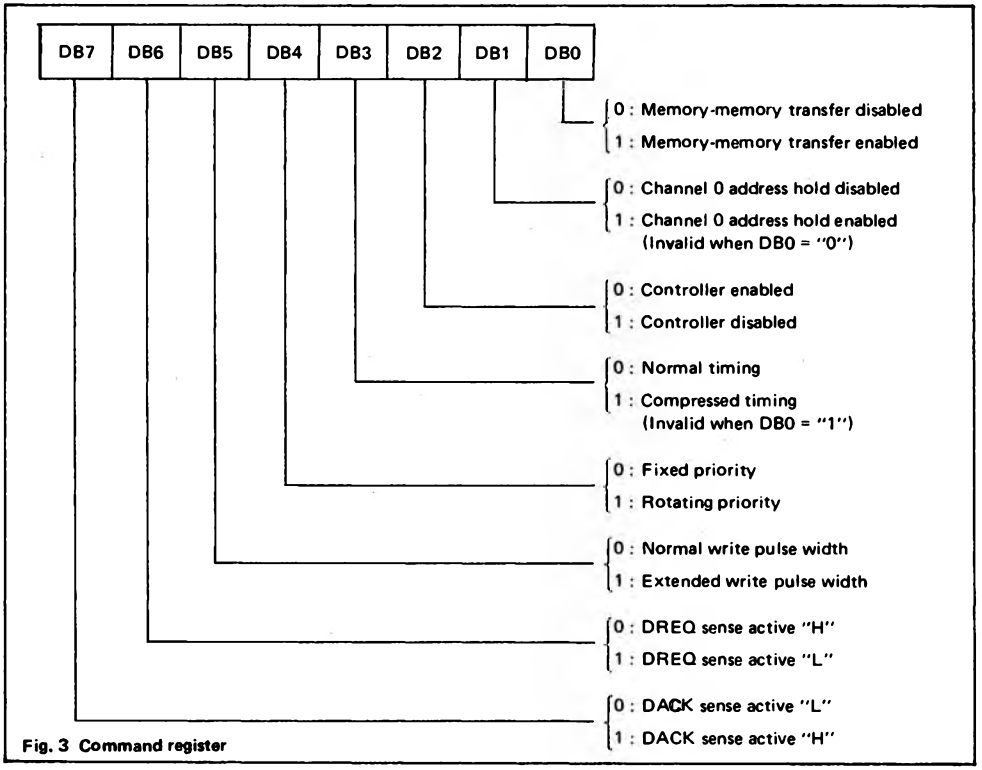


Fig. 3 Command register

MODE REGISTER

Each channel is equipped with a 6-bit write-only mode register, which is decided by setting DB0, DB1 which channel is to be written when writing from the CPU is programming status. The bit description is outlined in Figure 4.

This register is not cleared by Reset or Master Clear instruction.

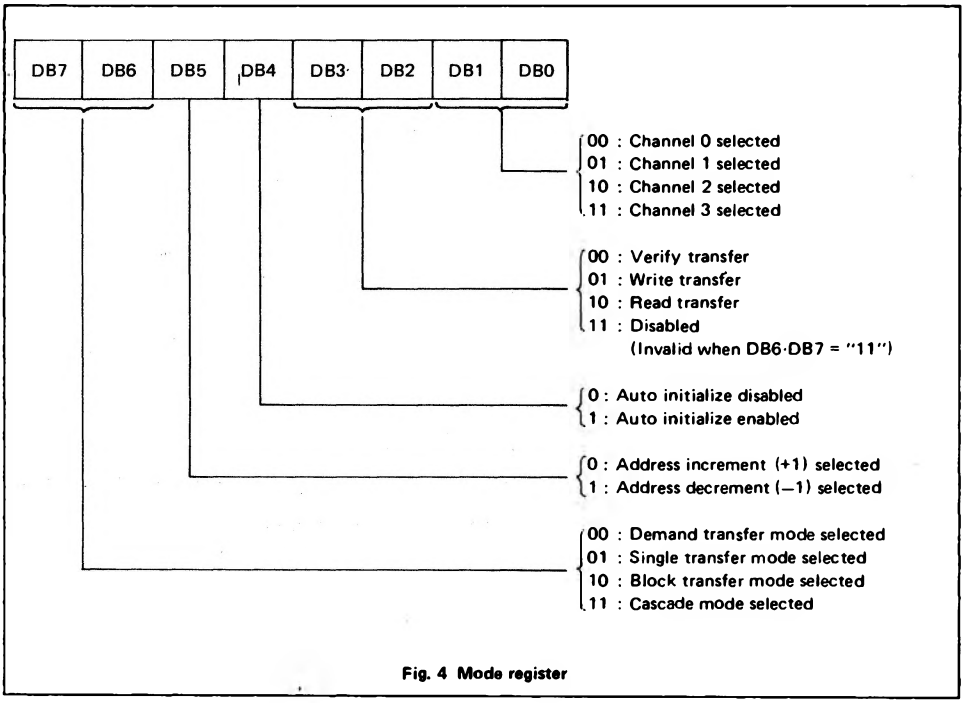


Fig. 4 Mode register

REQUEST REGISTER

In addition to using the DREQ signal, the MSM82C37A-5 can request DMA transfers by software means. This involves setting the request bit of request register. Each channel has a corresponding request bit in the request register, and the order of priority of these bits is determined by the priority decision circuit irrespective of the mask register. DMA transfers are acknowledged in accordance with the decided order of priority.

All request bits are reset when the TC is reached, and when the request bit of a certain channel has been received, all other request bits are cleared. When a memory-memory transfer is commenced, the channel 0 request bit is set. The bit description is outlined in Figure 5.

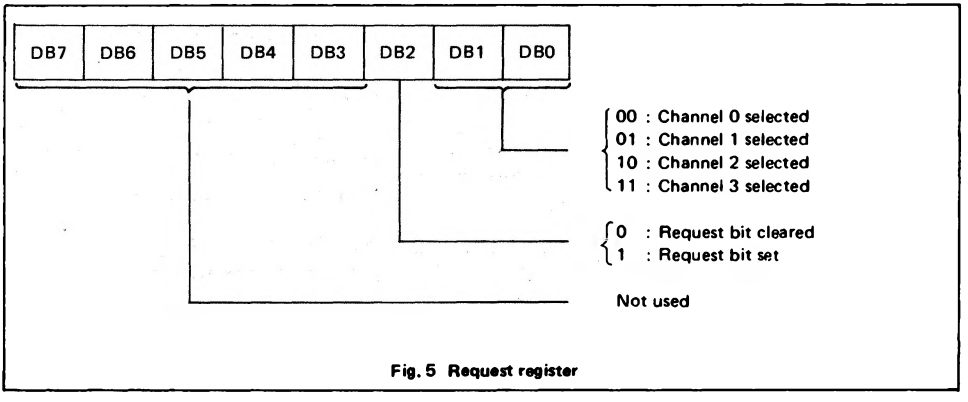
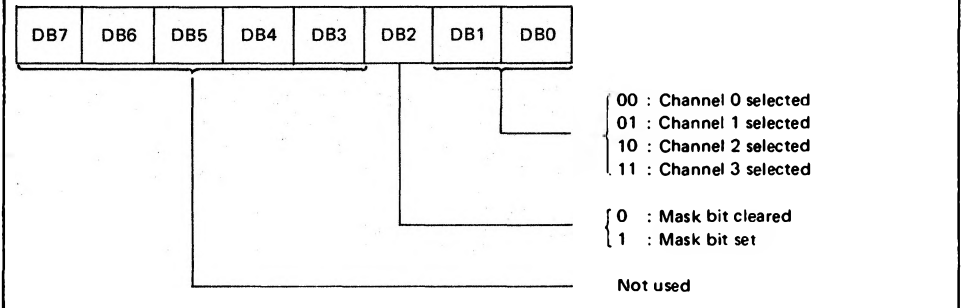


Fig. 5 Request register

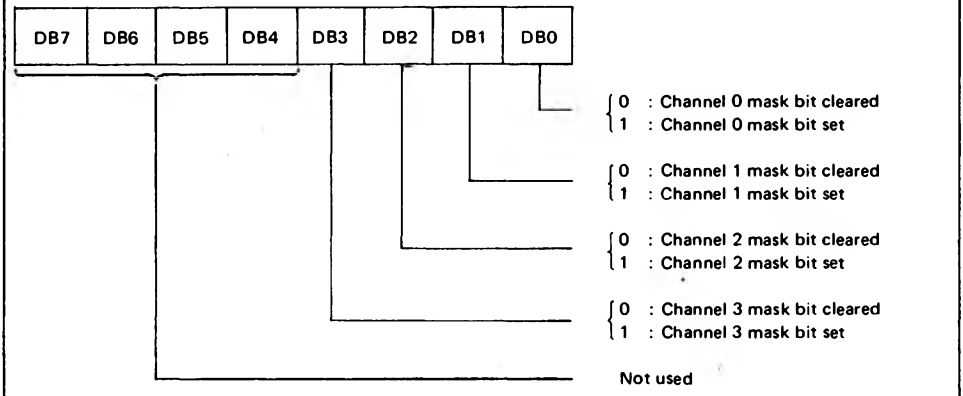
MASK REGISTER

This register is used in disabling and enabling of DMA transfers in each channel. Each channel includes a corresponding mask bit in the mask register, and each bit is set when the TC is reached if not in autoinitialize mode. This mask register can be set in two different ways.

The method for setting/resetting the register for each channel is outlined in Figure 6(a), while the method for setting/resetting the register for all channels at once is outlined in Figure 6(b).



(a) Single mask register (setting/resetting for each channel)



(b) All mask register (setting/resetting of all channels at once)

Fig. 6 Mask register

STATUS REGISTER

This register is a read-only register used in CPU reading of the MSM82C37A-5 status. The four higher order bits indicate the DMA transfer request status for each channel, '1' being set when the DREQ input signal is active.

The four lower order bits indicate whether the corresponding channel has reached the TC or not, '1' being set when the TC status is reached. These four lower order bits are reset by status register reading, or RESET input and master clearing. A description of each bit is outlined in Figure 7.

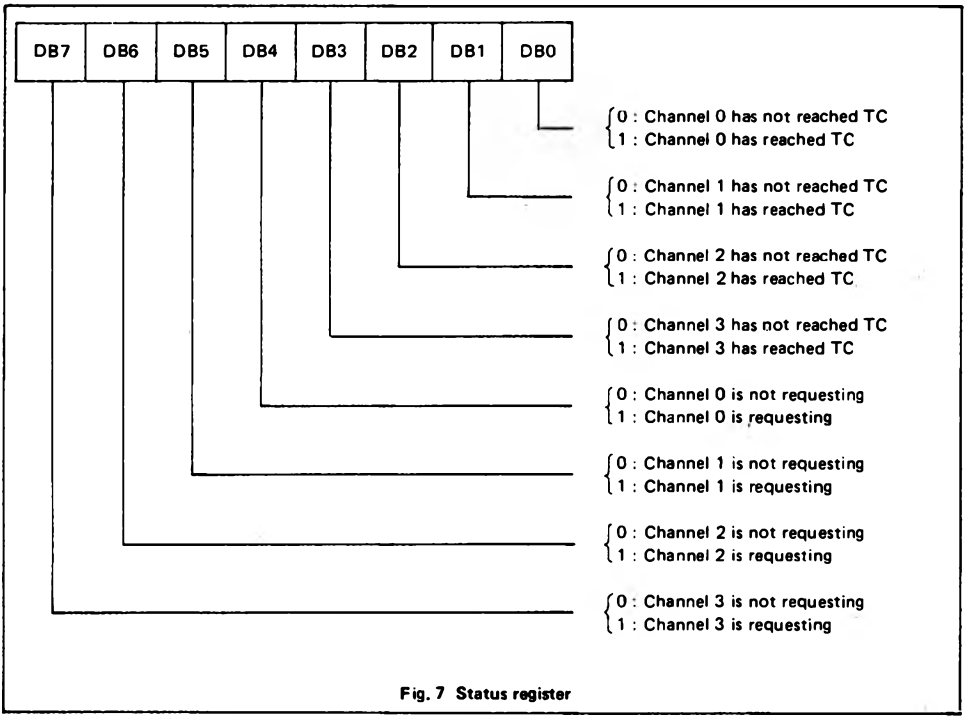


Fig. 7 Status register

TEMPORARY REGISTER

The temporary register is a register where transfer data is held temporarily during memory-memory transfers. Since the last item of data to be transferred is held after completion of the transfer, this item can be read by the CPU.

SOFTWARE COMMAND

The MSM82C37A-5 is equipped with software commands for executing special operations to ensure proper programming. Software command is irrespective of data bus contents.

CLEAR FIRST/LAST FLIP-FLOP

16-bit address and word count registers are read or written in two consecutive operations involving eight bits each (higher and lower order bits) under data bus port control. The fact that the lower order bits are accessed first by the MSM82C37A-5, followed by accessing of the higher order bits, is discerned by the internal first/last flip-flop. This command resets the first/last flip-flop with the eight lower order bits being accessed immediately after execution.

MASTER CLEAR

The same operation as when the hardware RESET input is applied. This command clears the contents of the command, status (for lower order bits), request, and temporary registers, also clears the first/last flip-flop, and sets the mask register. This command is followed by an idle cycle.

CLEAR MASK REGISTER

When this command is executed, the mask bits for all channels are cleared to enable reception of DMA transfers.

PROGRAMMING

The MSM82C37A-5 is switched to programming status when the HLDA input and $\overline{CS}$ are both at low level. In this state, $\overline{IOR}$ is changed to low level with $\overline{IOW}$ held at high level to enable reading by the CPU, or else $\overline{IOW}$ is changed to low level while $\overline{IOR}$ is held at high level to enable writing by the CPU.

A list of command codes for reading from the MSM82C37A-5 is given in Table 2, and a list of command codes for writing in the MSM82C37A-5 is given Table 3.

Note: If a DMA transfer request is received from an I/O device during MSM82C37A-5 programming, that DMA transfer may be commenced to prevent proper programming.
To prevent this interference, the DMA channel must be masked, or the controller disabled by the command register, or the system set so as to prevent DREQ becoming active during the programming.

Table 2 List of MSM82C37A-5 read commands

$\overline{CS}$	$\overline{IOR}$	A3	A2	A1	A0	Internal first/last flip/flop	Read out data		
0	0	0	0	0	0	0	Channel 0	Current address register	8 lower order bits
0	0	0	0	0	0	1			8 higher order bits
0	0	0	0	0	1	0		Current word count register	8 lower order bits
0	0	0	0	0	1	1			8 higher order bits
0	0	0	0	1	0	0	Channel 1	Current address register	8 lower order bits
0	0	0	0	1	0	1			8 higher order bits
0	0	0	0	1	1	0		Current word count register	8 lower order bits
0	0	0	0	1	1	1			8 higher order bits
0	0	0	1	0	0	0	Channel 2	Current address register	8 lower order bits
0	0	0	1	0	0	1			8 higher order bits
0	0	0	1	0	1	0		Current word count register	8 lower order bits
0	0	0	1	0	1	1			8 higher order bits
0	0	0	1	1	0	0	Channel 3	Current address register	8 lower order bits
0	0	0	1	1	0	1			8 higher order bits
0	0	0	1	1	1	0		Current word count register	8 lower order bits
0	0	0	1	1	1	1			8 higher order bits
0	0	1	0	0	0	X	Status register		
0	0	1	1	0	1	X	Temporary register		
0	0	Other combinations				X	Output data invalid		

Table 3 List of MSM82C37A-5 write commands

$\overline{CS}$	$\overline{IOW}$	A3	A2	A1	A0	Internal first/last flip-flop	Written data		
0	0	0	0	0	0	0	Channel 0	Current and base address registers	8 lower order bits
0	0	0	0	0	0	1			8 higher order bits
0	0	0	0	0	1	0		Current and base word count registers	8 lower order bits
0	0	0	0	0	1	1			8 higher order bits
0	0	0	0	1	0	0	Channel 1	Current and base address registers	8 lower order bits
0	0	0	0	1	0	1			8 higher order bits
0	0	0	0	1	1	0		Current and base word count registers	8 lower order bits
0	0	0	0	1	1	1			8 higher order bits
0	0	0	1	0	0	0	Channel 2	Current and base address registers	8 lower order bits
0	0	0	1	0	0	1			8 higher order bits
0	0	0	1	0	1	0		Current and base word count registers	8 lower order bits
0	0	0	1	0	1	1			8 higher order bits
0	0	0	1	1	0	0	Channel 3	Current and base address registers	8 lower order bits
0	0	0	1	1	0	1			8 higher order bits
0	0	0	1	1	1	0		Current and base word count registers	8 lower order bits
0	0	0	1	1	1	1			8 higher order bits
0	0	1	0	0	0	X	Command register		
0	0	1	0	0	1	X	Request register		
0	0	1	0	1	0	X	Single mask register		
0	0	1	0	1	1	X	Mode register		
0	0	1	1	0	0	X	Clear first/last flip-flop (software command)		
0	0	1	1	0	1	X	Master clear (software command)		
0	0	1	1	1	0	X	Clear mask register (software command)		
0	0	1	1	1	1	X	All mask register		