Preliminary

OKI semiconductor

MSM82C54-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

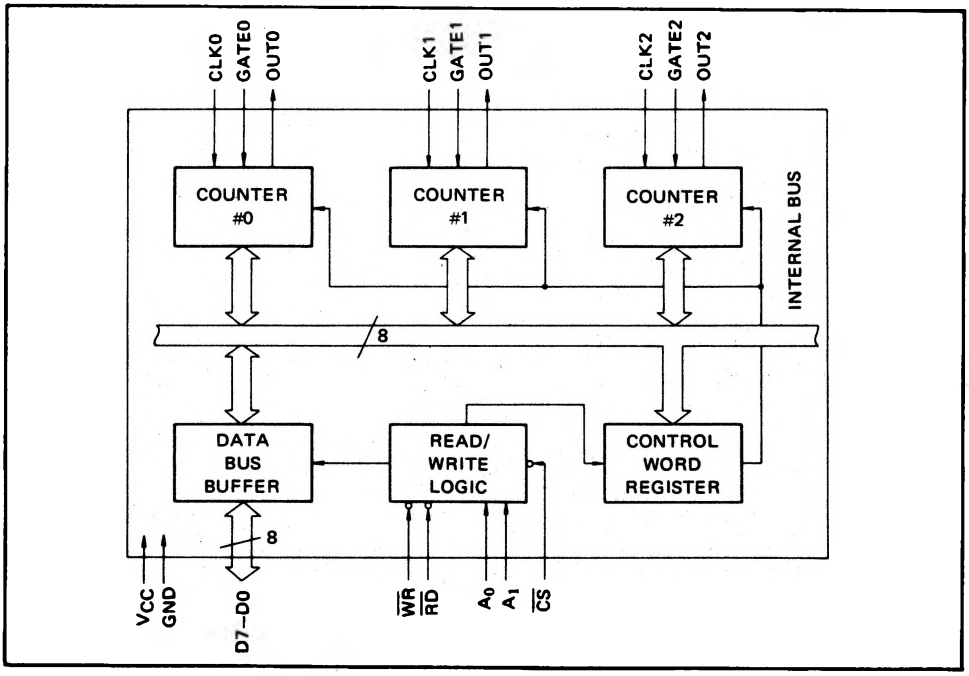
The MSM82C54-2RS/GS/JS is a programmable universal timer designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 10 μA (max.) when the chip is in the non-selected state. And during timer operation, the power consumption is still very low with only 10mA (max.) of current required.

It consists of three independent counters, and can count up to a maximum of 10 MHz. The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

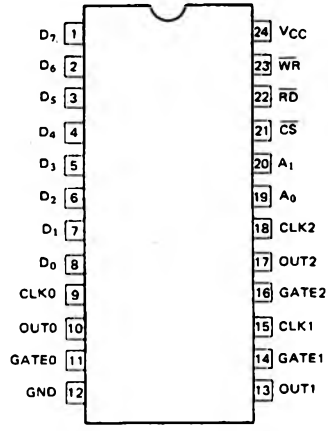
- Maximum operating frequency of 10 MHz (V_{CC}=5V)
- High speed and low power consumption achieved by silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- Status Read Back Commound
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24-pin DIP (MSM82C54-2RS)
- 32-pin flat package (MSM82C54-2GS)
- 28-pin PLCC package (MSM82C54-2JS)

FUNCTIONAL BLOCK DIAGRAM

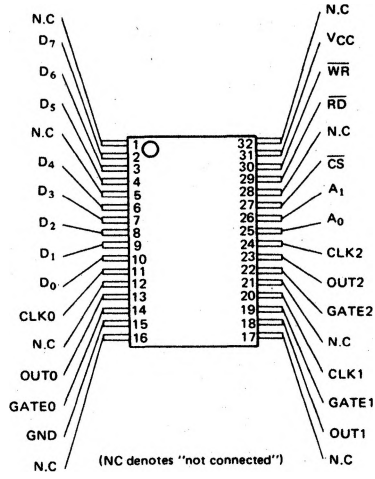


PIN CONFIGURATION

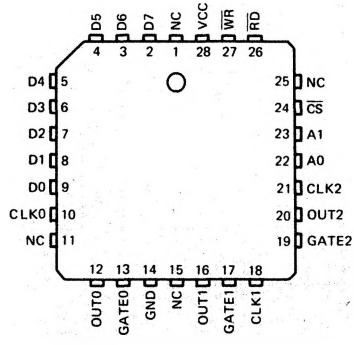
MSM82C54-2RS (TOP VIEW)
24 LEAD PLASTIC DIP



MSM82C54-2GS (TOP VIEW)
32 LEAD PLASTIC FLAT PACKAGE



MSM82C54-2JS (TOP VIEW)
28 Plastic Leaded Chip Carrier PACKAGE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C54-2RS	MSM82C54-2GS	MSM82C54-2JS	
Supply voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.5		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.5	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 2.5mA	V_{CC}=4.5V to 5.5V Ta=−40°C to +85°C			0.40	V
"H" Output Voltage	V_{OH}	I_{OH} = −2.5mA		3.0			V
		I_{OH}=−100μA		V_{CC}−0.4			
Input Leak Current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{CC}$		−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC}$ −0.2V $V_{IH} \geqq V_{CC}$ − 0.2V $V_{IL} \leqq 0.2V$				10	μA
Operating Supply Current	I_{CC}	t_{CLK}=100ns CL=0pF				10	mA

AC CHARACTERISTICS

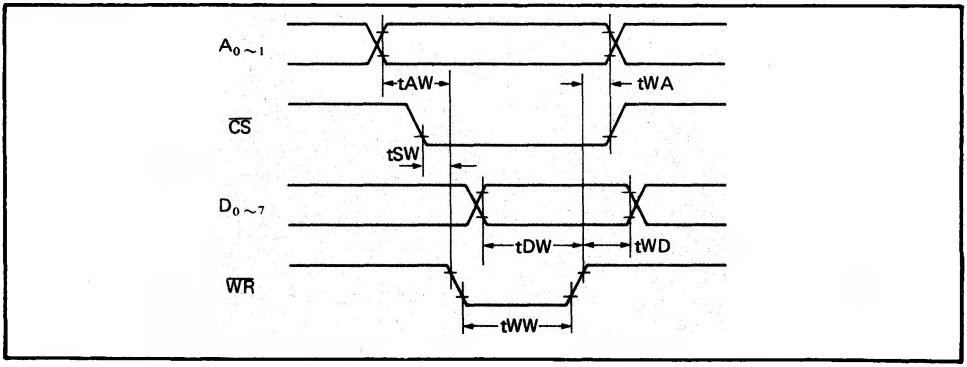
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	82C54-2 Min	82C54-2 Max	Unit	Conditions	
Address set-up time to falling edge of $\overline{RD}$	tAR	30		nS	Read timing	CL=150pF
Chip select input set-up time to falling edge of $\overline{RD}$	tSR	0		nS		
Address hold time from rising edge of $\overline{RD}$	tRA	0		nS		
$\overline{RD}$ pulse width	tRR	95		nS		
Data access time from falling edge of $\overline{RD}$	tRD		94	nS		
Data access time after address determination	tAD		185	nS		
Delay time from rising edge of $\overline{RD}$ to data floating state	tDF	5	65	nS		
$\overline{RD}$ recovery time	tRV	165		nS		
Address set-up time to falling edge of $\overline{WR}$	tAW	0		nS	Write timing	
Chip select input set-up time to falling edge of $\overline{WR}$	tSW	0		nS		
Address hold time from rising edge of $\overline{WR}$	tWA	0		nS		
$\overline{WR}$ pulse width	tWW	95		nS		
Data determination set-up time to rising edge of $\overline{WR}$	tDW	85		nS		
Data hold time after rising edge of $\overline{WR}$	tWD	0		nS		
$\overline{WR}$ recovery time	tRV	165		nS		
CLK cycle time	tCLK	100	D.C.	nS	Clock gate timing	
CLK "H" level width	tPWH	30		nS		
CLK "L" level width	tPWL	50		nS		
CLK rise time	tR		25	nS		
CLK fall time	tF		25	nS		
GATE "H" level width	tGW	50		nS		
GATE "L" level width	tGL	50		nS		
GATE input set-up time before rising edge of CLK	tGS	40		nS		
GATE input hold time before rising edge of CLK	tGH	50		nS		
Output delay time after falling edge of CLK	tOD		100	nS		
Output delay time after falling edge of GATE	tODG		100	nS		
CLK rise delay time after rising edge of $\overline{WR}$ for count value loading	tWC	0	55	nS		
GATE sampling delay time after rising edge of $\overline{WR}$ for count value loading	tWG	–5	40	nS		
Output delay time after falling edge of $\overline{WR}$ for mode set	tWO		240	nS		
CLK fall set-up time to falling edge of for counter latch command	tCL	–40	40	nS		

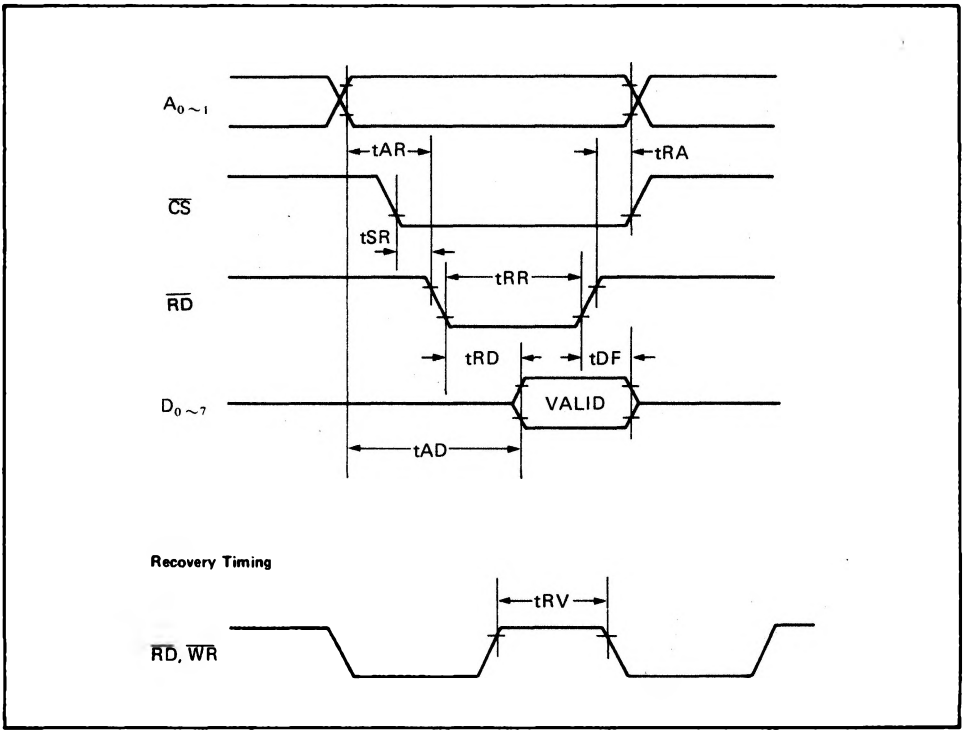
Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

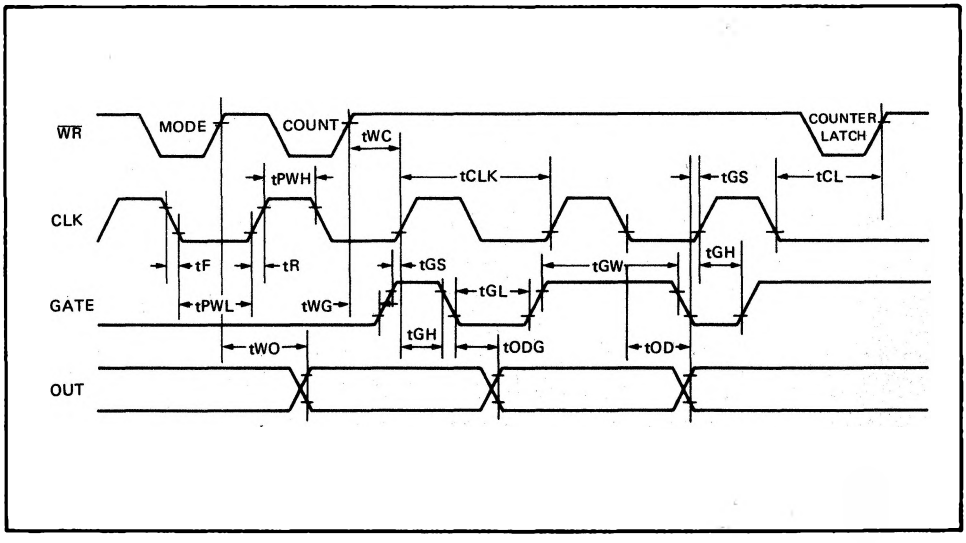
Write Timing



Read Timing



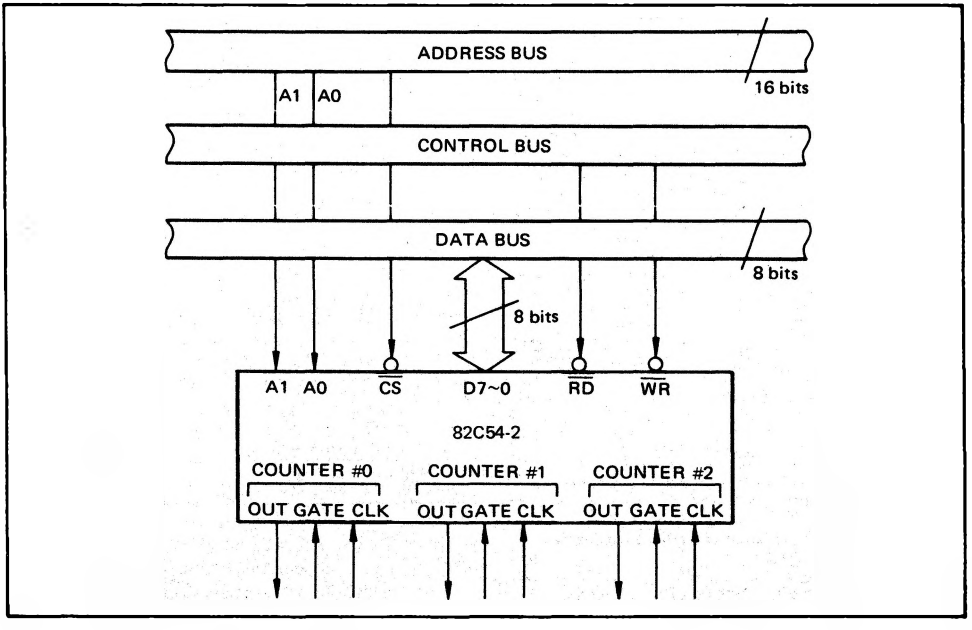
Clock & Gate Timing



DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C54-2 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C54-2 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C54-2.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

x denotes "not specified".

DESCRIPTION OF OPERATION

82C54-2 functions are selected by control words from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operating mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	READ BACK COMMAND

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, the count value is set first. In next clock, loading is performed, then counting starts.) This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can't be read.

The program sequence of the 82C54-2 is flexible. Free sequence programming is possible as long as the two following rules are observed:

(i) Write the control word before writing the initial count value in each counter.

(ii) Write the initial count value according to the count value read/write format specified by the control word.

(Note) Unlike the 82C53-5, the 82C54-2 allows count value setting for another counter between LSB and MSB settings.

- **Example of control word and count value setting**

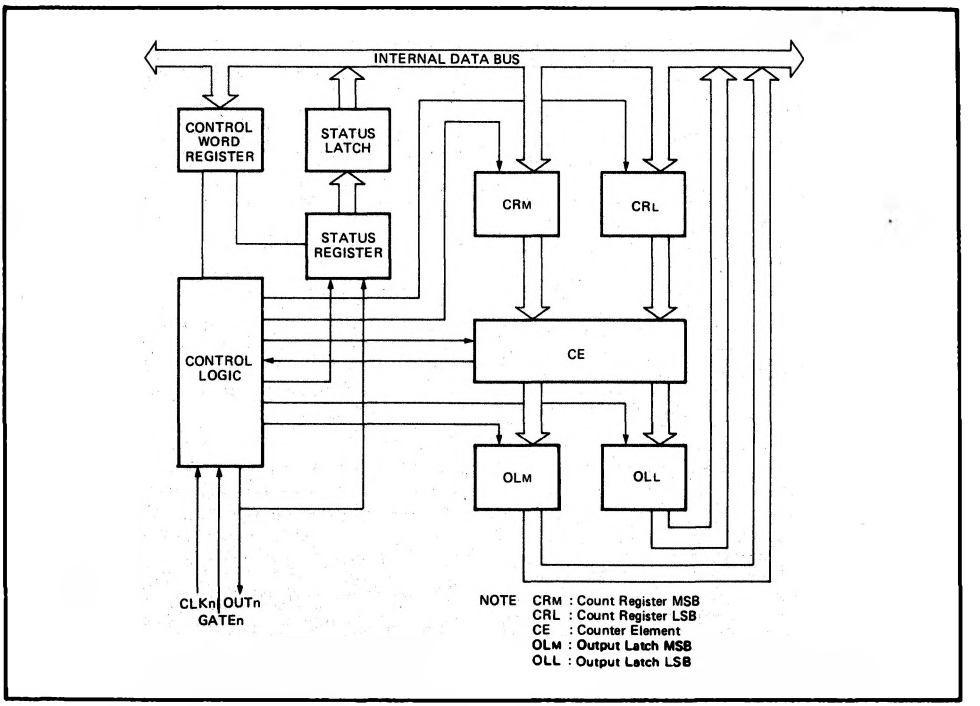
```
Counter #0: Read/Load LSB only, Mode 3,
            Binary count, count value 3H
Counter #1: Read/Load MSB only, Mode 5,
            Binary count, count value AA00H
Counter #2: Read/Load LSB and MSB, Mode 0,
            BCD count, count value 1234

MVI A, 1EH
OUT n3      ] Counter #0 control word setting
MVI A, 6AH
OUT n3      ] Counter #1 control word setting
MVI A, B1H
OUT n3      ] Counter #2 control word setting
MVI A, 03H
OUT n0      ] Counter #0 count value setting
MVI A, AAH
OUT n1      ] Counter #1 count value setting
MVI A, 34H
OUT n2
MVI A, 12H  ] Counter #2 count value setting
OUT n2      ] (LSB then MSB)
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min	Max	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	0	1 cannot be counted
4	1	0	
5	1	0	

INTERNAL BLOCK DIAGRAM OF A COUNTER



Mode definition

Mode 0

- Use: Event counter
- Output operation: The output is set to "L" level by the control word setting, and kept at "L" level until the counter value becomes 0.
- Gate function: "H" level validates the count operation, and "L" level invalidates it. The gate does not affect the output.
- Count value load timing: after the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. The first clock pulse does not cause the count value to be decremented. In other words, if the initial count value is N, the output is not set to "H" level until the input of (N+1) the clock pulse after the initial count value writing.
- Count value writing during counting:
  The count value is loaded in the CE at the falling edge of the next clock, and counting with the new count value continues. The operation for 2-byte count is as follows:
  1) The counting operation is suspended when the first byte is written. The output is immediately set to "L" level. (no clock pulse is required.)
  2) After the scond byte is written, the new count value is loaded to the CE at the falling edge of the next clock.
     For the output to go to "H" level again, N+1 clock pulses are necessary after new count value N is written.
- Count value writing when the gate signal is "L" level:
  The count value is also loaded to the CE at the falling edge of the next clock pulse in this case. When the gate signal is set to "H" level, the output is set to "H" level after the lapse of N clock pulses. Since the count value is already loaded in the CE, no clock pulse for loading in the CE is necessary.

Mode 1

- Use: Digital one-shot
- Output operation: The output is set to "H" level by the control word setting. It is set to "L" level at the falling edge of the clock succeeding the gate trigger, and kept at "L" level until the counter value becomes 0. Once the output is set to "H" level, it is kept at "H" level until the clock pulse succeeding the next trigger pulse.
- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the clock pulse succeeding the gate trigger and set the output to "L" level. The one-shot pulse starts in this way. If the initial count value is N, the one-shot pulse interval equals N clock pulses. The one-shot pulse is not repetitive.
- Gate function: The gate signal setting to "L" level after the gate trigger does not affect the output. When it is set to "H" level again from "L" level, gate retriggering occurs, the CR count value is loaded again, and counting continues.
- Count value writing during counting
  It does not affect the one-shot pulse being counted until retriggering occurs.

Mode 2

- Use: Rate generator, real-time interrupt clock.
- Output operation: The output is set to "H" level by control word setting. When the initial count value is decremented to 1, the output is set to "L" level during one clock pulse, and is then set to "H" level again. The initial count value is reloaded, and the above sequence repeats. In mode 2, the same sequence is repeated at intervals of N clock pulses if the initial count value is N for example.
- Gate function: "H" level validates counting, and "L" level invalidates it. If the gate signal is set to "L" level when the output pulse is "L" level, the output is immediately set to "H" level. At the falling edge of the clock pulse succeeding the trigger, the count value is reloaded and counting starts. The gate input can be used for counter synchronization in this way.
- Count value load timing:
  After the control word and initial count value is written, the count value is loaded to the CE at the falling edge of the next clock pulse. The output is set to "L" level upon lapse of N clock pulses after writing the initial count value N. Counter synchronization by software is possible in this way.
- Count value writing during counting:
  Count value writing does not affect the current counting operation sequence. If new count value writing completes and the gate trigger arrives before the end of current counting operation, the count value is loaded to the CE at the falling edge of the next clock pulse and counting continues from the new count value. If no gate trigger arrives, the new count value is loaded to the CE at the end of the current counting operation cycle. In mode 2, count value of 1 is prohibited.

Mode 3

- Use: Baud rate generator, square wave generator
- Output operation: Same as mode 2 except that the output duty is different.
  The output is set to "H" level by control word setting. When the count becomes half the initial count value, the output is set to "L" level and kept at "L" level during the remainder of the count.
  Mode 3 repeats the above sequence periodically. If the initial count value is N, the output becomes a square wave with a period of N.
- Gate operation: "H" level validates counting, and "L" level invalidates it. If the gate signal is set to "L" level when the output is "L" level, the output is immediately set to "H" level.
  The initial count value is reloaded at the falling edge of the clock pulse succeeding the next gate trigger. The gate can be used for counter synchronization in this way.

- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. Counter synchronization by software is possible in this way.
- Count value writing during counting:
  The count value writing does not affect the current counting operation. When the gate trigger input arrives before the end of a half cycle of the square wave after writing the new count value, the new count value is loaded in the CE at the falling edge of the next clock pulse, and counting continues using the new count value. If there is no gate trigger, the new count value is loaded at the end of the half cycle and counting continues.
- Even number counting operation:
  The output is initially set to "H" level. The initial count value is loaded to the CE at the falling edge of the next clock pulse, and is decremented by 2 by consecutive clock pulses. When the counter value becomes 2, the output is set to "L" level, the initial value is reloaded and then the above operation is repeated.
- Odd number counting operation:
  The output is initially set to "H" level. At the falling edge of the next clock pulse, the initial count value minus one is loaded in the CE, and then the value is decremented by 2 by consecutive clock pulses. When the counter value becomes 0, the output is set to "L" level, and then the initial count value minus 1 is reloaded to the CE. The value is then decremented by 2 by consecutive clock pulses. When the counter value becomes 2, the output is again set to "H" level and the initial count value minus 1 is again reloaded. The above operations are repeated. In other words, the output is set to "H" level during (N+1)/2 counting and to "L" level during (N−1)/2 counting in the case of odd number counting.

Mode 4

- Use: Software trigger strobe
- Output operation: The output is initially set to "H" level. When the counter value becomes 0, the output goes to "L" level during one clock pulse, and then restores "H" level again.
  The count sequence starts when the initial count value is written.
- Gate function: "H" level validates counting, and "L" level invalidates counting. The gate signal does not affect the output.
- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. The clock pulse does not decrement the initial count value. If the initial count value is N, the strobe is not output unless N+1 clock pulses are input after the initial count value is written.
- Count value writing during counting:
  The new count value is written to the CE at the falling edge of the next clock pulse, and counting continues using the new count value. The operation for 2-byte count is as follows:
  1) First byte writing does not affect the counting operation.
  2) After the second byte is written, the new count value is loaded to the CE at the falling edge of the next clock pulse.

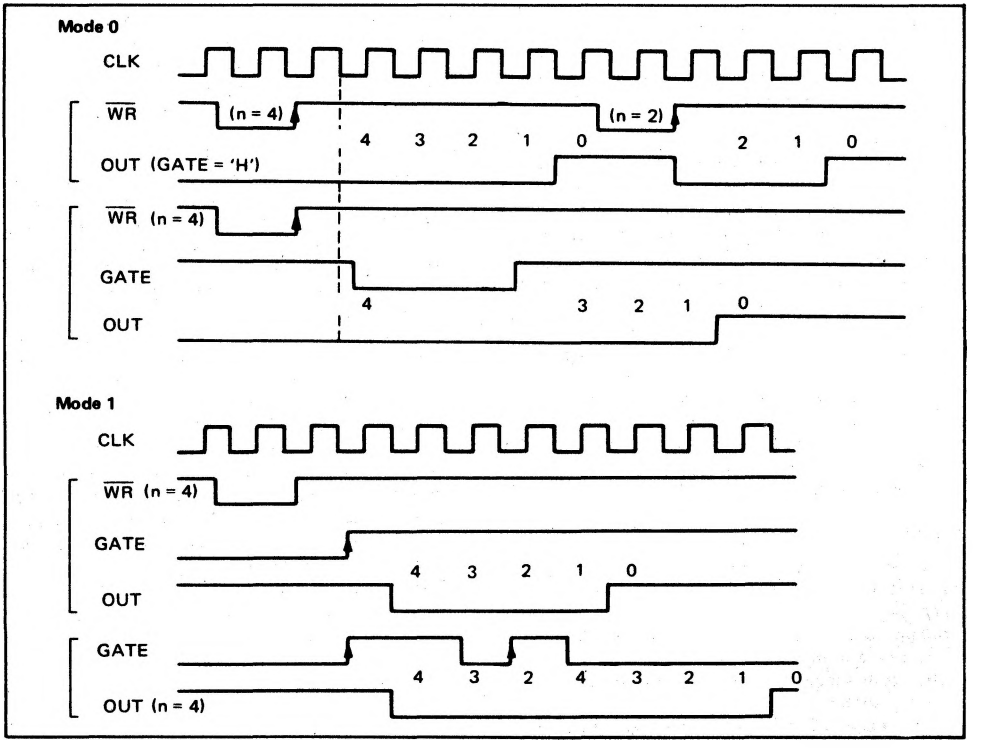
  This means that the counting operation is retriggered by software. The output strobe is set to "L" level upon input of N+1 clock pulses after the new count value N is written.

Mode 5

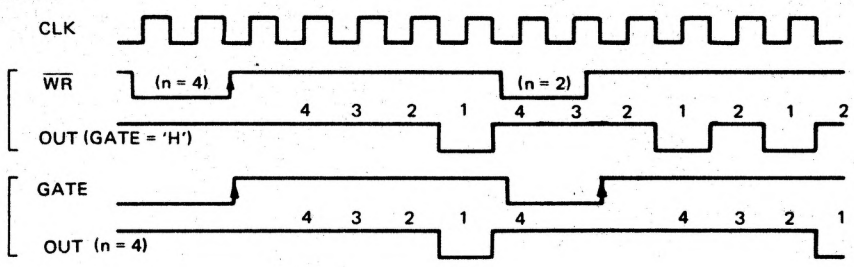
- Use: Hardware trigger strobe
- Output operation: The output is initially set to "H" level. When the counter value becomes 0 after triggering by the rising edge of the gate pulse, the output goes to "L" level during one clock pulse, and then restores "H" level.
- Count value load timing:
  Even after the control word and initial count value are written, loading to the CE does not occur until the input of the clock pulse succeeding the trigger. For the clock pulse for CE loading, the count value is not decremented. If the initial count value is N, therefore, the output is not set to "L" level until N+1 clock pulses are input after triggering.
- Gate function:
  The initial count value is loaded to the CE at the falling edge of the clock pulse succeeding gate triggering. The count sequence can be retriggered. The gate pulse does not affect the output.
- Count value writing during counting:
  The count value writing does not affect the current counting sequence. If the gate trigger is generated after the new count value is written and before the current counting ends, the new count value is loaded to the CE at the falling edge of the next clock pulse, and counting continues using the new count value.

The various roles of the gate input signals in the above modes are summarized in the following table.

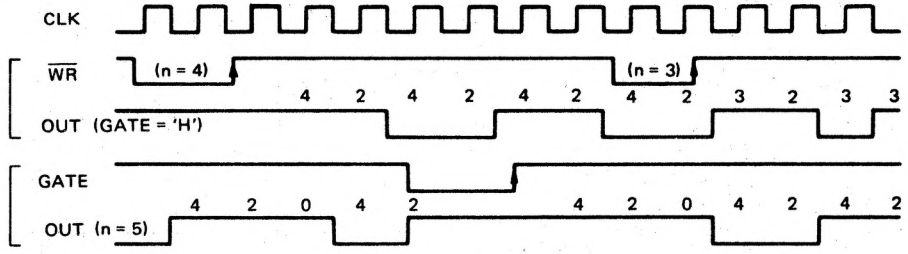
Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



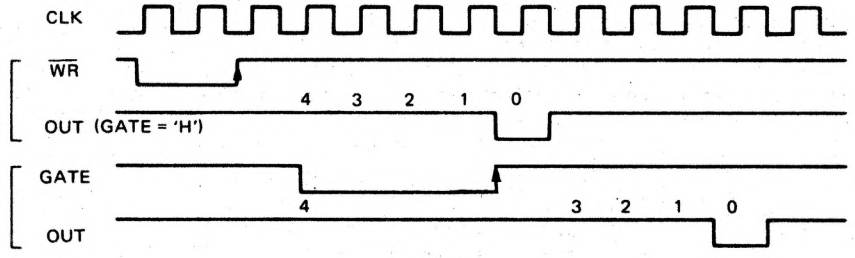
Mode 2



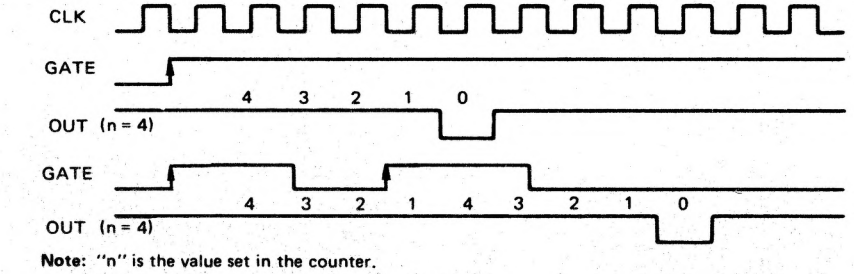
Mode 3



Mode 4



Mode 5



Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

Reading Counter Values

All 82C54-2 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, (2) counter latching ("read on the fly"), and (3) read back command.

(1) Direct reading

Counter values can be read by direct reading operations.

Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

(2) Counter latching

In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. The output latch (OL) of the selected counter latches the count value when a counter latch command is written. The count value is held until it is read by the CPU or the control word is set again.

If a counter latch command is written again before reading while a certain counter is latched, the second counter latch command is ignored and the value latched by the first counter latch command is maintained.

The 82C54-2 features independent reading and writing from and to the same counter.

When a counter is programmed for the 2-byte counter value, the following sequence is possible:

1. Count value (LSB) reading
2. New count value (LSB) writing
3. Count value (MSB) reading
4. New count value (MSB) writing

An example of a counter latching program is given below.

Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  01 00 x x x x
                └── Denotes counter latching
OUT n3 ──┬── Write in control word address (n3)
         └── The counter value at this point is latched
IN n1  ──┬── Reading of the LSB of the counter value latched from counter #1.
         └── n1: Counter #1 address
MOV B, A
IN n1  ──── Reading of MSB from counter #1.
MOV C, A
```

(3) Read Back Command Operation

Use of the read back command enables the user to check the count value, program mode, output pin state and null count flag of the selected counter.

The command is written in the control word register, and the format is as shown below. For this command, the counter selection occurs according to bits D3, D2 and D1.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	COUNT	STATUS	CNT2	CNT1	CNT0	0

(CS = 0, A0, A1 = 1, RD = 1, WR = 0)

D5: 0 = Selected counter latch operation
D4: 0 = Selected counter status latch operation
D3: 1 = Counter #2 selection
D2: 1 = Counter #1 selection
D1: 1 = Counter #0 selection
D0: 0 Fixed

It is possible to latch multiple counters by using the read back command. Latching of a read counter is automatically cancelled but other counters are kept latched. If multiple read back commands are written for the same counter, commands other than the first one are ignored.

It is also possible to latch the status information of each counter by using the read back command. The status of a certain counter is read when the counter is read.

The counter status format is as follows:

Bits D5 to D0 indicates the mode programmed by the most recently written control word.

Bit D7 indicates the status of the output pin.

Use of this bit makes it possible to monitor the counter output, so the corresponding hardware may be omitted.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RL1	RL0	M2	M1	M0	BCD

D7: 1 = Output pin status is 1.
0 = Output pin status is 0.
D6: 1 = Null count
0 = Count value reading is effective
D5 – D0: Programmed mode of counter (See the control word format.)

Null count indicates the count value finally written in the counter register (CR) has been loaded in the counter element (CE). The time when the count value was loaded in the CE depends on the mode of each counter, and it cannot be known by reading the counter value because the count value does not tell the new count value if the counter is latched.

The null count operation is shown below.

Operation	Result
A. Control word register writing	Null count = 1
B. Count register (CR) writing	Null count = 1
C. New count loading to CE (CR → CE)	Null count = 0

(Note) The null count operation for each counter is independent. When the 2-byte count is programmed, the null count is set to 1 when the count value of the second byte is written.

If status latching is carried out multiple times before status reading, other than the first status latch is ignored.

Simultaneous latching of the count and status of the selected counter is also possible. For this purpose, set bits D4 and D3, $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits, to 00. This is functionally the same as writing two separate read back commands at the same time. If counter/status latching is carried out multiple times before each reading, other than the first one is ignored here again. The example is shown below.

Command								Contents	Counter 0		Counter 1		Counter 2	
D7	D6	D5	D4	D3	D2	D1	D0		Count	Status	Count	Status	Count	Status
1	1	0	0	0	0	1	0	Read back status and count (counter 0)	L	L	–	–	–	–
1	1	1	0	0	1	0	0	Read back status (counter 1)	L	L	–	L	–	–
1	1	1	0	1	1	0	0	Read back status (counters 1 and 2)	L	L	–	L (NOTE)	–	L
1	1	0	1	1	0	0	0	Read back count (counter 2)	L	L	–	L	L	L
1	1	0	0	0	1	0	0	Read back status and count (counter 1)	L	L	L	L (NOTE)	L	L
1	1	1	0	0	0	1	0	Read back status (counter 0)	L	L (NOTE)	L	L	L	L

L: Latched, –: Not latched

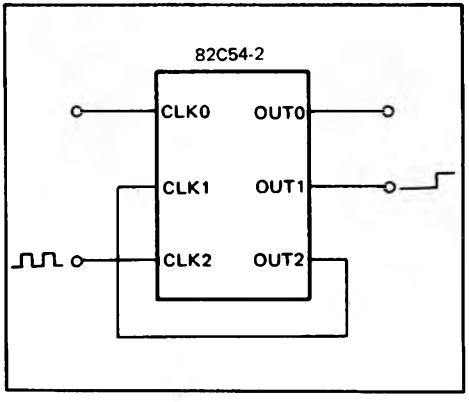
(Note) The latch command at this time point is ignored, and the first latch command is valid.

If both the count and status are latched, the status latched in the first counter read operation is read. The order of count latching and status latching is irrelevant.

The count(s) of the next one or two reading operations is or are read.

Example of Practical Application

- **82C54-2 used as a 32-bit counter.**



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.