OKI semiconductor

MSM82C59A-2RS/GS/JS

PROGRAMMABLE INTERRUPT CONTROLER

GENERAL DESCRIPTION

The MSM82C59A-2 is a programmable interrupt controller for use in MSM80C85A/A-2 and MSM80C86/88 microcomputer systems.

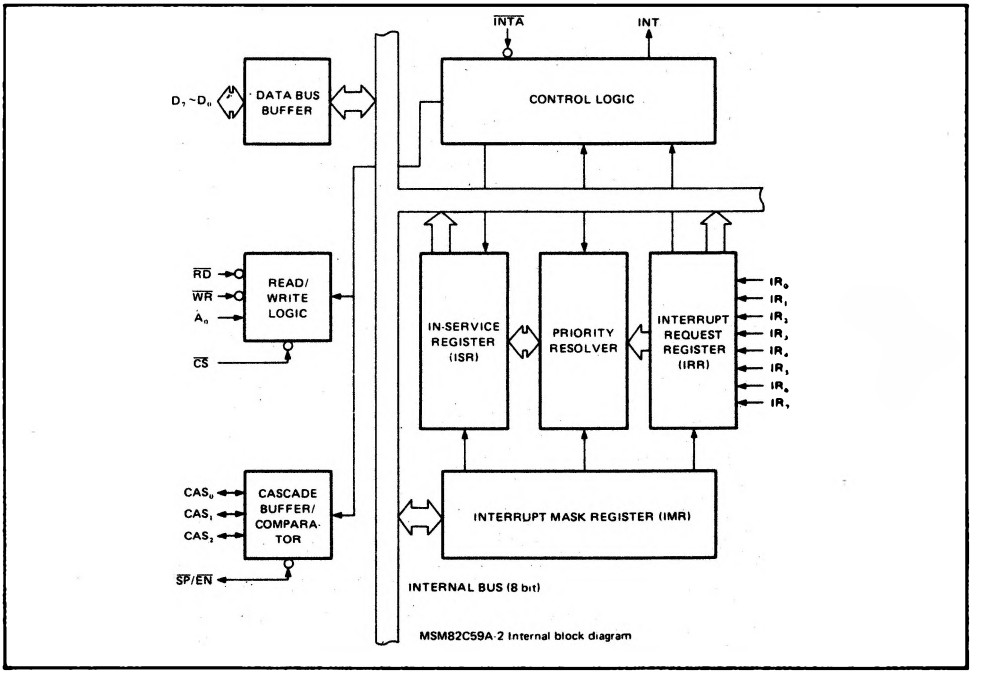
Based on CMOS silicon gate technology, this device features an extremely low standby current of 100 μA (max.) in chip non-selective status. During interrupt control status, the power consumption is very low with only 5 mA (max.) being required.

Internally, the MSM82C59A-2 can control priority interrupts up to 8 levels, and can be expanded up to 64 levels by cascade connection of a number of devices.

FEATURES

- Silicon gate CMOS technology for high speed and low power consumption.
- 3 V to 6 V single power supply
- 80C85A system compatibility (MAX5MHz)
- 80C86/88 system compatibility (MAX8MHz)
- 8-level priority interrupt control
- Interrupt levels expandable up to 64 levels
- Programmable interrupt mode
- Maskable interrupt
- Automatically generated CALL code (85 mode)
- TTL compatible
- 28-pin plastic DIP (MSM82C59A-2RS)
- 32-pin plastic flat package (MSM82C59A-2GS)
- 28-pin PLCC Package (MSM82C59A-2JS)

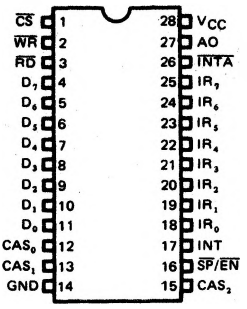
CIRCUIT CONFIGURATION



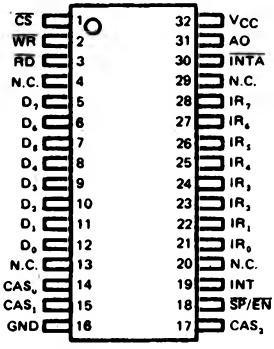
MSM82C59A-2 Internal block diagram

PIN CONNECTIONS

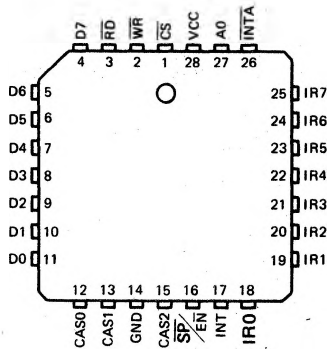
MSM82C59A-2RS (top view)
28-pin lead plastic DIP



MSM82C59A-2 GS (top view)
32-pin lead plastic flat package



MSM82C59A-2JS (top view)
28-pin plastic leaded chip carrier



NC: Not Connected

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C59A-2RS	MSM82C59A-2GS	MSM82C59A-2JS	
Power supply voltage	V_{CC}	Respect to GND	−0.5 ~ +7			V
Input voltage	V_{IN}		−0.5 ~ V_{CC} + 0.5			V
Output voltage	V_{OUT}		−0.5 ~ V_{CC} + 0.5			V
Storage temperature	T_{stg}	—	−55 ~ +150			°C
Power dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

Operating Ranges

Parameter	Symbol	Range	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	−40 ~ +85	°C

Recommended Operating Conditions

Parameter	Symbol	Max.	Typ.	Min.	Unit
Power supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	Top	−40	+25	+85	°C
"L" level input voltage	V_{IL}	-0.5		+0.8	V
"H" level input voltage	V_{IH}	2.2		V_{CC} +0.5	V

DC Characteristics

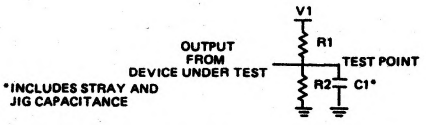
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" level output voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC}=4.5V~5.5V Ta=-40°C~+85°C			0.4	V
"H" level output voltage	V_{OH}	I_{OH} = -2.5 mA		3.0			V
		I_{OH} = -100 μA		V_{CC} - 0.4			
Input leak current	I_{LI}	$0V \leqq V_{IN} \leqq V_{CC}$		-1		1	μA
IR Input leak current	I_{LIR}			-300		10	μA
Output leak current	I_{LO}	$0V \leqq V_{OUT} \leqq V_{CC}$		-10		10	μA
Standby power supply current	I_{CCS}	$\overline{CS}=V_{CC}$, IR = V_{CC} V_{IL}=0V, $V_{IH}=V_{CC}$			0.1	100	μA
Average operation power supply current	I_{CC}	V_{IN}=0V/V_{CC} C_L = 0 pF				5	mA

AC Characteristics

Ta = -40°C ~ +85°C, V_{CC} = 5V ±10%

Parameter	Symbol	Min.	Max.	Unit	TEST	Conditions
Address setup time (to $\overline{RD}$)	TAHRL	10		nS		Read $\overline{INTA}$ timing
Address hold time (after $\overline{RD}$)	TRHAX	5		nS		
$\overline{RD}$/$\overline{INTA}$ pulse width	TRLRH	160		nS		
Address setup time (to $\overline{WR}$)	TAHWL	0		nS		Write timing
Address hold time (after $\overline{WR}$)	TWHAX	0		nS		
$\overline{WR}$ pulse width	TWLWH	190		nS		
Data setup time (to $\overline{WR}$)	TDVWH	160		nS		
Data hold time (after $\overline{WR}$)	TWHDX	0		nS		
IR input width (Low)	TJLJH	100		nS		$\overline{INTA}$ sequence
CAS input setup time (to $\overline{INTA}$) (slave)	TCVIAL	40		nS		
End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$	TRHRL	160		nS		Other timing
End of $\overline{WR}$ to Next $\overline{WR}$	TWHWL	190		nS		
End of Command to Next command	TCHCL	400		nS		
Data valid following $\overline{RD}$/$\overline{INTA}$	TRLDV		120	nS	1	Delay times
Data floating following $\overline{RD}$/$\overline{INTA}$	TRHDZ	10	85	nS	2	
INT output delay time	TJHIH		300	nS	1	
CAS valid following 1st. $\overline{INTA}$ (master)	TIALCV		360	nS	1	
$\overline{EN}$ active following $\overline{RD}$/$\overline{INTA}$	TRLEL		100	nS	1	
$\overline{EN}$ inactive following $\overline{RD}$/$\overline{INTA}$	TRHEH		150	nS	1	
Data valid after address	TAHDV		200	nS	1	
Data valid after CAS	TCVDV		200	nS	1	

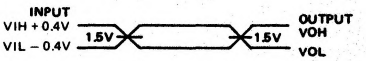
AC TEST CIRCUITS



TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8KΩ	1.8KΩ	30 pf

TEST CONDITION DEFINITION TABLE

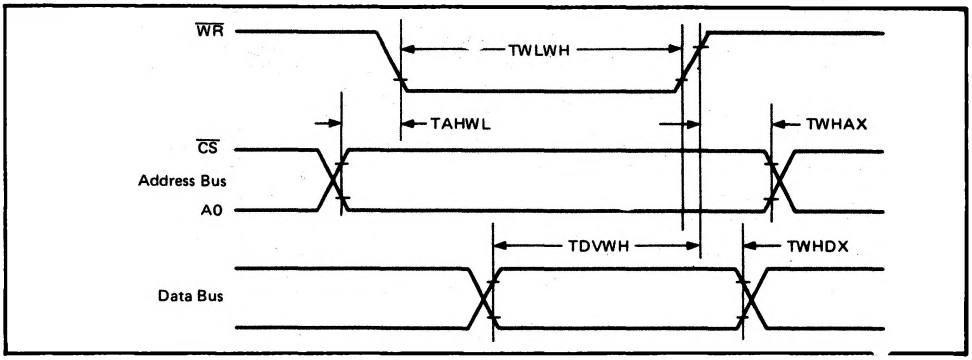
A.C. TESTING INPUT, OUTPUT WAVEFORM



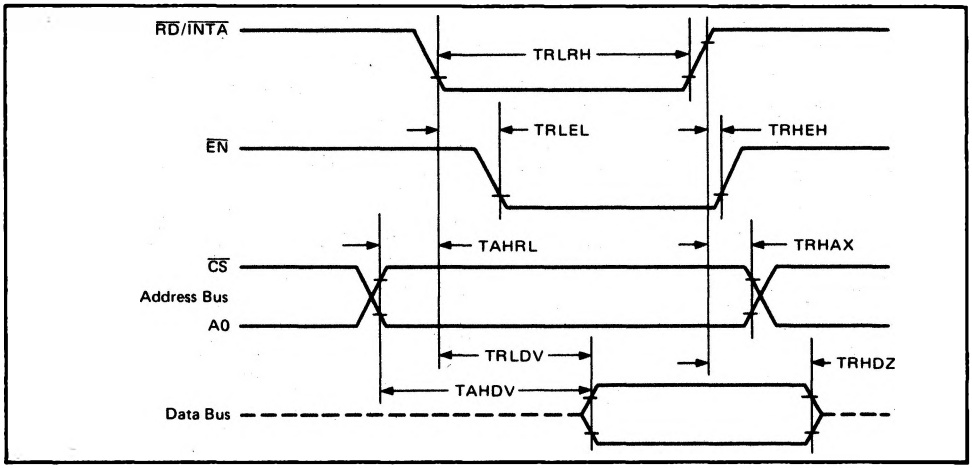
A.C. Testing: All input signals must switch between VIL-0.4V and VIH+0.4V. T_R and T_F must be less than or equal to 15 ns.

TIME CHART

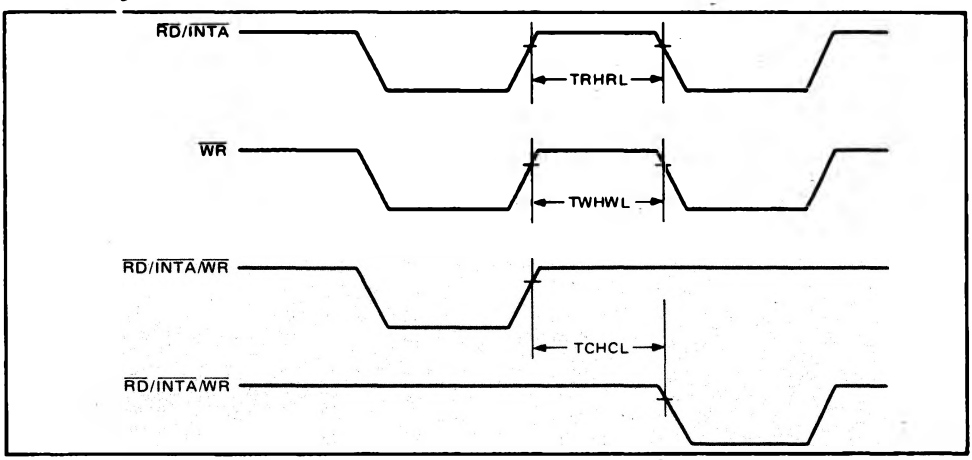
Write Timing



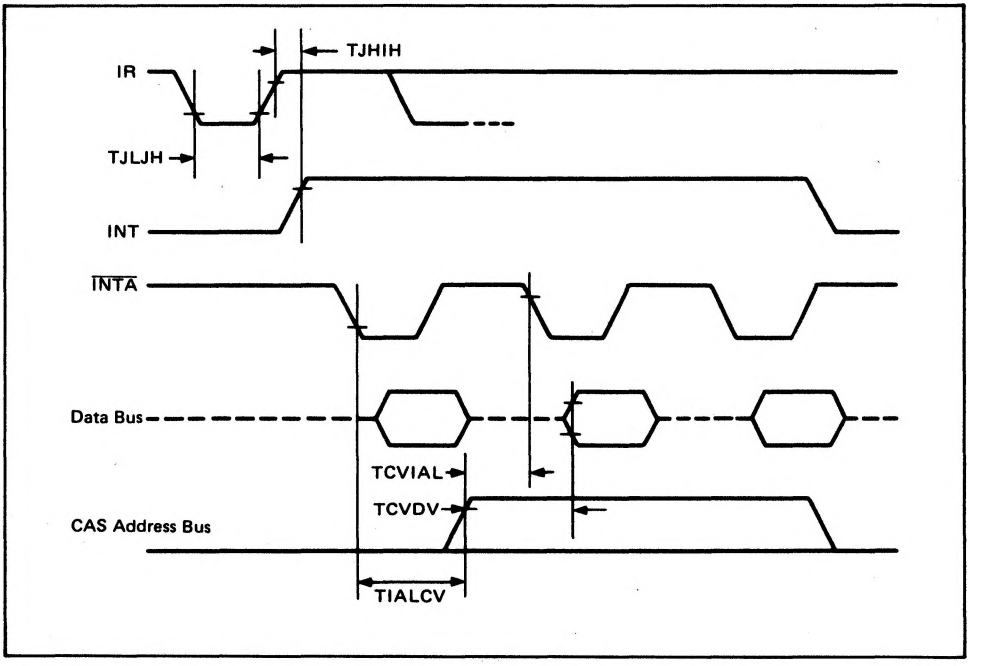
Read/INTA Timing



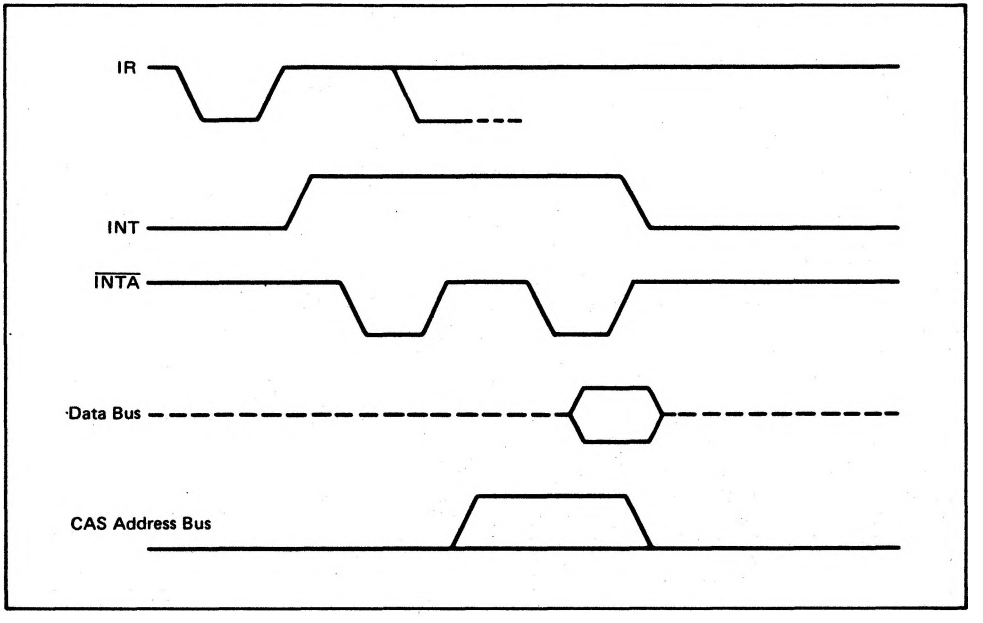
Other Timing



$\overline{\text{INTA}}$ Sequence (85 mode)



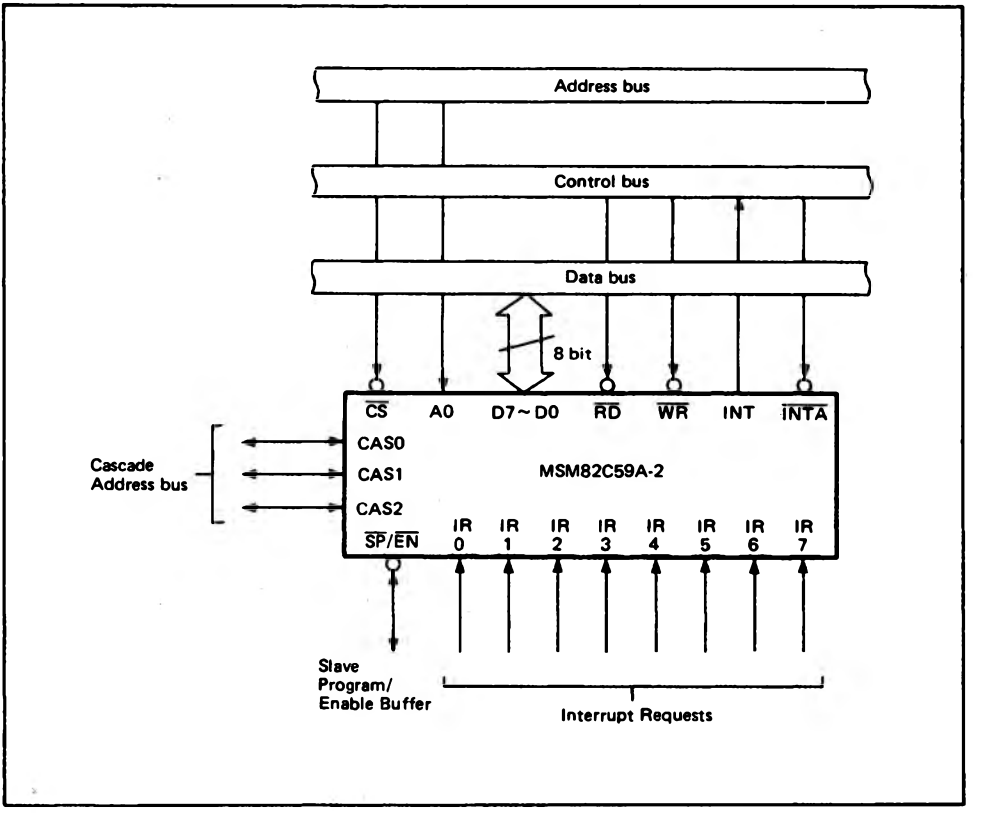
$\overline{\text{INTA}}$ Sequence (86 mode)



PIN FUNCTION DESCRIPTION

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	This 3-state 8-bit bidirectional data bus is used in reading status registers and writing command words through the $\overline{RD}$/$\overline{WR}$ signal from the CPU, and also in reading the CALL instruction code by the $\overline{INTA}$ signal from the CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled by $\overline{RD}$/$\overline{WR}$ when this pin is at low level. The data bus (D0 thru D7) is switched to high impedance when the pin is at high level. Note that $\overline{CS}$ does not effect $\overline{INTA}$.
$\overline{RD}$	Read input	Input	Data is transferred from the 82C59A to the CPU when this pin is at low level. IRR (Interrupt Request Register), ISR (In-Service Register), IMR (Interrupt Mask Register), or a Poll word is selected by OCW3 and A0.
$\overline{WR}$	Write input	Input	Commands are transferred from the CPU to the 82C59A when this pin is at low level.
A0	Address input	Input	This pin is used together with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals to write commands in the command registers, and to select and read status registers. This is normally connected to the least significant bit of the address bus. (A0 for 80C85A, and A1 for 80C86/88).
CAS0 ~ 2	Cascade address	Input/output	These pins are outputs when the 82C59A is used as the master, and inputs when used as a slave (in cascade mode). These pins are outputs when in single mode.
$\overline{SP}$/$\overline{EN}$	Slave program input/enable buffer output	Input/output	This dual function pin is used as an output to enable the data bus buffer in Buffered mode, and as an input for deciding whether the 82C59A is to be master ($\overline{SP}$/$\overline{EN}$ = 1) or a slave ($\overline{SP}$/$\overline{EN}$ = 0) during Non-buffered mode.
INT	Interrupt output	Output	When an interrupt request is made to the 82C59A, the INT output is switched to high level, and INT interrupt is sent to the CPU.
$\overline{INTA}$	Interrupt acknowledge input	Input	When this pin is at low level, the CALL instruction code or the interrupt vector data is enabled onto the data bus. When the CPU acknowledges the INT Interrupt, $\overline{INTA}$ is sent to the 82C59A. (Interrupt acknowledge sequence).
IR0 ~ 7	Interrupt request input	Input	These interrupt request input pins for the 82C59A can be set to edge trigger mode or level trigger mode (by ICW1). In edge trigger mode, interrupt request is executed by the rising edge of the IR input and holds it until that input is acknowledged by the CPU. In level trigger mode, interrupt requests are executed by high level IR inputs and holds them until that input is acknowledged by the CPU. These pins have a pull up resistor.

SYSTEM INTERFACE



BASIC OPERATION DESCRIPTION

Data transfers between the 82C59A internal registers and the data bus are listed below.

A0	D4	D3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function	Operation
0	X	X	0	1	0	IRR, ISR, or Poll word → Data bus	Read
1	X	X	0	1	0	IMR → Data bus	Read
0	0	0	1	0	0	Data bus → OCW2	Write
0	0	1	1	0	0	Data bus → OCW3	Write
0	1	X	1	0	0	Data bus → ICW1	Write
1	X	X	1	0	0	Data bus → OCW1, ICW2, ICW3, ICW4	Write
X	X	X	1	1	0	Data bus set to high impedance (when $\overline{INTA}$ = 1)	–
X	X	X	X	X	1		
X	X	X	0	0	X	Combinations prohibited	–

OPERATION DESCRIPTION

The 82C59A has been designed for real time interrupt driven microcomputer systems. The 82C59A is capable of handling up to 8 levels of interrupt requests, and can be expanded to cover a maximum of 64 levels when connected to other 82C59A devices.

Programming involves the use of system software in the same way as other microcomputer peripheral I/O devices. Selection of priority mode involves program execution, and enables the method of requesting interrupts to be processed by the 82C59A to be suitably configured for system requirements. That is, the priority mode can be dynamically updated or reconfigured during the main program at any time. A complete interrupt structure can be defined as required, based on the entire system environment.

(1) Functional Description of Each Block

Block name	Description of function
IRR, ISR	IR input line interrupts are processed by a cascaded interrupt request register (IRR) and the in-service register (ISR). The IRR stores all request levels where interrupt service is requested, and the ISR stores all interrupt levels being serviced.
Priority resolver	This logic block determines the priority level of the bits set in the IRR. The highest priority level is selected, and the corresponding ISR bit is set during $\overline{INTA}$ pulses.
Read/write logic	This block is capable of receiving commands from the CPU. These command words (ICW) and the operation command words (OCW) store the various control formats for 82C59A operations. This block is also used to transfer the status of the 82C59A to the Data Bus.
Cascade buffer comparator	This functional block is involved in the output and comparison of all 82C59A IDs used in the system. These three I/O pins (CAS0 thru CAS2) are outputs when the 82C59A operates as a master, and inputs when it operates as a slave. When operating as a master, the 82C59A sends a slave ID output to the slave where an interrupt has been applied. Furthermore, the selected slave sends the preprogrammed subroutine address onto the data bus during next one or two $\overline{INTA}$ pulses from the CPU.

(2) Interrupt Sequence

The major features of the 82C59A used in microcomputer systems are the programmability and the addressing capability of interrupt routines. This latter feature enables direct or indirect jumping to specific interrupt routines without polling the interrupt devices. The operational sequence during an interrupt varies for different CPUs.
The procedure for the 85 system (8085A/80C85A) is outlined below.

(i) One or more interrupt requests (IR0 thru IR7) becomes high, and the corresponding IRR bit is set.

(ii) The 82C59A evaluates these requests, and sends an INT signal to the CPU if the request is judged to be suitable.

(iii) The CPU issues an $\overline{INTA}$ output pulse upon reception of the INT signal.

(iv) Upon reception of the $\overline{INTA}$ signal from the CPU, the 82C59A releases the CALL instruction code (11001101) to the 8-bit data bus.

(v) A further two $\overline{INTA}$ pulses are then sent to the 82C59A from the CPU by this CALL instruction.

(vi) These two $\overline{INTA}$ pulses result in a preprogrammed subroutine address being sent from the 82C59A to the data bus. The lower 8-bit address is released by the first $\overline{INTA}$ pulse, and the higher 8-bit address is released by the second pulse.
The Falling Edge of the second $\overline{INTA}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.

(vii) 3-byte CALL instructions are thus released by the 82C59A. In Automatic End Of Interrupt (AEOI) mode, the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. In other cases, the ISR bit remains set until reception of a suitable EOI command at the end of the interrupt routine.

The procedure for the 86 system (80C86/88) is identical to the first three steps of the 85 system. The subsequent steps are described below.

(iv) Upon reception of the $\overline{INTA}$ signal from the CPU, the ISR bit with the highest priority is set, and the corresponding IRR bit is reset. In this cycle, the 82C59A sets the data bus to high impedance without driving the Data Bus.

(v) The CPU generates a second $\overline{INTA}$ output pulse, resulting in an 8-bit pointer to the data bus by the 82C59A.
The Falling Edge of the $\overline{INTA}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.

(vi) This completes the interrupt cycle. In AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. In other cases, the ISR bit remains set until reception of a suitable EOI command at the end of the interrupt routine.

If the interrupt request is cancelled prior to step (iv), that is, before the first $\overline{INTA}$ pulse has been received, the 82C59A operates as if a level 7 interrupt has been received, and the vector byte and CAS line operate as if a level 7 interrupt has been requested.

(3) Interrupt Sequence Output

85 Mode (80C85A)

The sequence in this case consists of three $\overline{INTA}$ pulses. A CALL operation code is released to the data bus by the first $\overline{INTA}$ pulse.

Contents of the first interrupt vector byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL code	1	1	0	0	1	1	0	1

The lower address of the interrupt service routine is released to the data bus by the second $\overline{INTA}$ pulse. If A5 ~ A7 is programmed with an address interval of 4, A0 ~ A4, is automatically inserted. And if A6 and A7 are programmed at an address interval of 8, A0 ~ A5 is automatically inserted.

Contents of the second interrupt vector byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

The higher address of the interrupt service routine programmed by the second byte (A8 ~ A15) of the initialization sequence is released to the data bus.

Contents of the third interrupt vector byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

86 Mode (80C86/88)

Apart from the two interrupt acknowledge cycles and the absence of a CALL operation code, the 86 mode is the same as the '85 mode. The first $\overline{INTA}$ cycle freezes interrupt status to resolve the priority internally in the same way as in 85 mode. When the device is used as a master, an interrupt code is issued to the cascade line at the end of the $\overline{INTA}$ pulse. During this first cycle, the data bus buffer is kept at high impedance without any data to the CPU. During the second $\overline{INTA}$ cycle, the 82C59A sends a byte of interrupt code to the CPU. Note that in 86 mode, the Address Interval (ADI) control status is ignored and A5 ~ A10 is not used.

Contents of interrupt vector byte in 86 system mode

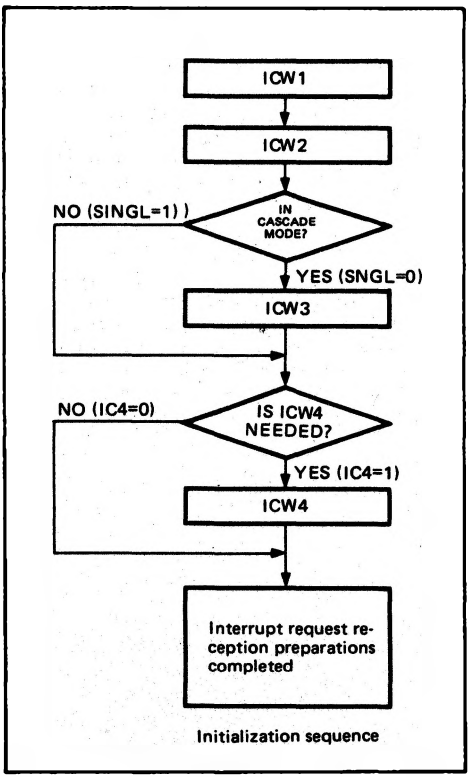
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

(4) Programming the 82C59A

The 82C59A receives two types of command words generaed by the CPU.

(i) Initialization Command Words (ICW1 thru ICW4)

Before commencing normal operations, each 82C59A in the system must be initialized by two to four $\overline{WR}$ pulse sequence.



Initialization sequence

(ii) Operation Command Words (OCW1 thru OCW3)

These commands are used in operating the 82C59A in the following modes.

a. Fully Nested Mode
b. Rotating Priority Mode
c. Special Mask Mode
d. Polled Mode

The OCW can be written into the 82C59A any time after initialization has been completed.

(5) Initialization Command Words (ICW1 thru ICW4)

When a command is issued with D4 = 1 and A0 = 0, it is always regarded as an Initialization Command Word 1 (ICW1). Starting of the initialization sequence by ICW1 results in automatic execution of the following steps.

a. The edge sense circuit is reset, and a low to high transition is necessary to generate an interrupt.
b. The interrupt mask register is cleared.
c. The IR7 input is assigned priority 7 (lowest priority)
d. Slave mode address is set to 7.
e. The Special Mask Mode is cleared, and the Status Read is set to IRR.
f. All ICW4 functions are cleared if IC4 = 0, resulting in a change to Non-Buffered mode, no-Auto EOI, and 85 mode.

Note: Master/slave in ICW4 can only be used in buffered mode.

(i) Initialization Command Words 1 and 2 (ICW1 and ICW2)

A4 thru A15: (Starting address of interrupt service routines)

In 85 mode, 8 request levels CALL 8 locations at equivalent intervals in the memory. The memory location interval can be set at this stage to 4 or 8 by program. (→ ADI) Hence, either 32 or 64 bytes/page respectively are used in the 8 routines.

The address format is 2 bytes long (A0 thru A15). When the routine interval is 4, A0 thru A4 is inserted automatically by the 82C59A, and A5 thru A15 is programmed externally. When the interval is 8, on the other hand, A0 thru A5 are inserted automatically by the 82C59A, and A6 thru A15 are programmed externally. In 86 mode, T3 thru T7 are inserted in the 5 most significant bits of the vector type, and the 82C59A sets the 3 least significant bits according to the interrupt level. A0 thru A10 are ignored, and the ADI (address interval) has no effect.

LTIM: The 82C59A is operated in level triggered mode when LTIM = 1, and the interrupt input edge circuit becomes disabled.

ADI: Designation of the CALL address interval. Interval = 4 when ADI = 1, and interval = 8 when ADI = 0.

SNGL: SNGL = 1 indicates the existence of only one 82C59A in the system. ICW3 is not required when SNGL = 1.

IC4: ICW4 is required when this bit is set, but not required when IC4 = 0.

(ii) Initialization Command Word 3 (ICW3)

This command word is written when there is more than one 82C59A used in cascade connections in the system, and is loaded into an 8-bit slave register. The functions of this slave register are listed below.

a. In a master mode system (BUF = 1 and M/S = 1 in ICW4 or $\overline{SP}/\overline{EN}$ = 1). "1" is set in each bit where a slave has been connected.
In 85 mode, the master 82C59A releases byte 1 of the CALL sequence to enable the corresponding slave to release byte 2 or 3 (only byte 2 in 86 mode) through the cascade line.

b. In slave mode (BUF = 1 and M/S = 0 in ICW4 or $\overline{SP}/\overline{EN}$ = 0). Bits 0 thru 2 identify the slave. The slave compares these bits with the cascade input, and releases bytes 2 and 3 of the CALL sequence (only byte 2 in 86 mode) if a matching result is obtained.

(iii) Initialization Command Word 4 (ICW4)

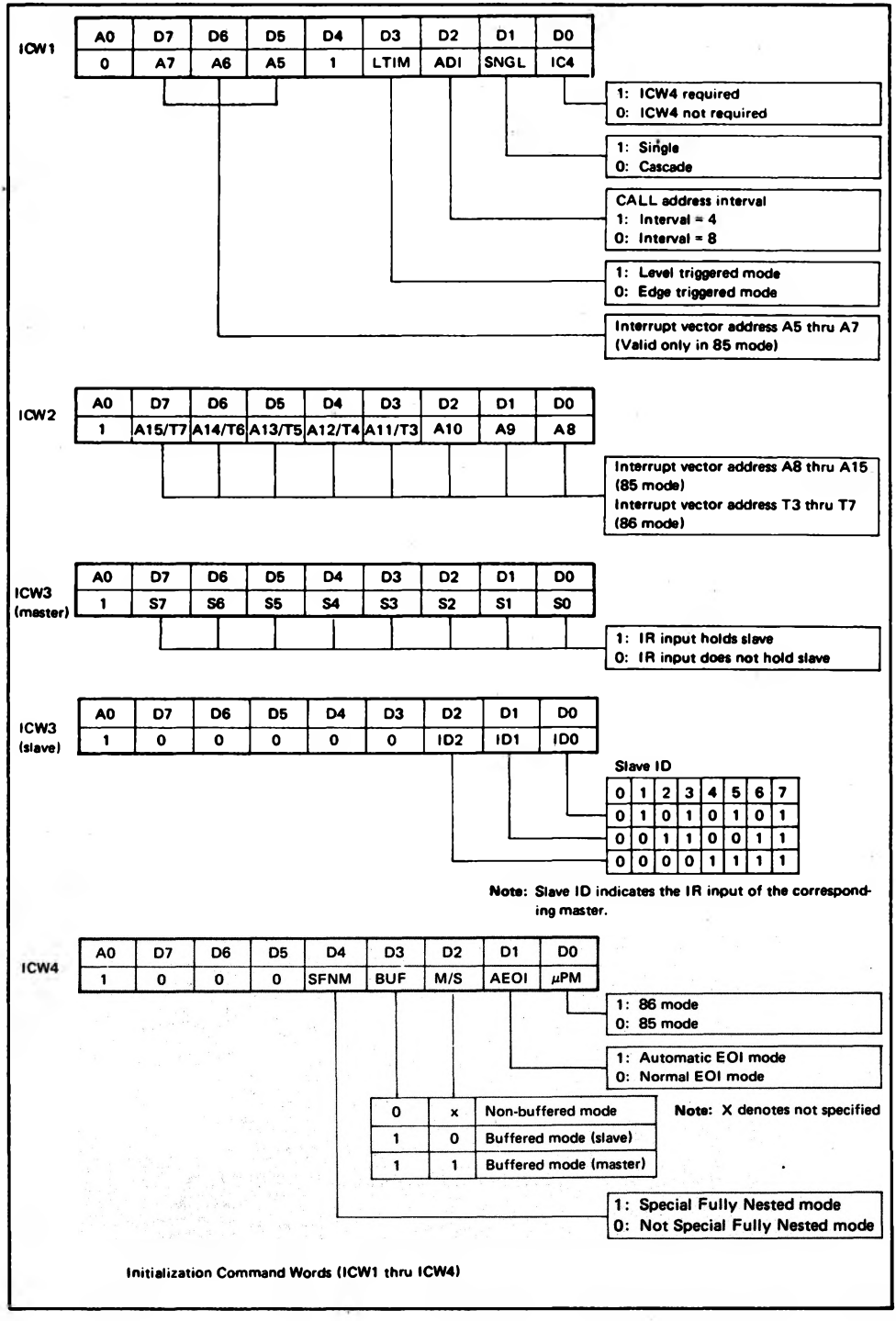
SFNM: Special Fully Nested Mode is programmed when SFNM = 1.

BUF: Buffered mode is programmed when BUF = 1. In Buffered mode, $\overline{SP}/\overline{EN}$ is an output, and Master/slave is selected by the M/S bit.

M/S: If buffered mode is selected, the 82C59A is programmed as the master when M/S = 1, and as a slave when M/S = 0. M/S is ignored, however, when BUF = 0.

AEOI: Automatic End Of Interrupt mode is programmed by AEOI = 1.

μPM: (Microprocessor mode)
The 82C59A is set to 85 system operation when μPM = 0, and to 86 system operation when μ PM = 1.



Initialization Command Words (ICW1 thru ICW4)

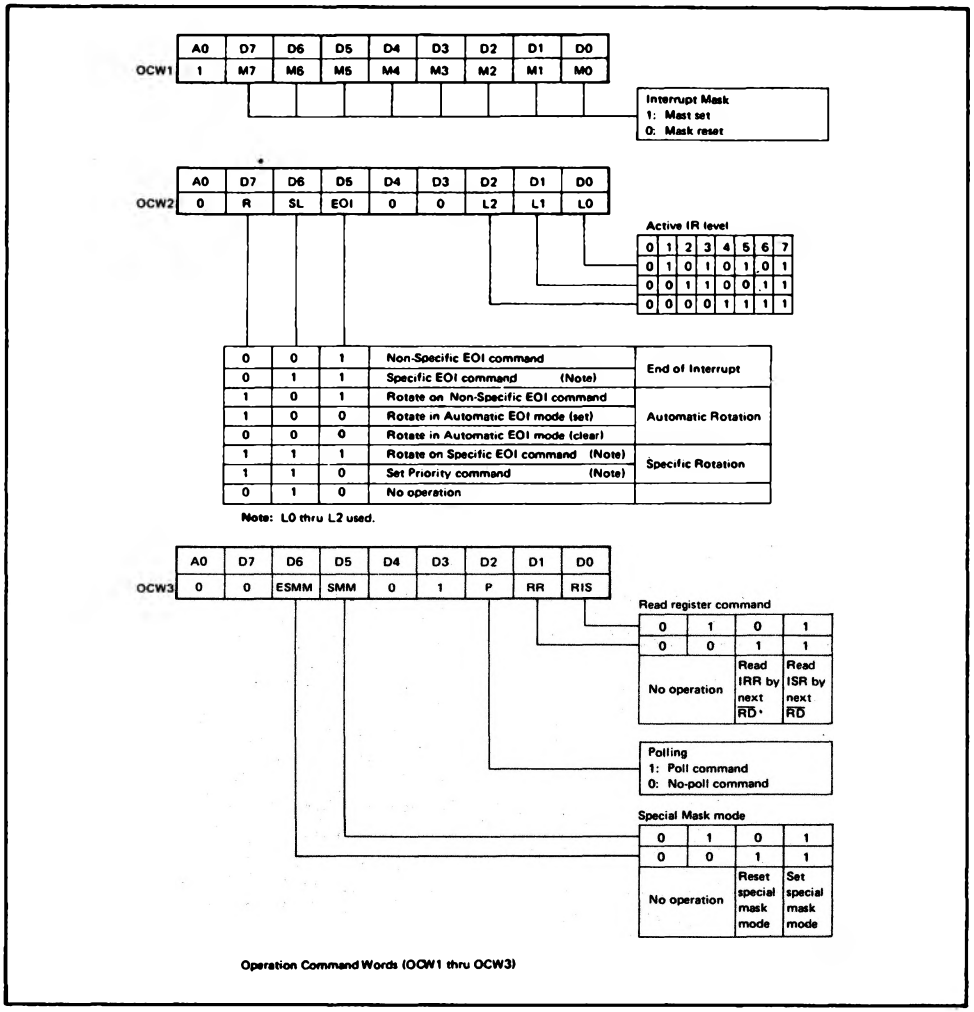
(6) Operation Command Words (OCW1 thru OCW3)

When Initialization Command Words (ICW) are programmed in the 82C59A, the interrupt input line is ready to receive interrupt requests. The Operation Command Words (OCWs) enable the 82C59A to be operated in various modes while the device is in operation.

(i) Operation Command Word 1 (OCW1)
OCW1 sets and resets the mask bits of the Interrupt Mask Register (IMR). M0 thru M7 represent 8 mask bits. The channel is masked when M = 1, but is enabled when M = 0.

(ii) Operation Command Word 2 (OCW2)
R, SL, EOI: The Priority Rotation and the End of Interrupt mode plus combinations of the two are controlled by combinations of these 3 bits. These combinations are listed in the operation command word format table.
L2, L1, L0: These bits indicate the specified interrupt level when SL = 1.

(iii) Operation Command Word 3 (OCW3)
ESMM: This enables the Special Mask Mode. The special mask mode can be set and reset by the SMM bit when ESMM = 1. The SMM bit is ignored when ESMM = 0.
SMM: (Special Mask Mode)
The 82C59A is set to Special Mask Mode when ESMM = 1 and SMM = 1, and is returned to normal mask mode when ESMM = 1 and SMM = 0. SMM is ignored when ESMM = 0.



Operation Command Words (OCW1 thru OCW3)

(7) Fully Nested Mode

As long as the 82C59A has not been programmed to another mode, this Fully Nested mode is set automatically after initialization. The interrupt requests are ordered in priority sequentially from 0 to 7 (where 0 represents highest priority). If an interrupt is then requested and is acknowledged highest priority, a corresponding vector address is released, and the corresponding bit in the in-service register (ISR) is set. The IS bit remains set until an End of Interrupt (EOI) command is issued from the microprocessor before returning from the interrupt service routine, or until the rising edge of the last $\overline{INTA}$ pulse arrives when the AEOI bit has been set.

When the IS bit is set, interrupts of the same or lower priority are inhibited - only interrupts of higher priority can be generated. In this case, interrupts can be ackowledged only when the internal interrupt enable F/F in the microprocessor has been enabled again through software. Following the initialization sequence, IR0 has the highest priority, and IR7 has the lowest. This priority can be changed by rotating priority mode in OCW2.

(8) End of Interrupt (EOI)

When the AEOI bit in ICW4 is set, the in-service (IS) bit is automatically reset by the rising edge of the last $\overline{INTA}$ pulse, or else is reset only when an EOI command is issued to the 82C59A prior to returning from the interrupt service routine.

And in cascade mode, the EOI command must be issued twice - once for the master, and once for the corresponding slave.

EOI commands are classified into specific EOI commands and Non-Specific EOI commands. When the 82C59A is operated in Fully Nested mode, the IS bit to be reset can be determined on EOI. If the Non-Specific EOI command is issued, the highest IS bit of those that are set is reset automatically, because the highest IS level is always the last servicing level in the Fully Nested mode. If, however, it is not in the fully Nested mode, the 82C59A will no longer be able to determine the last acknowledged level. In this case, it will be necessary to issue a Specific EOI which includes the IS level to be reset as part of the command. When the 82C59A is in Special Mask mode, care must be taken to ensure that IS bits masked by the IMR bit can not reset by the Non-Specific EOI.

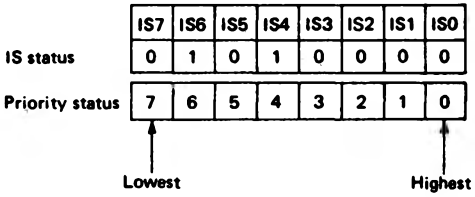
(9) Automatic End of Interrupt (AEOI) Mode

When AEOI = 1 in ICW4, the 82C59A continues to operate in AEOI mode until programmed again by ICW4. In this mode, the 82C59A automatically performs Non-Specific EOI operation at the rising edge of the last $\overline{INTA}$ pulse (the third pulse in 85 systems, and the second pulse in 86 systems). In terms of systems, this mode is best used in nested multiple level interrupt configurations. It is not necessary when there is only one 82C59A. AEOI mode is only used in a master 82C59A device, not in a slave.

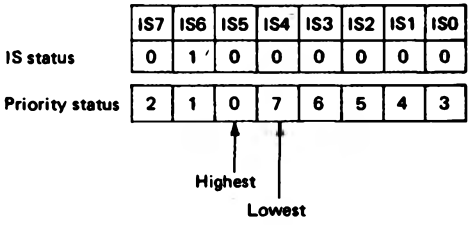
(10) Automatic Rotation (Devices with Equal Priority)

In some applications, there is often a number of devices with equal priority. In this mode, the device where an interrupt service has just been completed is set to the lowest priority. At worst, therefore, a particular interrupt request device may have to wait for seven other devices to be serviced at least once each. There are two methods for Automatic Rotation using OCW2 - Rotation on Non-Specific EOI command, and Rotation in Automatic EOI mode.

Before Rotation (IR4 the highest priority requesting service)



After Rotation (IR4 was serviced, all other priorities rotated correspondingly)



(11) Specific Rotation (Specific Priority)

All priority levels can be changed by programming the lowest priority level (Set Priority Command in OCW2). For example, if IR5 is programmed as the device of lowest priority, IR6 will have the highest priority. In this mode, the internal status can be updated during OCW2 by software control. This is unrelated, however, to the EOI command in the same OCW2.

Priority level can also be changed by using the OCW2 Rotate On Specific EOI command.

(12) Interrupt Mask

Interrupt inputs can be masked individually by Interrupt Mask Registers (IMR) programmed through the OCW1. Each interrupt channel is masked (disabled) when the respective IMR bit is set to "1". IR0 is masked by bit 0, and IR1 is masked by bit 1. Masking of any particular channel has no effect on other channels.

(13) Special Mask Mode

In some applications, there is a need for dynamic updating of the system's priority level structure by software control during execution of an interrupt service routine. For example, it may be necessary to inhibit the lower priority requests for part of the execution of a certain routine while enabling for another part. In this case, it is difficult to enable all lower priority requests if the IS bit has not yet been reset by the EOI command after an interrupt request has been acknowledged (during execution of a service routine). All of these requests would normally be disabled.

Hence the use of the Special Mask mode. When a mask bit is set by OCW1 in this mode, the corresponding interrupt level requests are disabled. And all other unmasked level requests (at both higher and lower priority levels) are enabled. Interrupts can thus be enabled selectively by loading the mask register.

In this mode, the specific EOI Command should be used.

This Special Mask mode is set by OCW3 ESMM = 1 and SMM = 1, and reset by ESMM = 1 and SMM = 0.

(14) POLL Command

In this mode, the INT output in not used, the internal interrupt enable F/F of the microprocessor is reset, and interrupt inputs are disabled. Servicing the I/O device is executed by software using the Poll command.

The Poll command is issued by setting P in OCW3 to "1". The 82C59A regards the next $\overline{RD}$ pulse as reception of an interrupt, and if there is a request, the corresponding IS bit is set and the priority level is read out. Interrupts are frozen between $\overline{WR}$ and $\overline{RD}$.

	D7	D6	D5	D4	D3	D2	D1	D0
Poll word	1	0	0	0	0	W2	W1	W0

W0 thru W2: Binary coded highest priority level of service being requested.

1: Set to "1" when there is an interrupt.

This mode is useful when there is a common routine for a number of levels, and the $\overline{INTA}$ sequence is not required. ROM space can thus be saved.

(15) Reading 82C59A Status

The status of a number of internal registers can be read out for updating user information on the system. The following registers can be read by means of OCW3 (IRR and ISR) and OCW1 (IMR).

a. IRR: (Interrupt Request Register) 8-bit register for storing interrupt requesting levels.

b. ISR: (In-Service Register) 8-bit register for storing priority levels being serviced.

c. IMR: (Interrupt Mask Register) 8-bit register for storing interrupt request lines to be masked.

The IRR can be read when a Read Register Command is issued with OCW3 (RR = 1 and RIS = 0) prior to the $\overline{RD}$ pulse, and the ISR can be read when a Read Register Command is issued with OCW3 (RR = 1 and RIS = 1) prior to the $\overline{RD}$ pulse. And as long as the read status does not change, OCW3 is not required each time before the status is read. This is because the 82C59A remembers whether IRR or ISR was selected by the previous OCW3. But this is not true when poll is used.

The 82C59A is set to IRR after initialization. OCW3 is not required to read IMR. IMR is issued to the data bus if $\overline{RD}$ = 0 and A0 = 1 (OCW1).

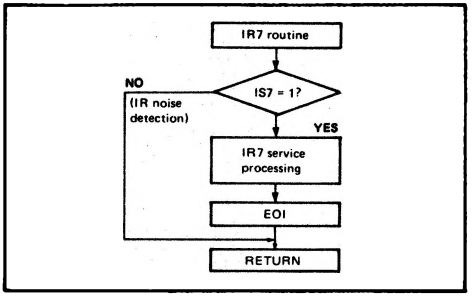
Reading status is disabled by polling when P = 1 and RR = 1 in OCW3.

(16) Edge and Level Trigger Mode

This mode is programmed by using bit 3 (LTIM) in ICW1. When LTIM = 0, the interrupt request is recognized by the IR input transition from Low to High. As long as the IR input is kept at High, no other interrupt is generated. Since interrupt requests are recognized by the IR input "H" level when LTIM = 1, edge detection is not required.

The interrupt request must be cancelled before output of the EOI command, and before the interrupt is enabled in order to prevent the generation of a second interrupt by the CPU.

The IR input must be held at High level until the falling edge of the first $\overline{INTA}$ pulse, irrespective of whether edge sense or level sense is employed. If the IR input is switched to Low level before the first $\overline{INTA}$ pulse, the default IR7 is generated when the interrupt is acknowledged by the CPU. This can be an effective safeguard to be adopted to detect interrupts generated by the noise glitches on the IR inputs. To take advantage of this feature, the IR7 routine is used as a "clean up" routine where the routine is simply executing a return instruction and the interrupt is subsequently ignored. When the IR7 is required for other purposes, the default IR7 can be detected by reading the ISR. Although correct IR7 interrupts involve setting of the corresponding ISR bit, the default IR7 is not set.



(17) Special Fully Nested Mode

This mode is used in large systems where the cascade mode is used and the respective Interrupt Requests within each slave have to be given priority levels. In this case, the Special Fully Nested mode is programmed to the master by using ICW4. This mode is practically identical to the normal Fully Nested mode, but differs in the following two respects.

a. When an interrupt request is received from a particular slave during servicing, a new interrupt request from an IR with a higher priority level than the interrupt level of the slave being serviced is recognized by the master and the interrupt is applied to the processor without the master priority logic being inhibited by the slave. In normal Fully Nested mode, if the request is in service, a slave is masked and no other requests can be recognized from the same slave.

b. When exiting from an interrupt service routine, it is first necessary to check whether or not the interrupt which has just been serviced by software was the only interrupt from that slave. This is done by sending a Non-Specific EOI command to that slave, followed by reading of the In-Service Register (ISR) to see whether that register has become all '0'. A Non-Specific EOI is sent to the master too if the ISR is empty, and if not no EOI should be sent.

(18) Buffered Mode

Control for buffer enabling is required when the 82C59A is used in a large system where a data bus drive buffer is needed and cascade mode is used. When buffered mode is selected, the 82C59A sends an enable signal on the $\overline{SP}/\overline{EN}$ pin to enable the buffer. In this mode, the $\overline{SP}/\overline{EN}$ output always becomes active while the 82C59A's data bus output is enabled. Therefore, the 82C59A requires programming to enable it to distinguish master from slave. Buffered mode is programmed by bit 3 in ICW4, and the ability to distinguish master from slave is programmed by bit 2 in ICW4.

(19) Cascade Mode

To enable the 82C59A to handle up to 64 priority levels, a maximum of 8 slaves can be easily connected to one master device.

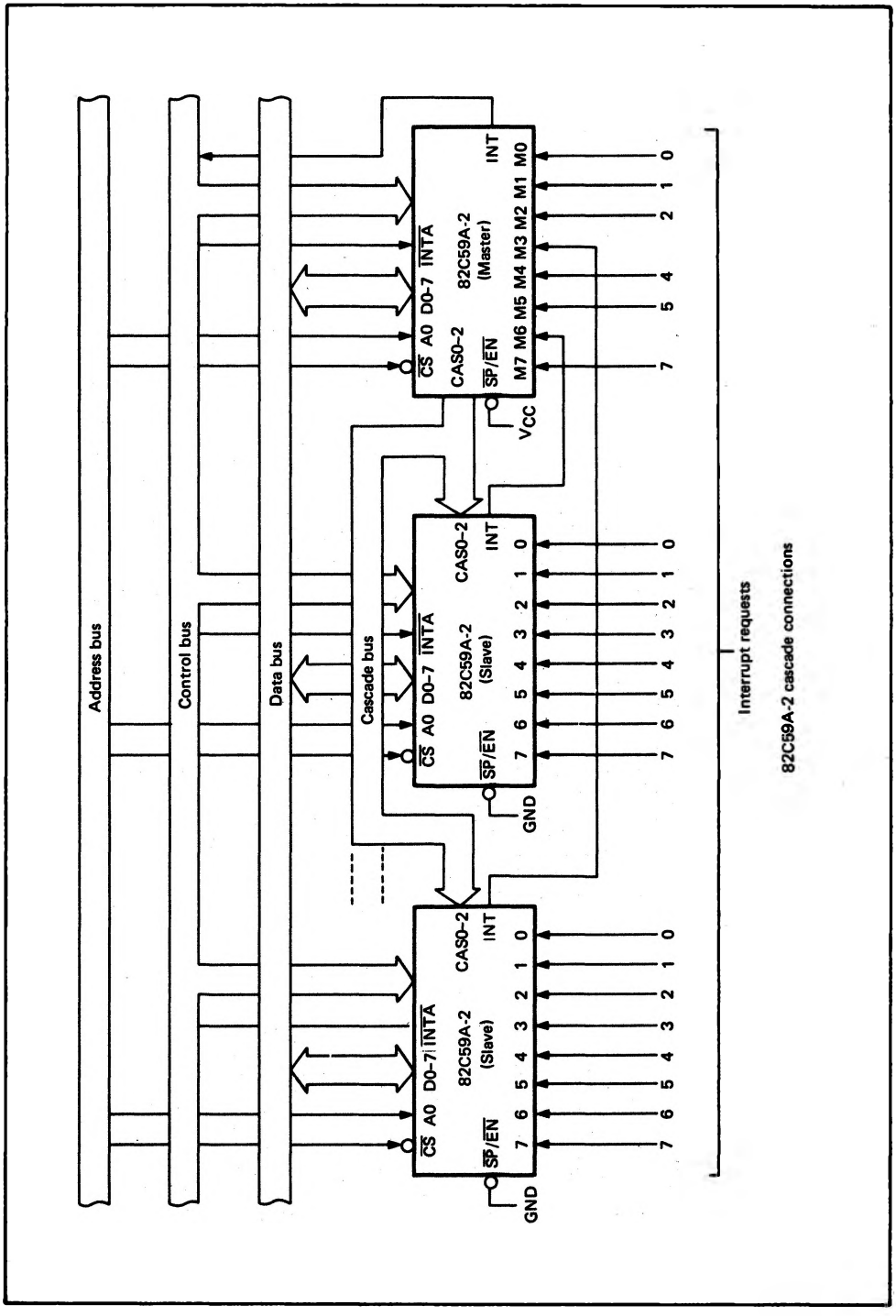
The master controls the slaves through three cascade lines, the cascade bus executes like a slave chip select during the $\overline{INTA}$ sequence.

In cascade configuration, slave interrupt outputs (INT) are connected to master interrupt request inputs (IR). When a slave IR becomes active and is acknowledged, the master enables the corresponding slave to release the routine address for that device during bytes 2 and 3 (only byte 2 in 86 mode) of the $\overline{INTA}$ sequence.

The cascade bus line is normally kept at low level, and holds the slave address during the period from the rising edge of the first $\overline{INTA}$ pulse up to the rising edge of the third $\overline{INTA}$ pulse (or the second $\overline{INTA}$ pulse in 86 mode).

Each 82C59A device in the system can operate in different modes in accordance with their initialization sequences. EOI commands must be issued twice, once for the master once for the corresponding slave. Each 82C59A requires an address decoder to activate the respective chip select (CS) inputs.

Since the cascade line is normally kept at low level, note that slaves must be connected to the master IR0 only after all slaves have been connected to the other IRs.


Address bus
Control bus
Data bus
Cascade bus
82C59A-2 (Master)
82C59A-2 (Slave)
82C59A-2 (Slave)
CS A0 D0-7 INTA
SP/EN
CAS0-2
INT
M7 M6 M5 M4 M3 M2 M1 M0
7 6 5 4 3 2 1 0
VCC
GND
Interrupt requests
82C59A-2 cascade connections