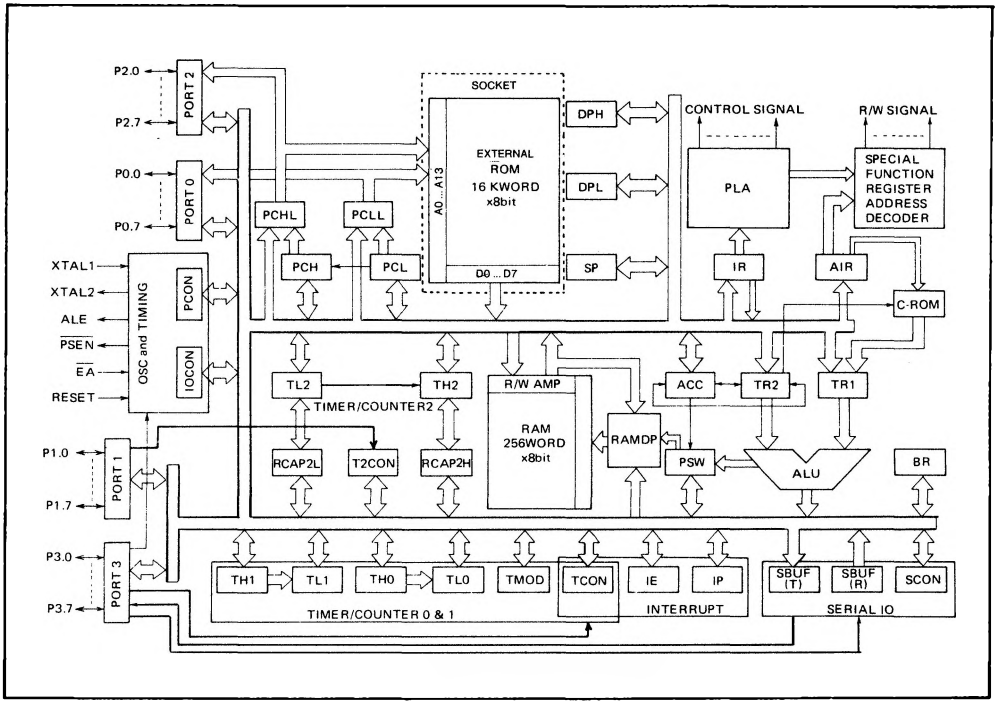
OKI semiconductor

MSM85C154VS

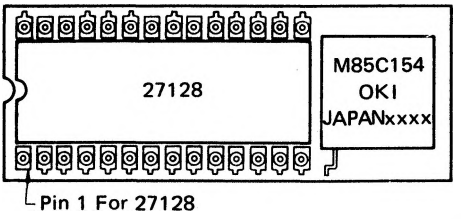
M83C154/M80C51F PIGGY BACK

GENERAL DESCRIPTION

The MSM85C154 is a device whose built-in ROM is replaced by external EPROM using the piggy-back method. External EPROM capacity is up to 16K bytes. It can be used for evaluation of programs for MSM83C154 and MSM80C51F.



INSTALLATION METHOD FOR EXTERNAL ROM



* The MSM85C154VS pin layout of bottom side is the same as the pin layout for MSM83C154-XXRS.

*NOTE

MSM85C154VS piggy back is originally designed for the programming of MSM83C154 and it covers the function as the piggy back for MSM80C51F.
Please be careful not to use additional function which dedicated to MSM83C154 in usig the piggy back for MSM80C51. The function, flag, and resistor listed below are dedicated to MSM83C154.

- ICON (0F8H) : I/O CONTROL RESISTOR
- TH2 (0CDH) : TIMER 2. UPPER SIDE RESISTOR
- TL2 (0CCH) : TIMER 2. LOWER SIDE RESISTOR
- RCAP2H (0CBH) : CAPTURE RESISTOR. UPPER SIDE
- RCAP2L (0CAH) : CAPTURE RESISTOR. LOWER SIDE
- T2CON (0C8H) : TIMER CONTROL RESISTOR 2
- IP (0B8H) : INTERRUPT PRIORITY RESISTOR 2
  bit 5 (Bit address BDH) PT2
  bit 7 (Bit address BFH) PCT
- IE (0A8H) : INTERRUPT ENABLE RESISTOR
  bit 5 (Bit address ADH) ET2
- PCON (087H) : POWER CONTROL RESISTOR
  bit 5 (Bit address Nil) RPD
  bit 6 (Bit address Nil) HPD

In using this piggy back for MSM80C51F, do not set the above items (Control bit should not be "1").
All bits are set to "0" at initial reset.

In high temperature atmosphere, malfunction may happen (output latches of the Port 0 are set when interrupt occurs) in writing the instruction code of which LSB is "0" at address 0 of the EPROM.
To avoid this problem, please be sure to write AJMP instruction (operational code is X1) at address 0 instead of LJMP instruction (operational code is 02).

Operating frequency is from DC to 12MHz.

The MSM85C154VS has been developed assuming that it is used for evaluation of program. Please use the MSM83C154 (mask ROM version) as the devices installed on a product.