MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Ultra-Low Supply Voltage (ULV) Range**
  - **0.9 V to 1.5 V (1 MHz)**
  - **1.5 V to 1.65 V (4 MHz)**
- **Low Power Consumption**
  - **Active Mode (AM): 45 µA/MHz (1.3 V)**
  - **Standby Mode (LPM3, WDT_A Mode): 6 µA**
  - **Off Mode (LPM4): 3 µA**
- **Wake-Up From LPMx in Less Than 5 µs**
- **16-Bit RISC Architecture**
  - **Extended Instructions**
  - **Up to 4-MHz System Clock**
- **Compact Clock System**
  - **1-MHz Internal Trimmable High-Frequency Clock**
  - **20-kHz Internal Low-Frequency Clock Source**
  - **External Clock Input**
- **16-Bit Timer0_A3 With Three Capture/Compare Registers**
- **16-Bit Timer1_A3 With Three Capture/Compare Registers**
- **ULV Analog Pool Modes**
  - **8-Bit Analog-to-Digital Converter (ADC)**
  - **8-Bit Digital-to-Analog Converter (DAC)**
  - **Programmable Comparator (COMP)**
  - **Supply Voltage Monitor (SVM)**
  - **Temperature Sensor**
  - **Internal Reference Voltage Source**
- **ULV Port Logic**
  - **V_{OL} Better Than 0.15 V at 2.5 mA**
  - **V_{OH} Better Than V_{CC} – 0.15 V at 1 mA**
  - **Timer0 PWM Signal Available on All Ports**
  - **Timer1 PWM Signal Available on All Ports**
- **ULV Brownout Circuit (BOR)**
- **ULV RAM Retention Voltage Below BOR Level**
- **32-Bit Watchdog Timer (WDT-A)**
- **Bootstrap Loader in MSP430L092 Development/Prototyping Device**
- **Full Four-Wire JTAG Debug Interface**
- **Family Members Include**
  - **MSP430C091**
    - **1KB ROM Memory**
    - **128 Bytes RAM + 96 Bytes CRAM (Lockable)**
  - **MSP430C092**
    - **2KB ROM Memory**
    - **128 Bytes RAM + 96 Bytes CRAM (Lockable)**
  - **MSP430L092**
    - **2KB Loader ROM With Service Functions**
    - **2KB RAM (1792 + 128 + 96 Bytes Lockable)**
- **For Complete Module Descriptions, See the *MSP430x09x Family User's Guide* (SLAU321)**

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled internal oscillators allow wake-up from low-power modes to active mode in less than 5 µs.

The MSP430C09x and MSP430L092 series are microcontroller configurations with two 16-bit timers, an ultra-low-voltage 8-bit analog-to-digital (A/D) converter, an 8-bit digital-to-analog (D/A) converter, and up to 11 I/O pins.

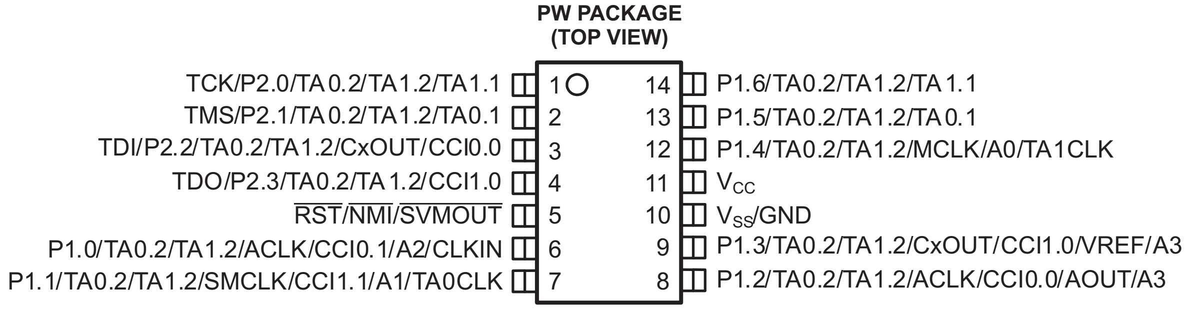
Typical applications for this device include single-cell systems requiring a full analog signal chain.

ORDERING INFORMATION(1)

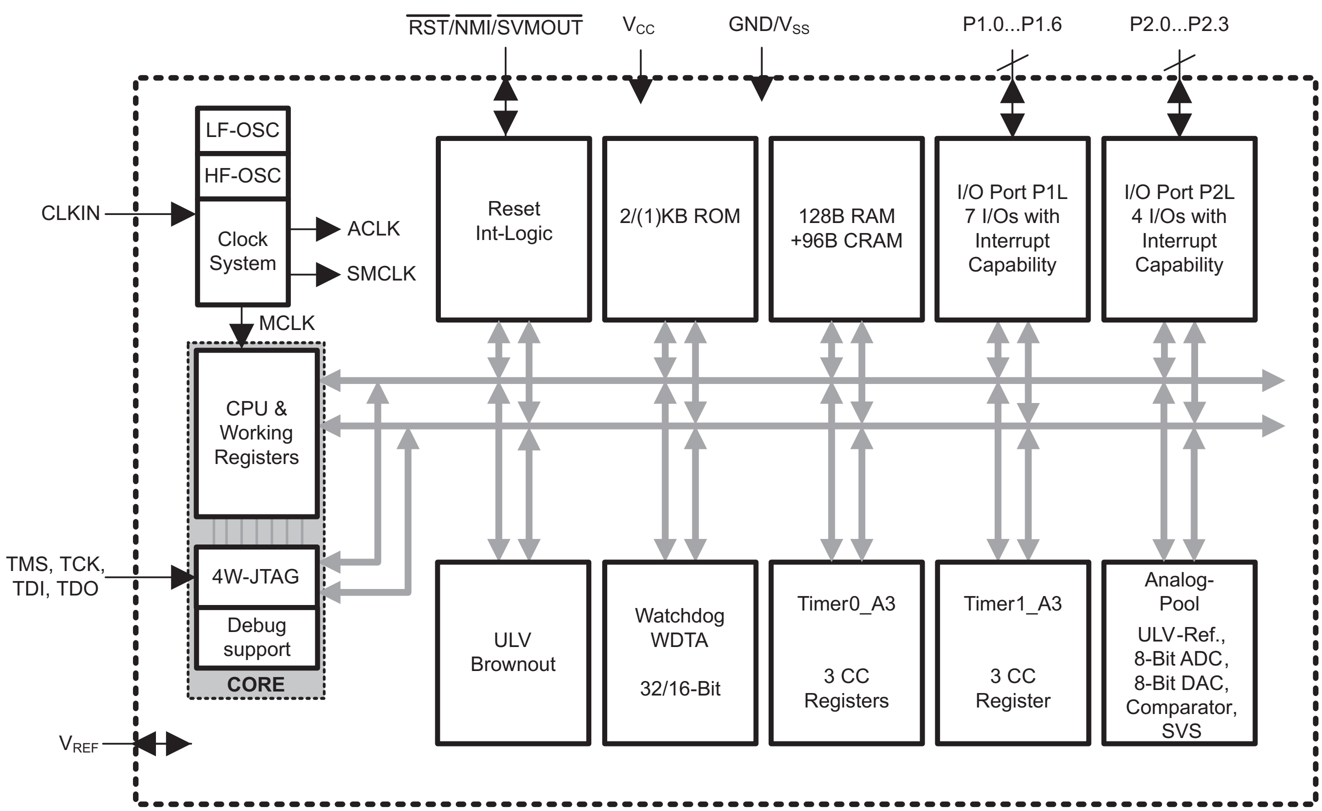
T_A	PACKAGED DEVICES(2) PLASTIC 14-PIN TSSOP (PW)
0ºC to 50ºC	MSP430C091SPW
	MSP430C092SPW
	MSP430L092SPW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.

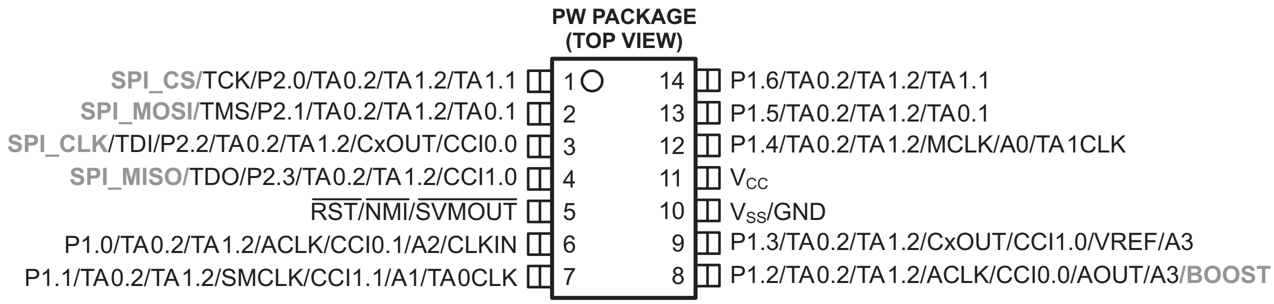
Pin Designation, MSP430C091PW, MSP430C092PW



Functional Block Diagram, MSP430C092PW, MSP430C091PW



Pin Designation, MSP430L092PW



Functional Block Diagram, MSP430L092PW

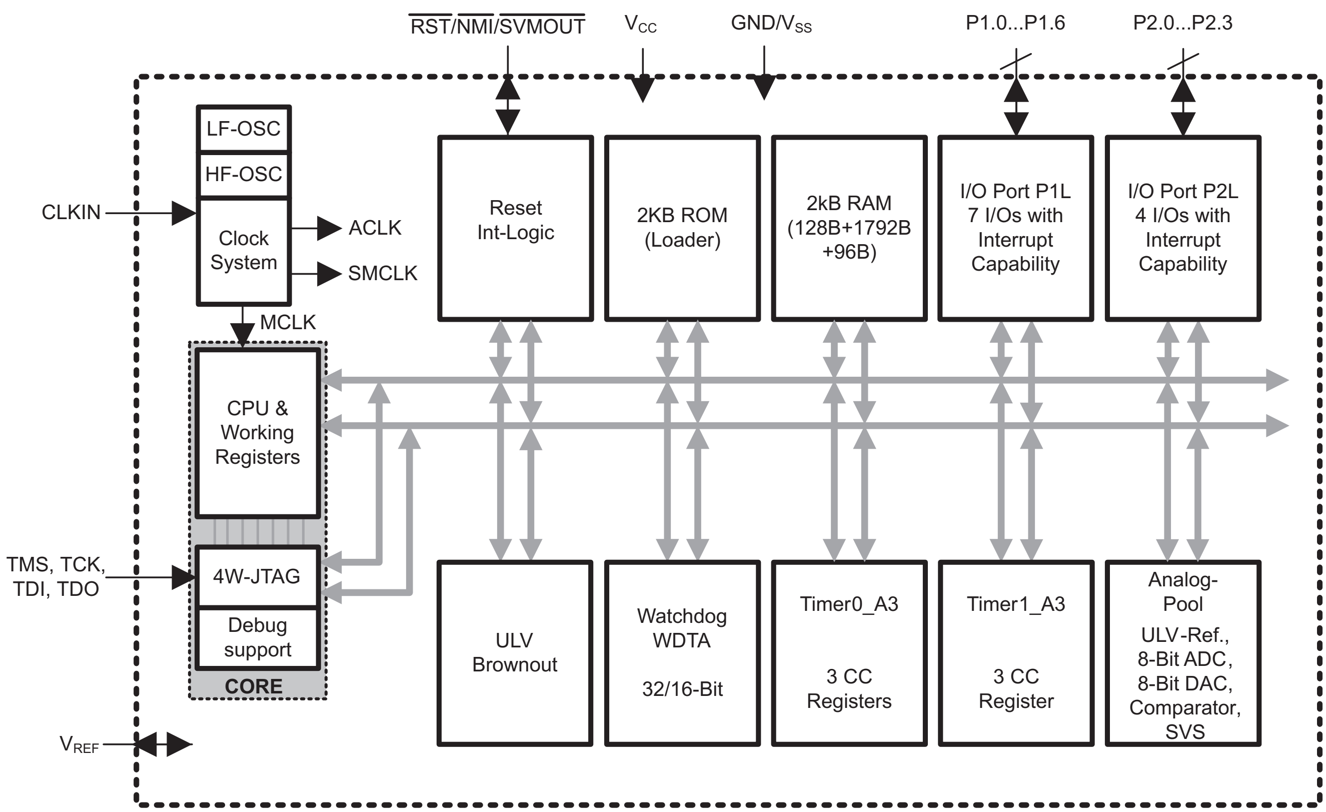


Table 1. Terminal Functions

TERMINAL		I/O (1)	DESCRIPTION
NAME	NO.		
TCK/P2.0/TA0.2/TA1.2/TA1.1	1	I/O	JTAG test clock General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output Timer1_A3 Out1 output Timer0_A3 CCR2 capture: CCI2A input, compare Timer1_A3 CCR2 capture: CCI2A input, compare
TMS/P2.1/TA0.2/TA1.2/TA0.1	2	I/O	JTAG test mode select General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output Timer0_A3 Out1 output Timer0_A3 CCR2 capture: CCI2B input, compare Timer1_A3 CCR2 capture: CCI2B input, compare
TDI/P2.2/TA0.2/TA1.2/CCI0.0/CxOUT	3	I/O	JTAG test data input General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output Comparator output Timer0_A3 CCR0 capture: CCI0A input, compare Test clock input
TDO/P2.3/TA0.2/TA1.2/CCI1.0	4	I/O	JTAG test data output General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output Timer1_A3 CCR0 capture: CCI0A input, compare
$\overline{\text{RST}}$/$\overline{\text{NMI}}$/$\overline{\text{SVMOUT}}$	5	I/O	Reset input active low Non-maskable interrupt input SVM output
P1.0//TA0.2/TA1.2/ACLK/CCI0.1/A2/CLKIN	6	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output ACLK output Timer0_A3 CCR1 capture: CCI1B input, compare Analog input A2 – A-Pool Input terminal for external clock
P1.1/TA0.2/TA1.2/SMCLK/CCI1.1/A1/TA0CLK	7	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output SMCLK output Timer1_A3 CCR1 capture: CCI1B input, compare Analog input A1 – A-Pool Timer0_A3 clock signal TACLK input

(1) I = input, O = output, N/A = not available on this package offering

Table 1. Terminal Functions (continued)

TERMINAL		I/O (1)	DESCRIPTION
NAME	NO.		
P1.2/TA0.2/TA1.2/ACLK/CCI0.0/AOUT/A3	8	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output ACLK output Timer0_A3 CCR0 capture: CCI0B input, compare Analog input A3 – A-Pool Analog output – A-Pool
P1.3/TA0.2/TA1.2/CxOUT/CCI1.0/VREF/A3	9	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output Comparator output Timer1_A3 CCR0 capture: CCI0B input, compare Analog input A3 – A-Pool Reference voltage input / output
V_{SS}/GND	10		Analog and digital power supply ground reference
V_{CC}	11		Analog and digital power supply
P1.4/TA0.2/TA1.2/MCLK/A0/TA1CLK	12	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 Out2 output MCLK Output Analog input A0 – A-Pool
P1.5/TA0.2/TA1.2/TA0.1	13	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 OUT2 output Timer0_A3 OUT1 output Timer0_A3 CCR1 capture: CCI1A input, compare
P1.6/TA0.2/TA1.2/TA1.1	14	I/O	General-purpose digital I/O Timer0_A3 Out2 output Timer1_A3 OUT2 output Timer1_A3 OUT1 output Timer1_A1 CCR1 capture: CCI1A input, compare

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 2 shows examples of the three types of instruction formats, Table 3 shows the address modes.

Table 2. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 → R5
Single operands, destination only	e.g., CALL R8	PC→(TOS), R8 →PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 3. Address Mode Descriptions

ADDRESS MODE	S (1)	D (1)	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	•	•	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	•	•	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	•		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) → R11 R10 + 2→ R10
Immediate	•		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

(1) S = source D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active for all sources
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active (for LF oscillator and CLKIN as source, HF oscillator is mapped to LF oscillator as source)
  - MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active for all sources
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK remains active (for LF oscillator and CLKIN as source, HF oscillator is mapped to LF oscillator as source)
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - MCLK is disabled
  - SMCLK is disabled
  - ACLK is disabled
  - Oscillators are stopped

LPM2 vs LPM3

If only MCLK is feed by the HF oscillator (SELA ≠ 00, SELS ≠ 00, SELM = 00 of CCSCTL4 register) the following behavior is implemented:

- Entering LPM2 turns off the HF oscillator and starts again with the HF oscillator selected for MCLK
- Entering LPM3 turns off the HF oscillator and starts again with the LF oscillator selected for MCLK

The only difference between LPM2 and LPM3 is the selection of the source for MCLK when re-entering active mode and, therefore, and the level of power savings.

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 4. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog	WDTIFG(1)	Reset	0x0FFFE	15, highest
System NMI Vacant memory access	SVMIFG, VMAIFG(1)	(Non)maskable	0x0FFFC	14
User NMI NMI	NMIIFG(1)(2)	(Non)maskable	0x0FFFA	13
Timer1_A3	TA1CCR0 CCIFG0(3)	Maskable	0x0FFF8	12
Timer1_A3	TA1CCR1 CCIFG1(1)(3)	Maskable	0x0FFF6	11
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0x0FFF4	10
A-Pool	CxIFG	Maskable	0x0FFF2	9
I/O Port P1	P1IFG.0 to P1IFG.6(1)(3)	Maskable	0x0FFF0	8
Timer0_A3	TA0CCR0 CCIFG0(3)	Maskable	0x0FFEE	7
Timer0_A3	TA0CCR1 CCIFG1(1)(3)	Maskable	0x0FFEC	6
I/O Port P2	P2IFG.0 to P2IFG.3(1)(3)	Maskable	0x0FFEA	5
Reserved	Reserved(4)		0x0FFE8	4
			⋮	⋮
			0x0FFE0	0

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Special Function Registers (SFRs)

The MSP430 SFRs are located in the lowest address space and can be accessed via word or byte formats.

Legend	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	(shaded)	SFR bit is not present in device.

Interrupt Enable 1

15	14	13	12	11	10	9	8
							SVMIE
r0	r0	r0	r0	r0	r0	r0	rw-0

7	6	5	4	3	2	1	0
JMBOUTIE	**JMBINIE**		**NMIIE**	**VMAIE**		**OFIE**	**WDTIE**
rw-0	rw-0	r0	rw-0	rw-0	r0	rw-0	rw-0

SVMIE	SVM interrupt enable
JMBOUTIE	
JMBINIE	
NMIIE	Nonmaskable-interrupt enable
VMAIE	Vacant memory access interrupt enable
OFIE	
WDTIE	Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

Interrupt Enable 2

15	14	13	12	11	10	9	8
							SVMIFG
r0	r0	r0	r0	r0	r0	r0	rw-0

7	6	5	4	3	2	1	0
JMBOUTIFG	**JMBINIFG**		**NMIIFG**	**VMAIFG**		**OFIFG**	**WDTIFG**
rw-0	rw-0	r0	rw-0	rw-0	r0	rw-0	rw-0

SVMIFG	Set by SVM when voltage falls below set voltage
JMBOUTIFG	
JMBINIFG	
NMIIFG	Set via $\overline{RST}/\overline{NMI}$ pin
VMAIFG	Set on vacant memory access
OFIFG	
WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation Reset on V_{CC} power-on or a reset condition at the $\overline{RST}/\overline{NMI}$ pin in reset mode

Reset Pin Control Register

15	14	13	12	11	10	9	8
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
				SYSRSTRE	**SYSRSTUP**	**SYSNMIES**	**SYSNMI**
r0	r0	r0	r0	r1	r1	r1	rw-0

SYSRSTRE	Indicates resistor present on $\overline{\text{RST}}$ pin
SYSRSTUP	Indicates pullup on $\overline{\text{RST}}$ pin
SYSNMIES	Indicates NMI edge select
SYSNMI	NMI enable on $\overline{\text{RST}}$/$\overline{\text{NMI}}$ pin

Memory Organization

Table 5. Memory Organization

	TYPE	MSP430C091	MSP430C092	MSP430L092	MSP430L092 (EMU)(1)
Primary interrupt vectors	ROM	32 B 0x0FFE0(2) – 0x0FFFF	32 B 0x0FFE0(2) – 0x0FFFF	32 B 0x0FFE0(2) – 0x0FFFF	32 B 0x0FFE0(2) – 0x0FFFF
Secondary interrupt vectors	RAM Lockable			0x01C60 – 0x01C7F	
Application ROM memory	ROM	864 B 0x0FC80 – 0x0FFDF	1888 B 0x0F880 – 0x0FFDF		ROM not available
Boot Code (BC) / Loader Code	ROM (by TI)	128 B (BC) 0x0F800 – 0x0F87F	128 B (BC) 0x0F800 – 0x0F87F	2016 B (Loader) 0x0F800 – 0x0FFDF	Config/loading by tool 0x0F800 – 0x0F87F
RAM memory	RAM	128B 0x02380 – 0x023FF	128B 0x02380 – 0x023FF	128 B 0x02380 – 0x023FF	128 B 0x02380 – 0x023FF
LRAM memory (lockable)	RAM			1792 B 0x01C80 – 0x0237F	1760 B 0xF900 – 0xFFDF
CRAM memory (lockable)	RAM	96 B 0x01C00 – 0x01C5F	96 B 0x01C00 – 0x01C5F	96 B 0x01C00 – 0x01C5F	128 B(3) 0x0F880 – 0x0F8FF
Peripherals	Size	4 kB 0x00000 – 0x00FFF	4 kB 0x00000 – 0x00FFF	4 kB 0x00000 – 0x00FFF	4 kB 0x00000 – 0x00FFF

(1) The MSP430L092 emulates the MSP430C092 device (MSP430C091 emulation via tool and software).
(2) Not the whole interrupt vector range of CSYS is used on MSP430x09x devices (see Table 4).
(3) Resets and interrupt redirections in RAM with alternate interrupt vectors cannot be emulated .

Start-Up Code (SUC)

The MSP430C09x start-up code checks the password and releases control to the application or enables JTAG on password match, enters LPM4, and waits for a debug session. The behavior of the SUC is described in the *MSP430L092 Loader Code User's Guide* (SLAU324).

Loader Code (Loader)

The MSP430L092 loader checks the presence of an external SPI/I2C memory device containing a valid code signature, loads validated code into the application LRAM, and starts the application. The loader program uses P1.2 with an external circuit to pump up the voltage required for SPI memory device readout. For complete description of the features of the loader and its implementation, see the *MSP430L092 Loader Code User's Guide* (SLAU324).

RAM Memory

The RAM memory is split into three ranges for different purposes: application memory, lockable application memory, and calibration memory.

Lockable application memory and calibration memory can be protected against accidental erasure by setting a dedicated lock bit in the special functions register (System Maintenance Register).

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x09x Family User's Guide* (SLAU321).

Digital I/O

There are two I/O ports implemented: P1 (7 I/O lines) and P2 (4 I/O lines).

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt input capability for all ports on P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 and P2) or word-wise in pairs (P1/P2 combo).

Oscillator and System Clock

The clock system in the MSP430x09x family of devices is supported by the Compact Clock System (CCS) module that includes support for an internal 20-kHz current-controlled low-frequency oscillator (LF-OSC), an internal adjustable 1-MHz current-controlled high-frequency oscillator (HF-OSC), and an external clock input from CLKIN; however, a missing CLKIN signal does not trigger an oscillator failsafe mechanism in this family.

The CCS module is designed to meet the requirements of both low system cost and low power consumption. The CCS provides a fast turn-on of the oscillators, less than 1 ms. The CCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the 20-kHz internal LF-OSC, the 1-MHz internal HF-OSC, or CLKIN.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- VLOCLK is an ultra-low-power low-frequency clock that is available as long the device is powered.

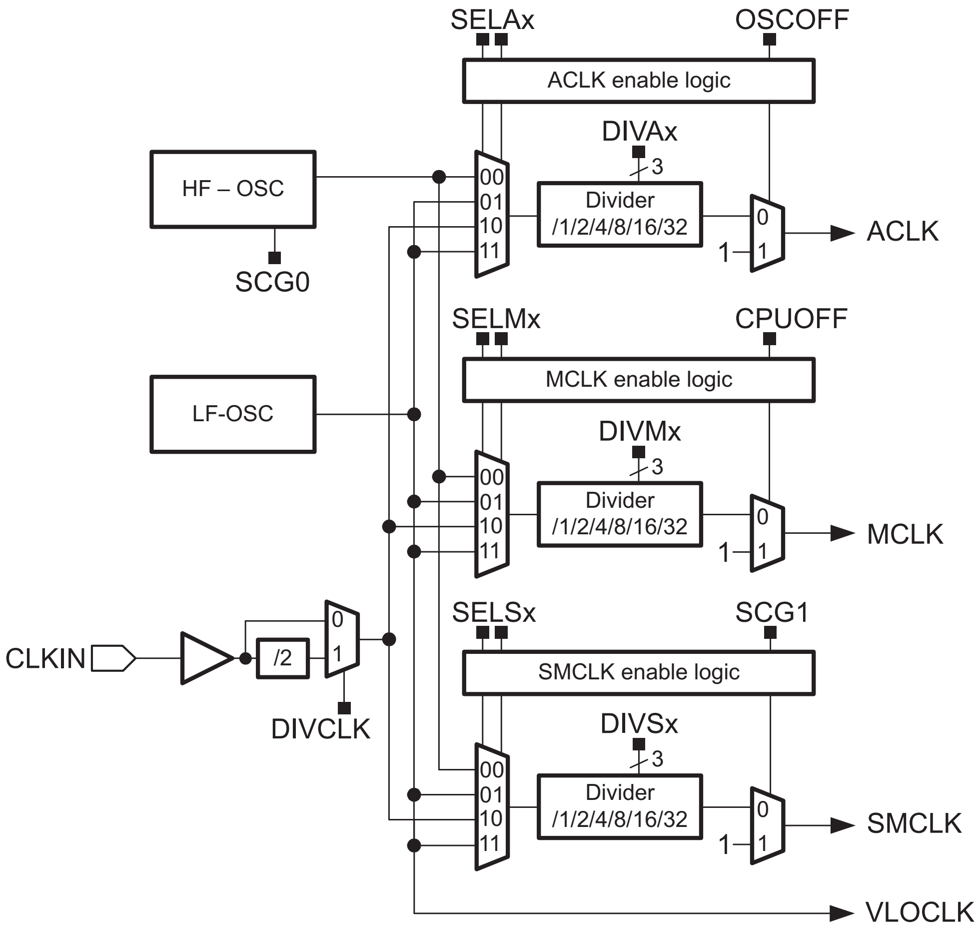


Figure 1. Compact Clock System (CCS) Block Diagram

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Table 6. WDT_A Signal Connections

DEVICE CLOCK SIGNAL	MODULE CLOCK SIGNAL
ACLK	ACLK
SMCLK	SMCLK
LF-OSC-CLK	VLOCLK
LF-OSC-CLK	X-CLK

Compact System Module (C-SYS)

The Compact SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, and configuration management. It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

RST/NMI/SVMOUT System

The reset system of the MSP430x09x family features the functions reset input, reset output, NMI input, SVM output, and SVS input.

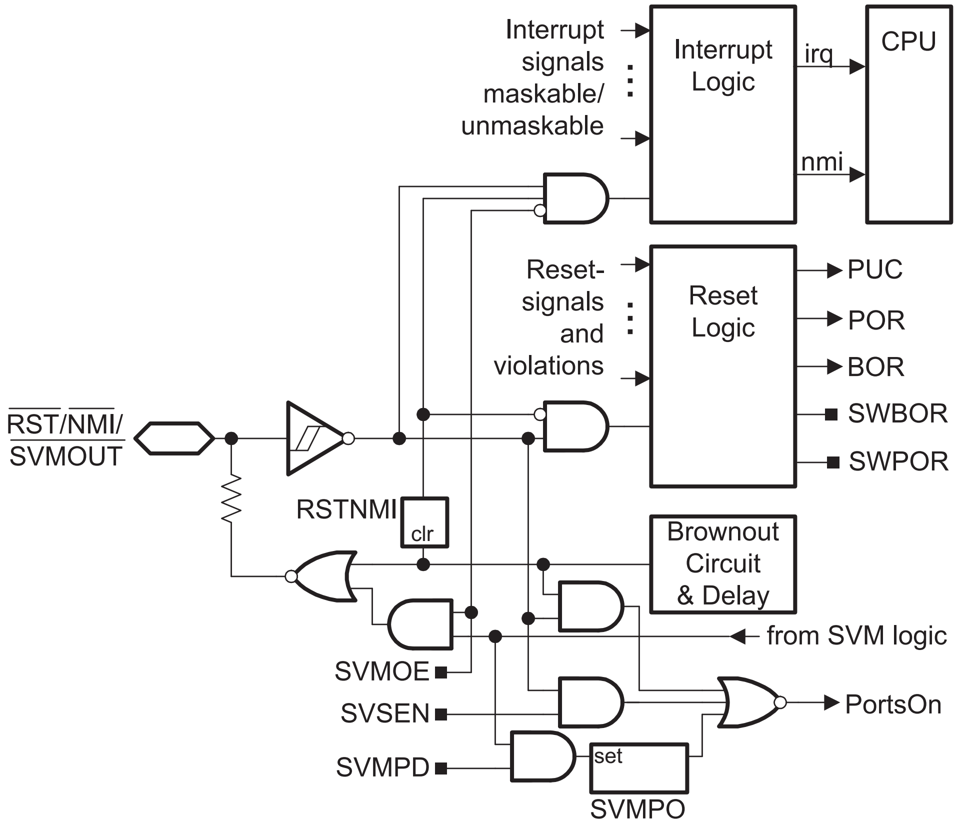


Figure 2. RST/NMI/SVMOUT and PortsOn Logic Block Diagram

Table 7. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT VECTOR	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	SVMBOR (BOR)		04h	
	RST/NMI (BOR)		06h	
	DoBOR (BOR)		08h	
	Security violation (BOR)		0Ah	
	DoPOR(POR)		0Ch	
	WDT timeout (PUC)		0Eh	
	WDT key violation (PUC)		10h	
	CCS key violation		12h	
	PMM key violation		14h	
	Peripheral area fetch (PUC)		16h	
	Reserved		18h-3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMIFG		02h	Highest
	VMAIFG		04h	
	JMBINIFG		06h	
	JMBOUTIFG		08h	
	Reserved		0Ah-3Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	BERR		06h	
	Reserved		08h-3Eh	Lowest
SYSBERRIV, Bus Error	No interrupt pending	0198h	00h	
	Reserved		02h-3Eh	Lowest

Timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 8. Timer0_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
PW						PW
7 – P1.1	TA0CLK	TACLK	Timer	NA	NA	
	ACLK	ACLK				
	SMCLK	SMCLK				
7 – P1.1	TA0CLK	TACLK				
3 – P2.2	CCI0.0	CCI0A	CCR0	TA0	TA0.0	
8 – P1.2	CCI0.0	CCI0B				
	V_{SS}	GND				
	V_{CC}	V_{CC}				
13 – P1.5	TA0.1	CCI1A	CCR1	TA1	TA0.1	2 – P2.1
6 – P1.0	CCI0.1	CCI1B				13 – P1.5
	V_{SS}	GND				
	V_{CC}	V_{CC}				
1 – P2.0	TA0.2	CCI2A	CCR2	TA2	TA0.2	1-4 – P2.0-P2.3
2 – P2.1	TA0.2	CCI2B				6-9 – P1.0-P1.3
	V_{SS}	GND				12-14 – P1.4-P1.6
	V_{CC}	V_{CC}				

Timer1_A3

Timer1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer1_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9. Timer1_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER
PW						PW
12 – P1.4	TA1CLK	TACLK	Timer	NA	NA	
	ACLK	ACLK				
	SMCLK	SMCLK				
12 – P1.4	TA1CLK	TACLK				
4 – P2.3	CCI1.0	CCI0A	CCR0	TA0	TA1.0	
9 – P1.3	CCI1.0	CCI0B				
	V_{SS}	GND				
	V_{CC}	V_{CC}			TA1.1	
14 – P1.6	TA1.1	CCI1A	CCR1	TA1		1 – P2.0
7 – P1.1	CCI1.1	CCI1B				14 – P1.6
	V_{SS}	GND				
	V_{CC}	V_{CC}				
1 – P2.0	TA1.2	CCI2A	CCR2	TA2	TA1.2	1-4 – P2.0-P2.3
2 – P2.1	TA1.2	CCI2B				6-9 – P1.0-P1.3
	V_{SS}	GND				12-14 – P1.4-P1.6
	V_{CC}	V_{CC}				

A-Pool

The analog functions pool (A-Pool) provides a series of functions that can be configured to a digital-to-analog converter (DAC), multichannel analog-to-digital converter (ADC), supply voltage supervisor (SVS), and comparator. Input voltage dividers and an internal reference source allow a wide range of combined analog functions.

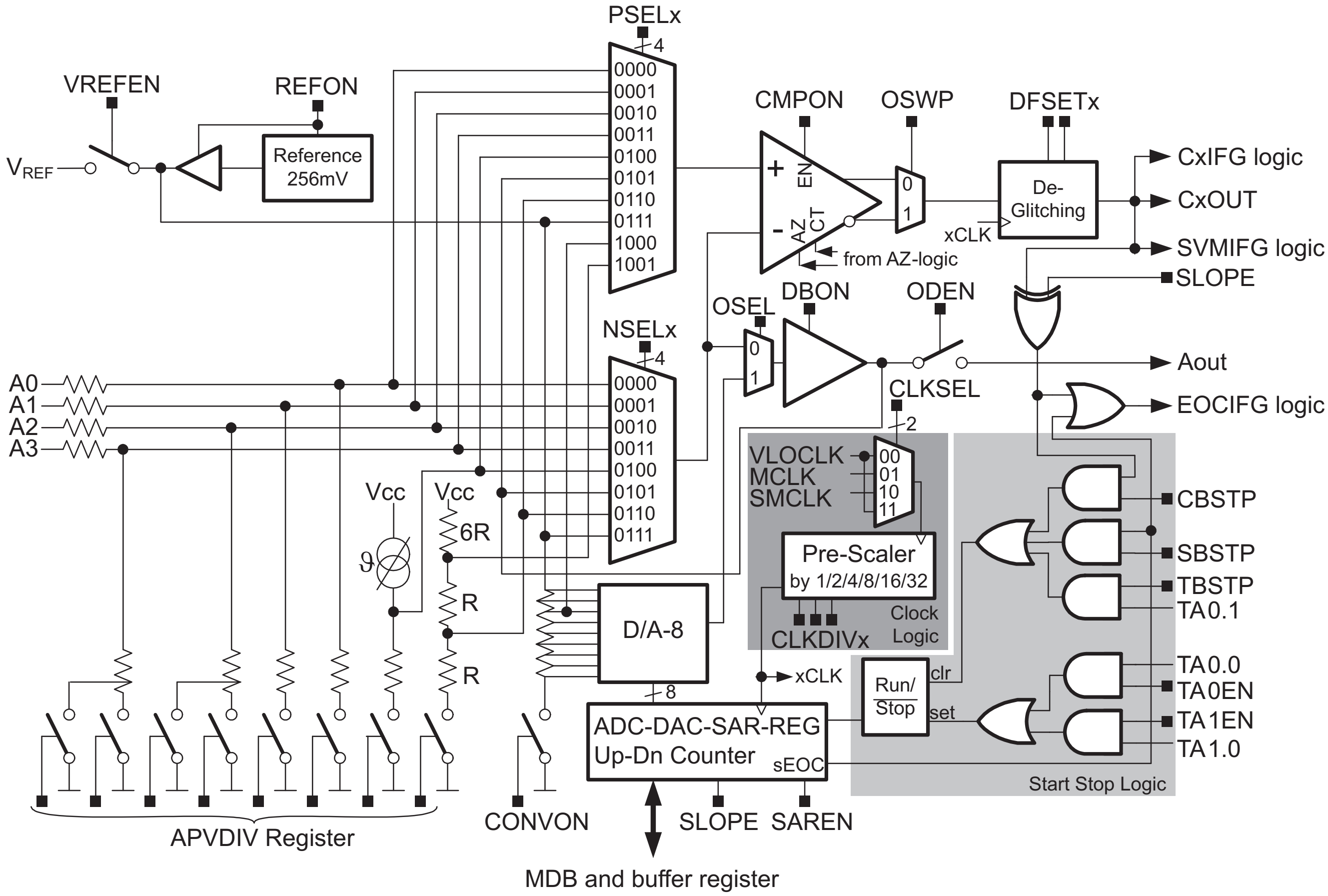


Figure 3. A-Pool Block Diagram

Versatile I/O Port P1, P2

The versatile I/O ports P1 and P2 feature device-dependent reset values. The reset values for the MSP430x09x devices are shown in Table 10.

Table 10. Versatile Port Reset Values

PORT NUMBER	PxOUT	PxDIR	PxREN	PxSEL0	PxSEL1	RESET	PORTS ON	COMMENT
P1.0	0	0	0	0	0	PUC	yes	P1.0, input
P1.1	0	0	0	0	0	PUC	yes	P1.1, input
P1.2	0	0	0	0	0	PUC	yes	P1.2, input
P1.3	0	0	0	0	0	PUC	yes	P1.3, input
P1.4	0	0	0	0	0	PUC	yes	P1.4, input
P1.5	0	0	0	0	0	PUC	yes	P1.5, input
P1.6	0	0	0	0	0	PUC	yes	P1.6, input
P1.7	-	-	-	-	-	-	-	-
P2.0	1	0	1	1	1	BOR	no	JTAG TCK, input, pullup
P2.1	1	0	1	1	1	BOR	no	JTAG TMS, input, pullup
P2.2	1	0	1	1	1	BOR	no	JTAG TDI, input, pullup
P2.3	0	1	0	1	1	BOR	no	JTAG TDO, output, pullup

Peripheral File Map

Table 11. Peripherals

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Timer1_A3	Timer1_A interrupt vector	TA1IV	0380h	2Eh
	Capture/compare register 2	TA1CCR2		16h
	Capture/compare register 1	TA1CCR1		14h
	Capture/compare register 0	TA1CCR0		12h
	Timer1_A register	TA1R		10h
	Capture/compare control 2	TA1CCTL2		06h
	Capture/compare control 1	TA1CCTL1		04h
	Capture/compare control 0	TA1CCTL0		02h
	Timer1_A control	TA1CTL		00h
Timer0_A3	Timer0_A interrupt vector	TA0IV	0340h	2Eh
	Capture/compare register 2	TA0CCR2		16h
	Capture/compare register 1	TA0CCR1		14h
	Capture/compare register 0	TA0CCR0		12h
	Timer1_A register	TA0R		10h
	Capture/compare control 2	TA0CCTL2		06h
	Capture/compare control 1	TA0CCTL1		04h
	Capture/compare control 0	TA0CCTL0		02h
	Timer1_A control	TA0CTL		00h

Table 11. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Port P2	Port P2 interrupt Flag	P2IFG	0200h	1Dh
	Port P2 interrupt enable	P2IE		1Bh
	Port P2 interrupt edge select	P2IES		19h
	Port P2 interrupt vector word	P2IV		1Eh
	Port P2 selection 1	P2SEL1		0Dh
	Port P2 selection 0	P2SEL0		0Bh
	Port P2 pullup/pulldown enable	P2REN		07h
	Port P2 direction	P2DIR		05h
	Port P2 output	P2OUT		03h
	Port P2 input	P2IN		01h
Port P1	Port P1 interrupt Flag	P1IFG	0200h	1Ch
	Port P1 interrupt enable	P1IE		1Ah
	Port P1 interrupt edge select	P1IES		18h
	Port P1 interrupt vector word	P1IV		0Eh
	Port P1 selection 1	P1SEL1		0Ch
	Port P1 selection 0	P1SEL0		0Ah
	Port P1 pullup/pulldown enable	P1REN		06h
	Port P1 direction	P1DIR		04h
	Port P1 output	P1OUT		02h
	Port P1 input	P1IN		00h
A-POOL	Analog pool interrupt vector register	APIV	01A0h	1Eh
	Analog pool interrupt enable register	APIE		1Ch
	Analog pool interrupt flag register	APIFG		1Ah
	Analog pool fractional value buffer	APFRACTB		16h
	Analog pool fractional value register	APFRACT		14h
	Analog pool integer value buffer	APINTB		12h
	Analog pool integer value register	APINT		10h
	Analog pool voltage divider register	APVDIV		06h
	Analog pool operation mode register	APOMR		04h
	Analog pool control register	APCTL		02h
	Analog pool configuration register	APCNF		00h
CSYS	Reset vector generator	SYSRSTIV	0180h	1Eh
	System NMI vector generator	SYSSNIV		1Ch
	User NMI vector generator	SYSUNIV		1Ah
	Bus error vector generator	SYSBERRIV		18h
	System Configuration register	SYSCNF		10h
	JTAG mailbox output register #1	SYSJMBO1		0Eh
	JTAG mailbox output register #0	SYSJMBO0		0Ch
	JTAG mailbox input register #1	SYSJMBI1		0Ah
	JTAG mailbox input register #0	SYSJMBI0		08h
	JTAG mailbox control register	SYSJMBC		06h
	System control register	SYSCTL		00h

Table 11. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
CCS	CCS control 15 register	CCSCTL15	0160h	1Eh
	CCS control 8 register	CCSCTL8		10h
	CCS control 7 register	CCSCTL7		0Eh
	CCS control 5 register	CCSCTL5		0Ah
	CCS control 4 register	CCSCTL4		08h
	CCS control 2 register	CCSCTL2		04h
	CCS control 1 register	CCSCTL1		02h
	CCS control 0 register	CCSCTL0		00h
WDT_A	Watchdog timer control	WDTCTL	0150h	0Ch
PMM	PMM control 0	PMMCTL0	0120h	00h
ET-Wrapper	ET Key and select	ETKEYSEL	0110h	00h
Special Functions	SFR Reset pin control register	SFRRPCR	0100h	04h
	SFR interrupt flag register	SFRIFG1		02h
	SFR interrupt enable register	SFRIE1		00h

Absolute Maximum Ratings[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Voltage applied at V_{CC} referenced to V_{SS} (V_{AMR})	–0.3 V to 1.90 V
Voltage applied to any pin (references to V_{SS})	–0.3 V to V_{CC} + 0.3 V
	–0.3 V to 1.90 V
Diode current at any device pin[2]	±2.5 mA
Current derating factor when I/O ports are switched in parallel electrically and logically[3]	0.9
Storage temperature range[4]	–55°C to 150°C
ESD tolerance, Human-Body Model (HBM)	2000 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.
(3) The diode current increases to ±4.5 mA when two pins are connected, ± 6.75 mA for three pins.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution		0.9		1.65	V
V_{SS}	Supply voltage (GND reference)			0		V
T_A	Operating free-air temperature		0		50	°C
C_{VCC}	Capacitor on V_{CC}			470		nF
f_{SYSTEM} [1][2]	System operating frequency	V_{CC} > 0.9 V, t_{LOW} ≥ 450 ns, t_{HIGH} ≥ 450 ns		1		MHz
		V_{CC} > 1.5 V, t_{LOW} ≥ 113 ns, t_{HIGH} ≥ 113 ns		4		MHz

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.

Active Mode Supply Current (Into V_{CC}) Excluding External Current(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	0°C		59	68	µA
		1.3 V			72	84	
		1.65 V			86	101	
	f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	30°C		59	68	
		1.3 V			72	84	
		1.65 V			86	101	
	f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	50°C		60	70	
		1.3 V			74	87	
		1.65 V			88	105	
$I_{AM,125kHz}$	f_{MCLK} = f_{SMCLK} = 125 kHz, f_{ACLK} = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	0°C		31	35	µA
		1.3 V			33	38	
		1.65 V			37	42	
	f_{MCLK} = f_{SMCLK} = 125 kHz, f_{ACLK} = 20 kHz Program executes in RAM CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	30°C		31	35	
		1.3 V			33	38	
		1.65 V			37	42	
	f_{MCLK} = f_{SMCLK} = 125 kHz, f_{ACLK} = 20 kHz, Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	50°C		32	37	
		1.3 V			35	41	
		1.65 V			40	48	
I_{AM}/MHz	f_{MCLK} = f_{SMCLK} : 1 to 5 MHz, f_{ACLK} = 20 kHz Program executes in RAM, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	1.3 V	30°C		45		µA/MHz

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Characterized with program executing typical data processing "Type2".

Low-Power Mode Supply Current (Into V_{CC}) Excluding External Current(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
I_{LPM0}	f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 20 kHz CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	0.9 V	0°C		6.6	8	µA
		1.3 V			7.6	9	
		1.65 V			8.6	11	
		0.9 V	30°C		7	9	
		1.3 V			8.3	11	
		1.65 V			9.5	12	
		0.9 V	50°C		8.9	12	
		1.3 V			11	14	
		1.65 V			12	17	
I_{LPM1}	f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 0, OSCOFF = 0	0.9 V	0°C		6.6	8	µA
		1.3 V			7.6	9	
		1.65 V			8.6	11	
		0.9 V	30°C		7	9	
		1.3 V			8.3	11	
		1.65 V			9,5	12	
		0.9 V	50°C		8.9	12	
		1.3 V			11	14	
		1.65 V			12	17	

(1) Current for WDT clocked by ACLK included.
(2) Current for Brownout included.

Low-Power Mode Supply Current (Into V_{CC}) Excluding External Current[(1)(2)] (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
$I_{LPM2,1MHz}$	f_{MCLK} = f_{SMCLK} = 1MHz, f_{ACLK} = 1MHz CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	0.9 V	0°C to 30°C		26	30	µA
		1.3 V			28	32	
		1.65 V			29	33	
		0.9 V	50°C		28	32	
		1.3 V			30	35	
		1.65 V			32	38	
$I_{LPM2,20kHz}$	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 kHz CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	0.9 V	0°C		6.6	8	µA
		1.3 V			7.6	10	
		1.65 V			8.6	11	
		0.9 V	30°C		7	10	
		1.3 V			8.3	12	
		1.65 V			9.5	13	
		0.9 V	50°C		8.9	13	
		1.3 V			11	15	
		1.65 V			12	17	
I_{LPM3}	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	0.9 V	0°C		6.6	8	µA
		1.3 V			7.6	9	
		1.65 V			8.6	11	
		0.9 V	30°C		7.1	9	
		1.3 V			8.3	11	
		1.65 V			9.5	12	
		0.9 V	50°C		8.9	12	
		1.3 V			11	14	
		1.65 V			12	17	
I_{LPM4}	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 20 kHz CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	0.9 V	0°C		3.2	4.7	µA
		1.3 V			5.1	6.3	
		1.65 V			6.5	8	
		0.9 V	30°C		4	5.7	
		1.3 V			6	7.9	
		1.65 V			7.8	10	
		0.9 V	50°C		6	8.9	
		1.3 V			8.6	12	
		1.65 V			11	16	

Ports P1 and P2, $\overline{RST}$/$\overline{NMI}$/SVMOUT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	V_{CC} = 0.9 V, I_{OH} = –1 mA (1) for ports P1, P2	V_{CC} – 0.25			V
	V_{CC} = 1.65 V, I_{OH} = –1 mA (1) for ports P1, P2	V_{CC} – 0.15			
	V_{CC} = 0.9 V, I_{OH} = –300 µA (1) for ports P1, P2	V_{CC} – 0.15			
V_{OL}	V_{CC} = 0.9 V, I_{OL} = 2.5 mA (2) for ports P1, P2			0.2	V
	V_{CC} = 1.65 V, I_{OL} = 2.5 mA (2) for ports P1, P2			0.15	
	V_{CC} = 0.9 V, I_{OL} = 300 µA (2) for ports P1, P2			0.07	
V_{IL}	V_{CC} = 1.65 V			0.3 × V_{CC}	V
	V_{CC} = 0.9 V			0.25 × V_{CC}	
V_{IH}	V_{CC} = 1.65 V	0.7 × V_{CC}			V
	V_{CC} = 0.9 V	0.75 × V_{CC}			
V_{HYS}	Intrinsic hysteresis		150		mV
Δt/Δv	V_{CC} = 0.9 V, C_L = 15 pF || R_L = 750 Ω to V_{SS} on V_{OH} for ports P1, P2			75	ns/V
	V_{CC} = 0.9 V, C_L = 15 pF || R_L = 320 Ω to V_{CC} on V_{OL} for ports P1, P2			75	
	V_{CC} = 1.65 V, C_L = 25 pF || R_L = 1600 Ω to V_{SS} on V_{OH} for ports P1, P2			75	
	V_{CC} = 1.65 V, C_L = 25 pF || R_L = 600 Ω to V_{SS} on V_{OL} for ports P1, P2			75	
I_{OH}	V_{CC} = 0.9 V to 1.65 V for ports P1, P2	–1			mA
I_{OL}	V_{CC} = 0.9 V to 1.65 V for ports P1, P2	2.5			mA
I_{LKG}	V_{CC} = 0.9 V to 1.65 V (at 50°C)			±100	nA
t_{INT}	P0.x, V_{CC} = 0.9 V to 1.65 V		200		ns
R_{PULL}	For pullup: VIN = V_{SS}, For pulldown: VIN = V_{CC} for ports P1, P2	30	35	40	kΩ
R_{RST}	Pullup on $\overline{RST}$/$\overline{NMI}$/SVMOUT	30	35	40	kΩ
R_{EXT}	External pullup resistor on $\overline{RST}$ terminal (optional)	680			kΩ
C_I	V_{IN} = V_{SS} or V_{CC}		7		pF

(1) The maximum total current I_{OH}, for all outputs combined should not exceed 5 mA to hold the maximum voltage drop specified.
(2) The maximum total current I_{OL}, for all outputs combined should not exceed 15 mA to hold the maximum voltage drop specified.

Typical Characteristics – Outputs

TYPICAL LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

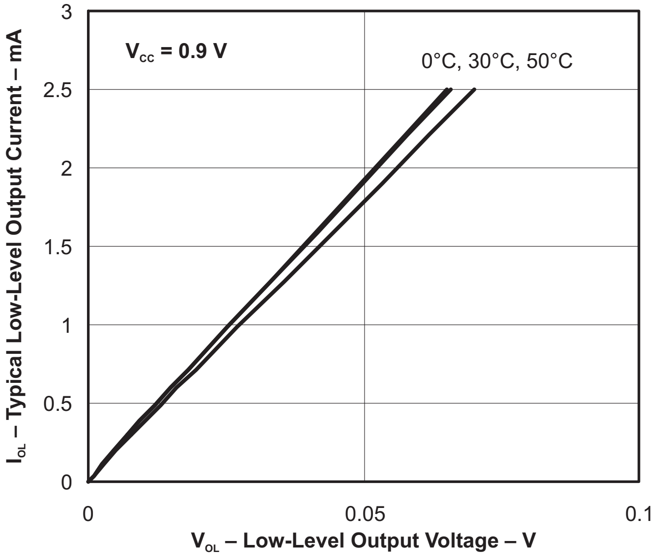


Figure 4.

TYPICAL HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

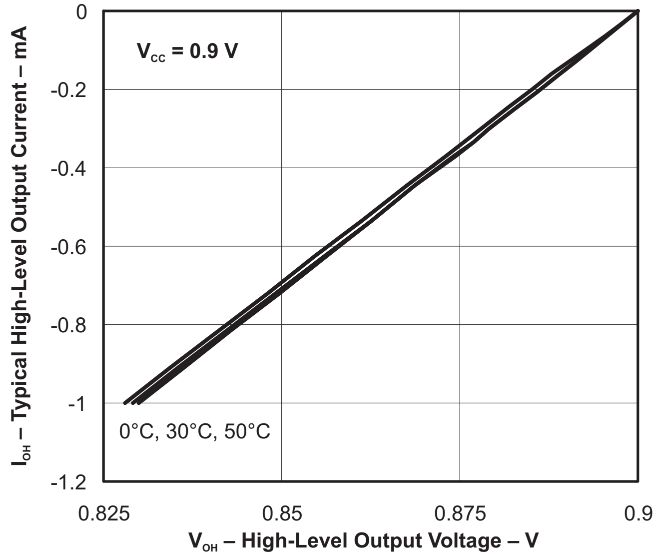


Figure 5.

TYPICAL LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

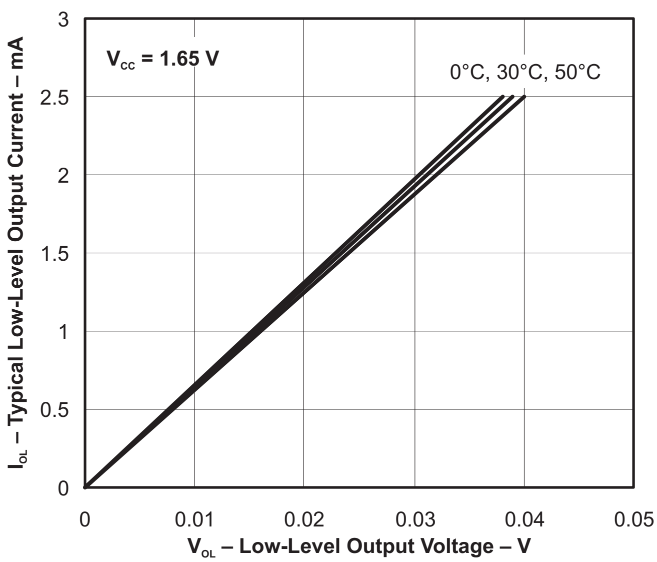


Figure 6.

TYPICAL HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

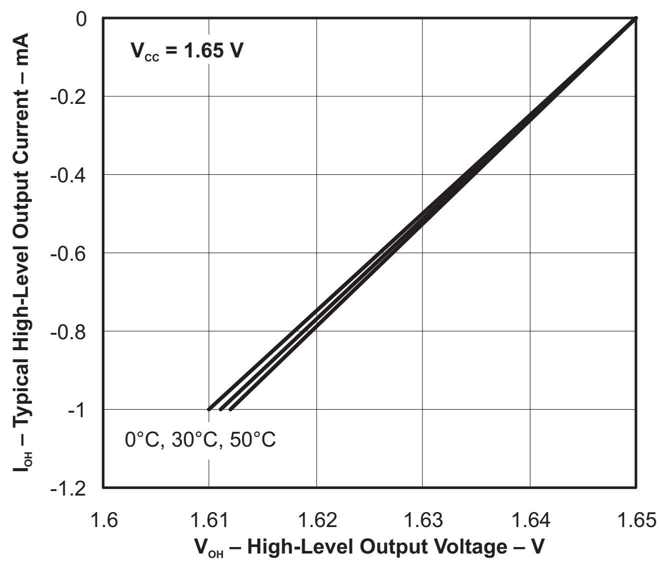


Figure 7.

Typical Characteristics – Outputs (continued)

TYPICAL LOW-LEVEL OUTPUT VOLTAGE vs LARGE SIGNAL OUTPUT CURRENT

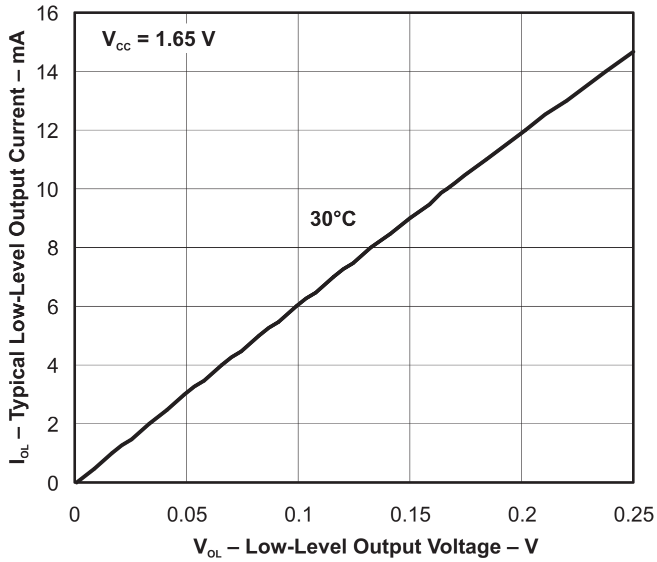


Figure 8.

TYPICAL HIGH-LEVEL OUTPUT VOLTAGE vs LARGE SIGNAL OUTPUT CURRENT

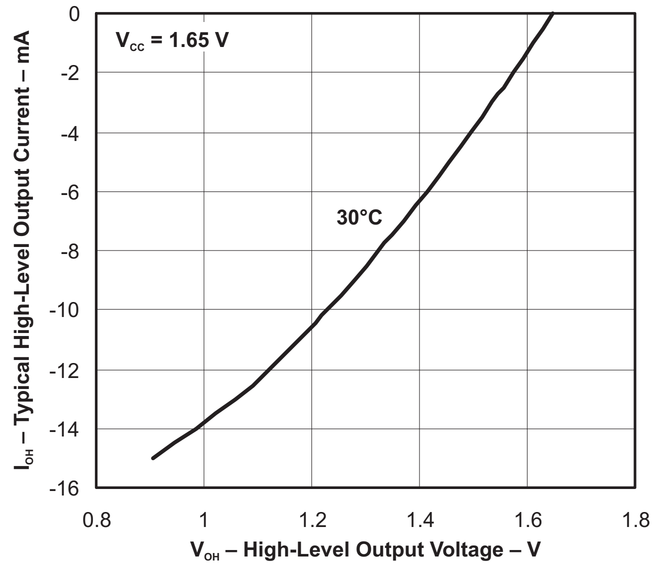


Figure 9.

TYPICAL LOW-LEVEL INPUT VOLTAGE vs SUPPLY VOLTAGE

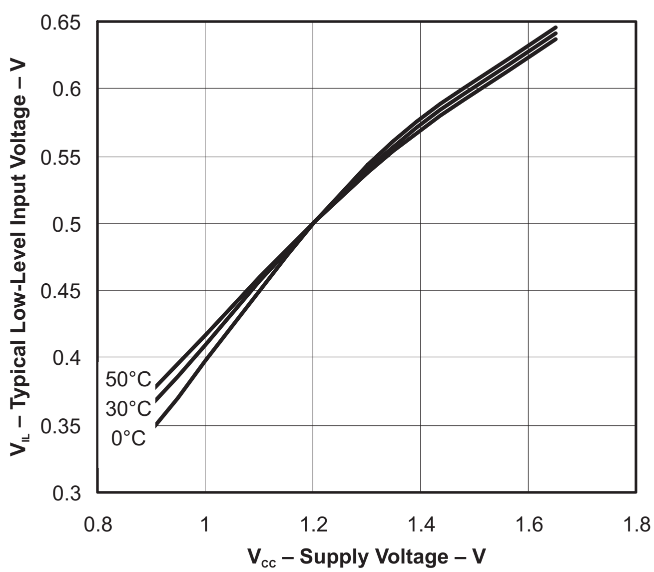


Figure 10.

TYPICAL LOW-LEVEL INPUT VOLTAGE vs SUPPLY VOLTAGE

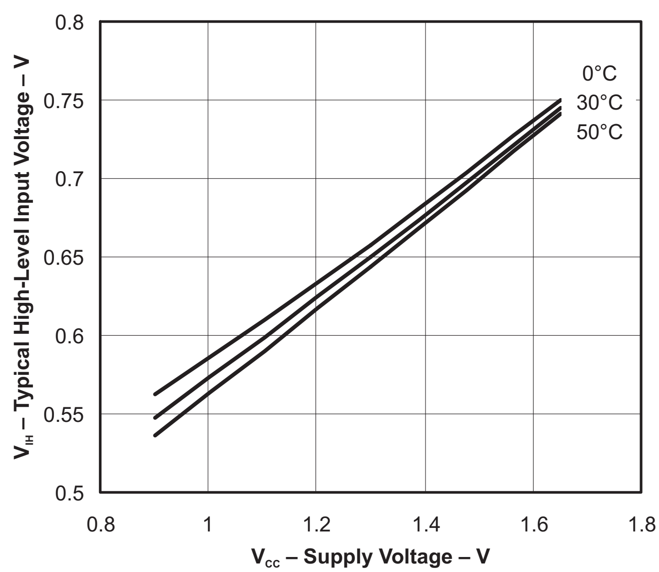


Figure 11.

High-Frequency Oscillator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{HFOSC}	V_{CC} = 0.9 V to 1.65 V (minimum trim range via register)	0.75	1	1.25	MHz
f_{HFOSC}	V_{CC} = 0.9 V to 1.65 V (trimmed at 30°C)	0.92	1	1.08	MHz
Duty cycle	V_{CC} = 0.9 V to 1.65 V	45	50	55	%
t_{START}	V_{CC} = 0.9 V to 1.65 V			20	µs
$\Delta f_{HFOSC}/DT$	V_{CC} = 0.9 V to 1.65 V, f_{HFOSC} = 1 MHz		±0.07	±0.15	%/°C
$\Delta f_{HFOSC}/\Delta V_{CC}$	V_{CC} = 1.0 V to 1.65 V, f_{HFOSC} = 1 MHz			±1	%/V
$\Delta f_{HFOSC}/\Delta V_{CC}$	V_{CC} = 0.90 V to 1.0 V, f_{HFOSC} = 1 MHz		±1	±2.5	%/V
Δf_{HFOSC}/CALSTEP (1)	V_{CC} = 0.9 V to 1.65 V, f_{HFOSC} = 1 MHz, ±64 calibration steps	0.1	1	4	%/ Step
I_{OSC}	V_{CC} = 0.9 V to 1.65 V, f_{HFOSC} = 1 MHz		22		µA

(1) Normalized to typical frequency

Typical Characteristics – High-Frequency Oscillator

FREQUENCY vs TRIM SETTING

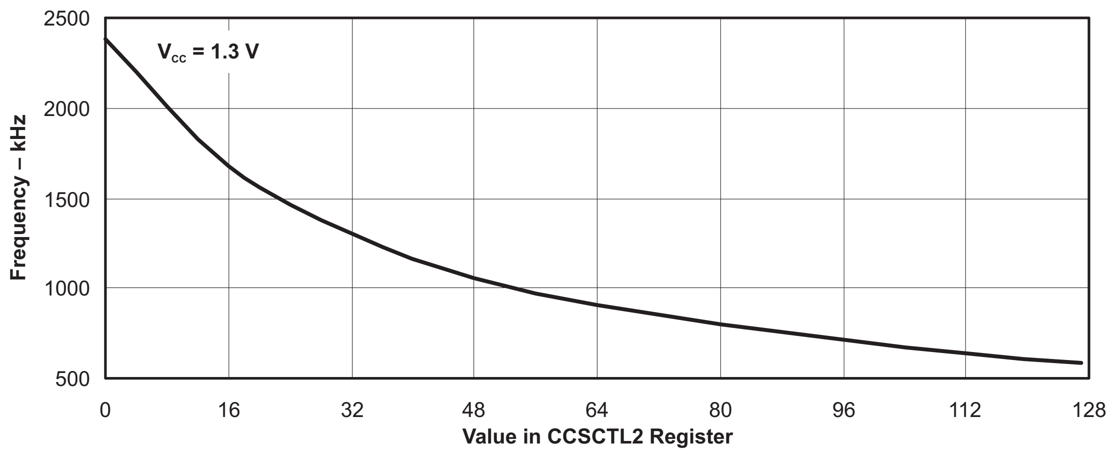


Figure 12.

FREQUENCY vs TEMPERATURE

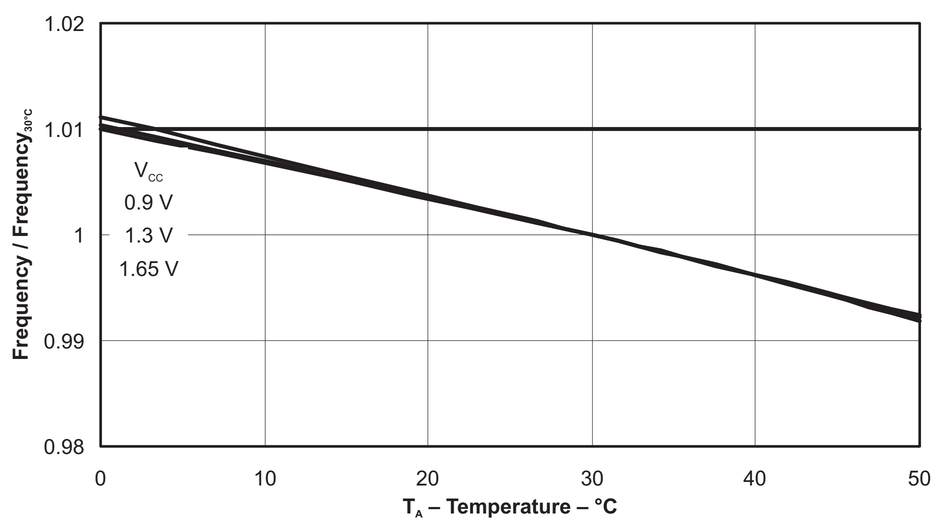


Figure 13.

Low-Frequency Oscillator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	V_{CC} = 0.9 V to 1.65 V	6	20	45	kHz
Duty cycle	V_{CC} = 0.9 V to 1.65 V	45	50	55	%
t_{START}	V_{CC} = 0.9 V to 1.65 V			500	µs
I_{OSC}	V_{CC} = 0.9 V to 1.65 V, f_{LFOSC} = 20 kHz		0.6		µA

Typical Characteristics – Low-Frequency Oscillator

FREQUENCY vs TEMPERATURE

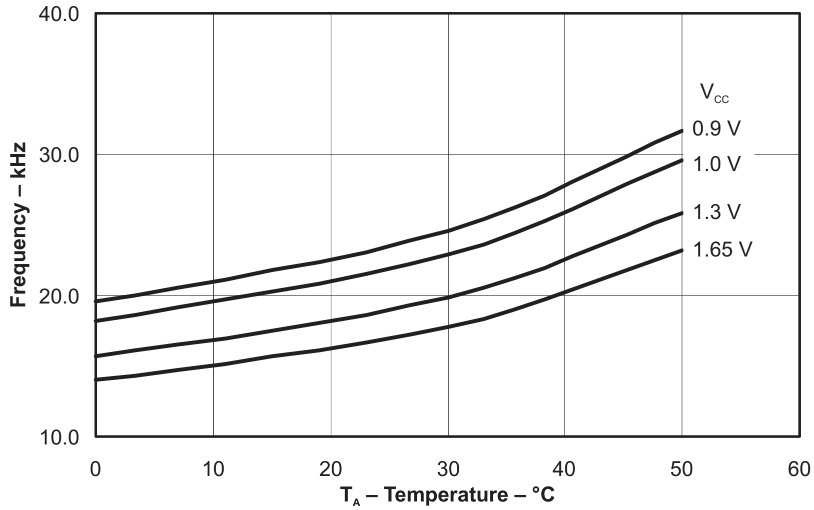


Figure 14.

Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR(Start)}$		490			mV
$V_{(BOR\_IT+)}$	V_{CC} rising, $\Delta V_{CC}/\Delta t$ < 3 V/s	1095		1150	mV
$V_{(BOR\_IT-)}$	V_{CC} falling, $\Delta V_{CC}/\Delta t$ < 3 V/s	860		900	mV
$V_{hys(BOR)}$			200		mV
V_{MARGIN}	$V_{MARGIN} = V_{(BOR-IT-)} - V_{CRIT}$, ($V_{CRIT}$ < 820 mV)(1)	40			mV
$t_{d(BOR)}$				3000(2)	µs

(1) V_{CRIT} is a temperature depending voltage where the single components of the device become unreliable (the 'L092 provides a safety margin to ensure overall device function).
(2) Strongly depends on voltage ramp in system (actually a maximum typical value).

A-POOL, External Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{CC} = 0.9 V to 1.65 V, ADC / DAC operational	100		275	mV
	V_{CC} = 0.9 V to 1.65 V, ADC / DAC not operational	0		V_{CC}	V
$I_{REF(Input)}$	V_{CC} = 0.9 V to 1.65 V, load to external sinks		3		µA
C_{REF}	REFON = 0	20		50	pF

A-POOL, Built-In Reference Source

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{CC} = 0.9 V to 1.65 V (±1.5%, overall 3%)		256		mV
I_{REF}	V_{CC} = 0.9 V to 1.65 V		10		µA
C_{REF}	REFON = 1	20		50	pF
T_{REF}	V_{CC} = 0.9 V to 1.65 V ($\Delta V/\Delta T \times V_{REF}$ referenced to 25°C)		±250		ppm/°C
t_{SETTLE}	V_{CC} = 0.9 V to 1.65 V, REFON = 1, C_{REF} = C_{REF}(max) (1)		900 (1)		µs
$I_{REF(Output)}$	V_{CC} = 0.9 V to 1.65 V, REFON = 1, C_{REF} = C_{REF}(max)		2		µA

(1) As the actual on reference enable signal is synchronized with the LF oscillator.

Typical Characteristics – A-POOL Built-In Reference Source

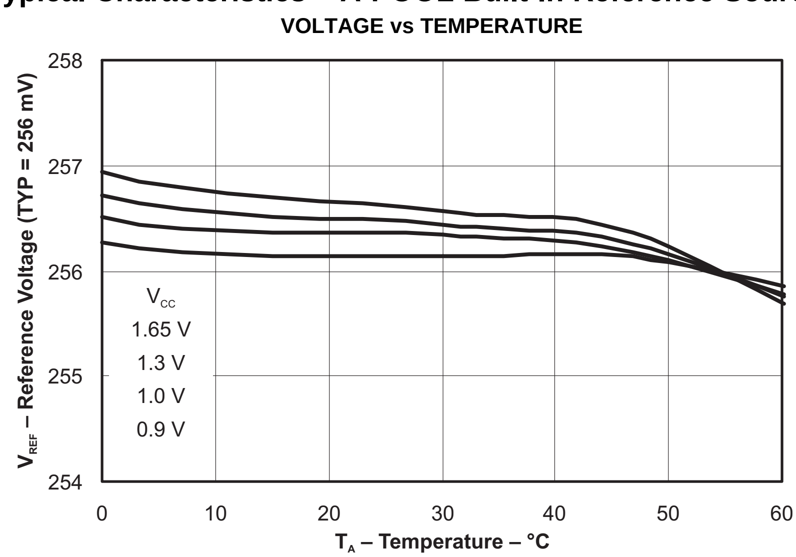


Figure 15.

A-POOL, Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SENSOR}	V_{CC} = 0.9 V to 1.65 V		2		µA
TC_{SENSOR}	V_{CC} = 0.9 V to 1.65 V, T_A = 0°C to 50°C (ΔV/ΔT referenced to 30°C)		464		µV/°C
$V_{OFFSET25}$	V_{CC} = 0.9 V to 1.65 V at T_A = 30°C		179		mV
t_{SETTLE}	V_{CC} = 0.9 V to 1.65 V (before start of conversion)			15	µs
V_{SENSOR} (1)	V_{CC} = 0.9 V to 1.65 V, T_A = 0°C to 50°C		179		mV

(1) This formula can be used to calculate the temperature sensor output voltage: $V_{SENSOR} = V_{OFFSET25} + TC_{SENSOR} \times (T_A - 30°C)$.

A-POOL, Input Voltage Dividers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔRx/Rx	Any Rx in dividers		±1.5		%
	Any Rx across switches and internal supply voltage divider (by 4, by 8)		±2		
RIN	On A0/A1 , VA0/VA1 = 0.5V, ADIV0/ADIV1 = 1 (500-mV range)	120	200	300	kΩ
	On A2/A3 , VA2/VA3 = 0.5V, ADIV2/ADIV4 = 1 (1-V range)	80	133	190	
	On A2/A3 , VA2/VA3 = 0.5V, ADIV2+ADIV3/ADIV4+ADIV5 = 1 (2-V range)	70	114	150	
$ΔI_{VCC}$	ADIV7 = 1 (supply voltage divider on)		2		µA

A-POOL, DAC-8

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	V_{CC} = 0.9 V to 1.65 V		256		mV
t_{SETTLE}	On ±1 LSB steps (6τ), V_{CC} = 0.9 V to 1.65 V, external V_{REF}		2		µs
	Between all codes > 20 on AOUT (6τ), V_{CC} = 0.9 V to 1.65 V, external V_{REF}		14		
EI	V_{CC} = 0.9 V to 1.65 V, external V_{REF}, add ±7 mV for V_{OUT} offset(1) for codes > 7			±3	LSB
ED	V_{CC} = 0.9 V to 1.65 V, external VREF, add ±7 mV for V_{OUT} offset(1) for codes > 7			±1	LSB

(1) This offset can be compensated using software.

A-POOL, Comparator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	V_{CC} = 0.9 V to 1.65 V	0		275	mV
t_{pd}	Overdrive = 20 mV			0.5	µs
	Overdrive = 5 mV			0.5	
	Overdrive = 1 mV			1	

A-POOL, AOUT Terminal

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\mid I_{LOAD} \mid$	V_{CC} = 0.9 V to 1.65 V, C_{LOAD} = 25 pF	V_{OUT} > 50 mV (accuracy ±1% of V_{OUT})	5			µA
		V_{OUT} > 20 mV (accuracy ±1% of V_{OUT})	2			
t_{SETTLE}	V_{CC} = 0.9 V to 1.65 V, C_{LOAD} = 25 pF, ± 1% (6τ) (for AOUT 20 to 256 mV)				4	µs

A-POOL, ADC-8 Counter

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CNT}	V_{CC} = 0.9 V to 1.65 V			1	MHz
t_{CONV}	Full conversion (all codes), f_{CNT} = 1 MHz		256		µs

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OP}	Operating temperature 0°C to 70°C, f_{CPU} = 1MHz	900			mV
V_{RET}	Operating temperature 0°C to 70°C (tracks BOL level)	700			mV

PORT SCHEMATICS

Port P1, P1.0 Input/Output

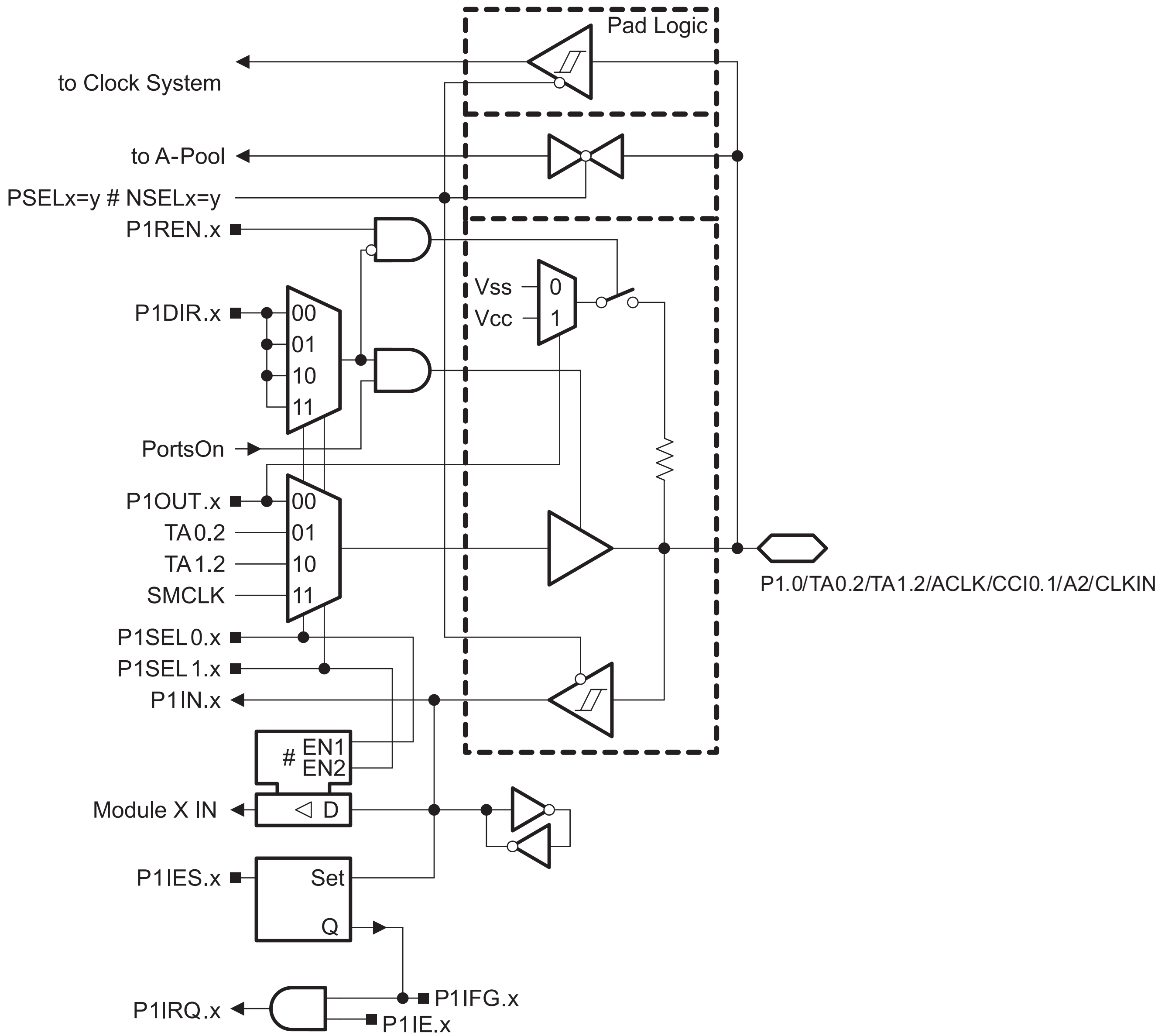


Table 12. Port P1 (P1.0) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx
P1.0/TA0.2/TA1.2/ACLK/CCI0.1/A2/CLKIN	0	P1.0 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		ACLK	1	1	1	0
		Timer A0, CCI1B	0	≠0	≠0	X
		A2	X	X	X	2
		CLKIN (via Bypass)	X	X	X	X

(1) X = Don't care

Port P1, P1.1 and P1.4 Input/Output

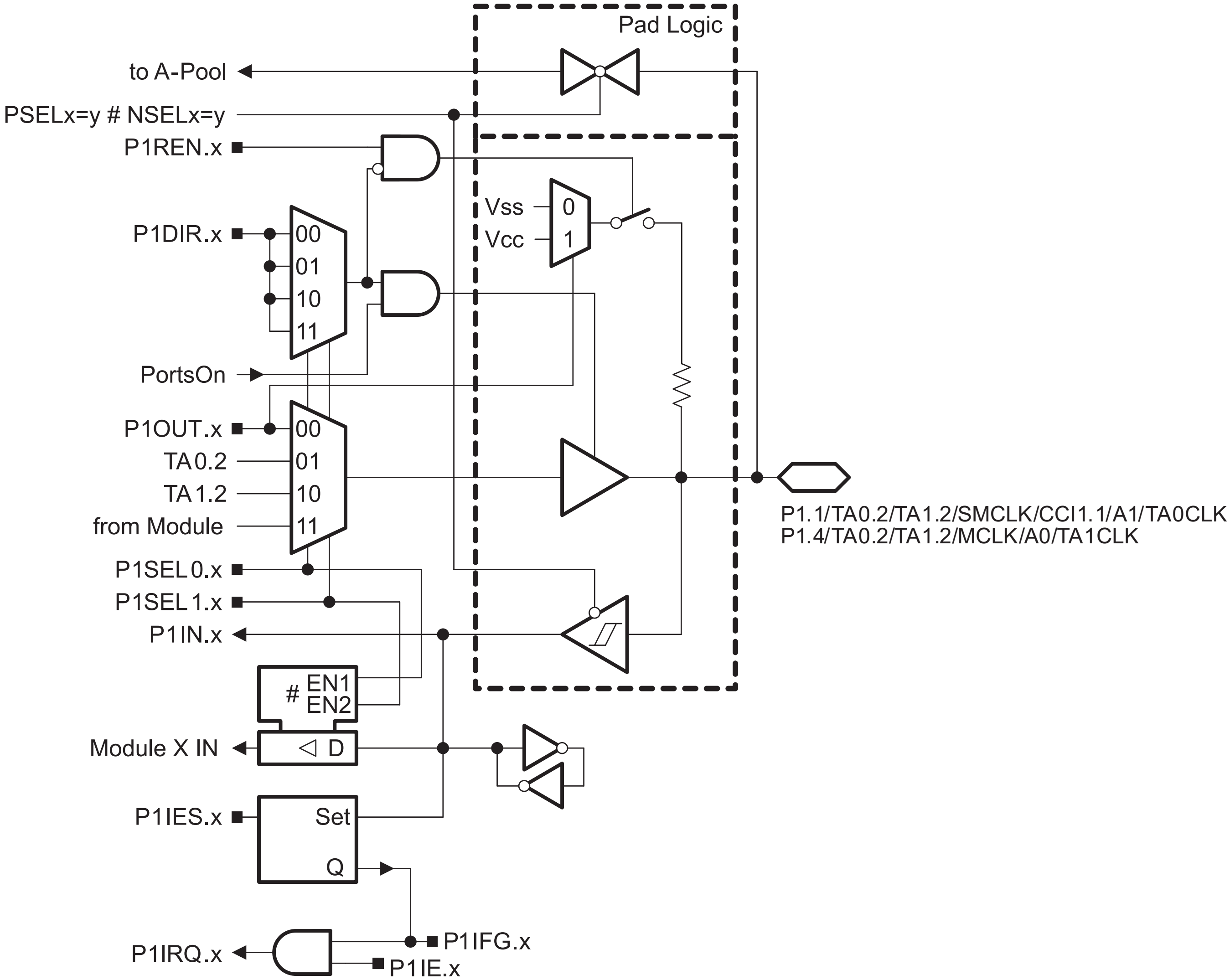


Table 13. Port P1 (P1.1, P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx
P1.1/TA0.2/TA1.2/SMCLK/CCI1.1/A1/TA0CLK	1	P1.1 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		SMCLK	1	1	1	0
		A1	X	X	X	1
		TimerA0 CLK	X	≠0	≠0	X
		Timer A1, CCI1B	0	≠0	≠0	X
P1.4/TA0.2/TA1.2/MCLK/A0/TA1CLK	4	P1.4 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		MCLK	1	1	1	0
		A0	X	X	X	0
		TimerA1 CLK	0	≠0	≠0	X

(1) X = Don't care

Port P1, P1.2 and P1.3 Input/Output

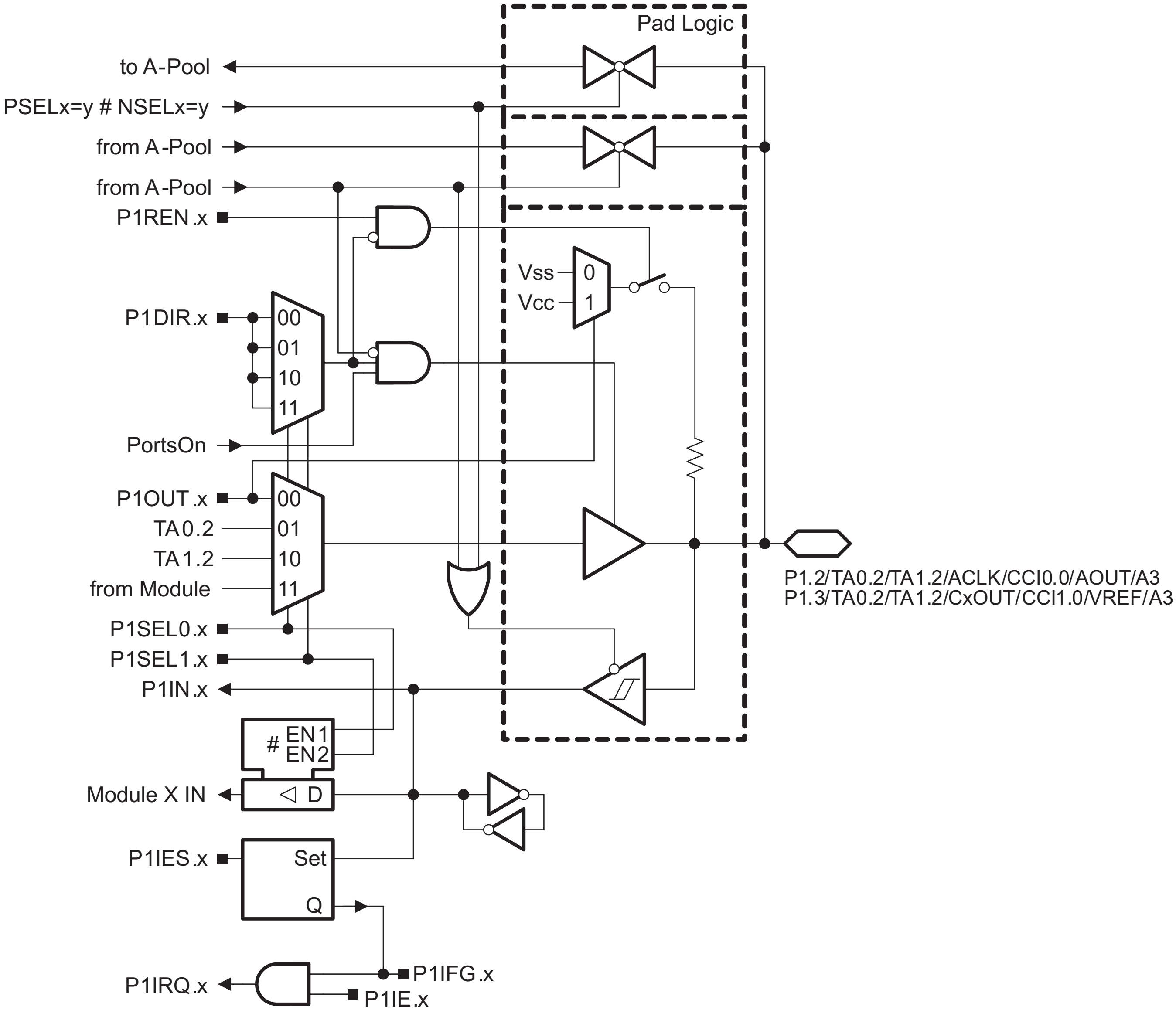


Table 14. Port P1 (P1.2, P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)				
			P1DIR.x	P1SEL1.x	P1SEL0.x	RSELx/ASELx	Analog Out
P1.2/TA0.2/TA1.2/ACLK/CCI0.0/AOUT/A3	2	P1.2 (I/O)	I:0, O:1	0	0	0	0
		Timer_A0.2	1	0	1	0	0
		Timer_A1.2	1	1	0	0	0
		ACLK	1	1	1	0	0
		Timer A0, CCI0B	0	≠0	≠0	X	X
		A3	X	X	X	3	X
		AOUT (2)	X	X	X	X	1
P1.3/TA0.2/TA1.2/CxOUT/CCI1.0//VREF/A3	3	P1.3 (I/O)	I:0, O:1	0	0	0	0
		Timer_A0.2	1	0	1	0	0
		Timer_A1.2	1	1	0	0	0
		CxOUT	1	1	1	0	0
		Timer A1, CCI0B	0	≠0	≠0	X	X
		A3	X	X	X	3	X
		VREF (2)	X	X	X	X	1

(1) X = Don't care
(2) An analog output enable overrides the digital output control.

Port P1, P1.5 and P1.6 Input/Output

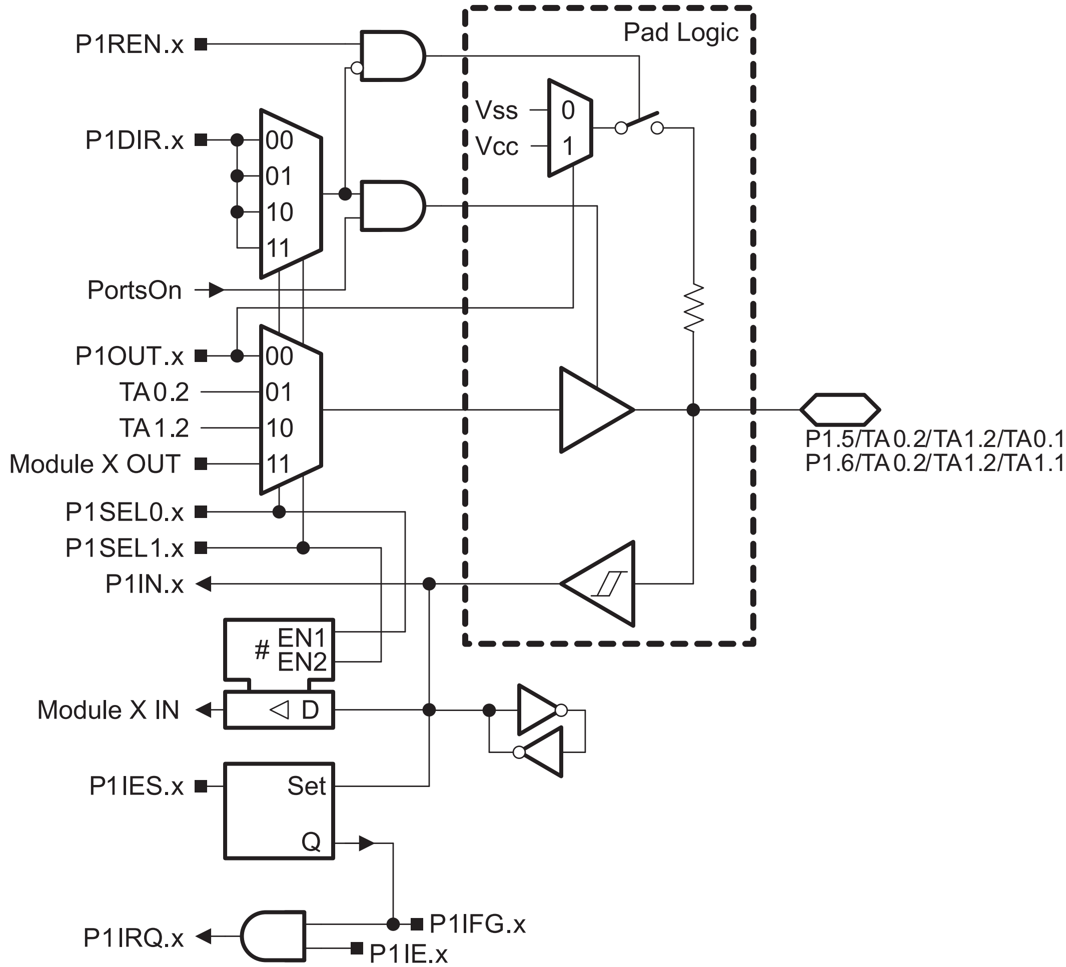


Table 15. Port P1 (P1.5, P1.6) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.5/TA0.2/TA1.2/TA0.1	5	P1.5 (I/O)	I:0, O:1	0	0
		Timer_A0.2	1	0	1
		Timer_A1.2	1	1	0
		Timer A0.1	1	1	1
		Timer_A0.CCI1A	0	≠0	≠0
P1.6/TA0.2/TA1.2/TA1.1	6	P1.6 (I/O)	I:0, O:1	0	0
		Timer_A0.2	1	0	1
		Timer_A1.2	1	1	0
		Timer A1.1	1	1	1
		Timer_A1.CCI1A	0	≠0	≠0

(1) X = Don't care

Port P2, P2.0 to P2.2, Input/Output

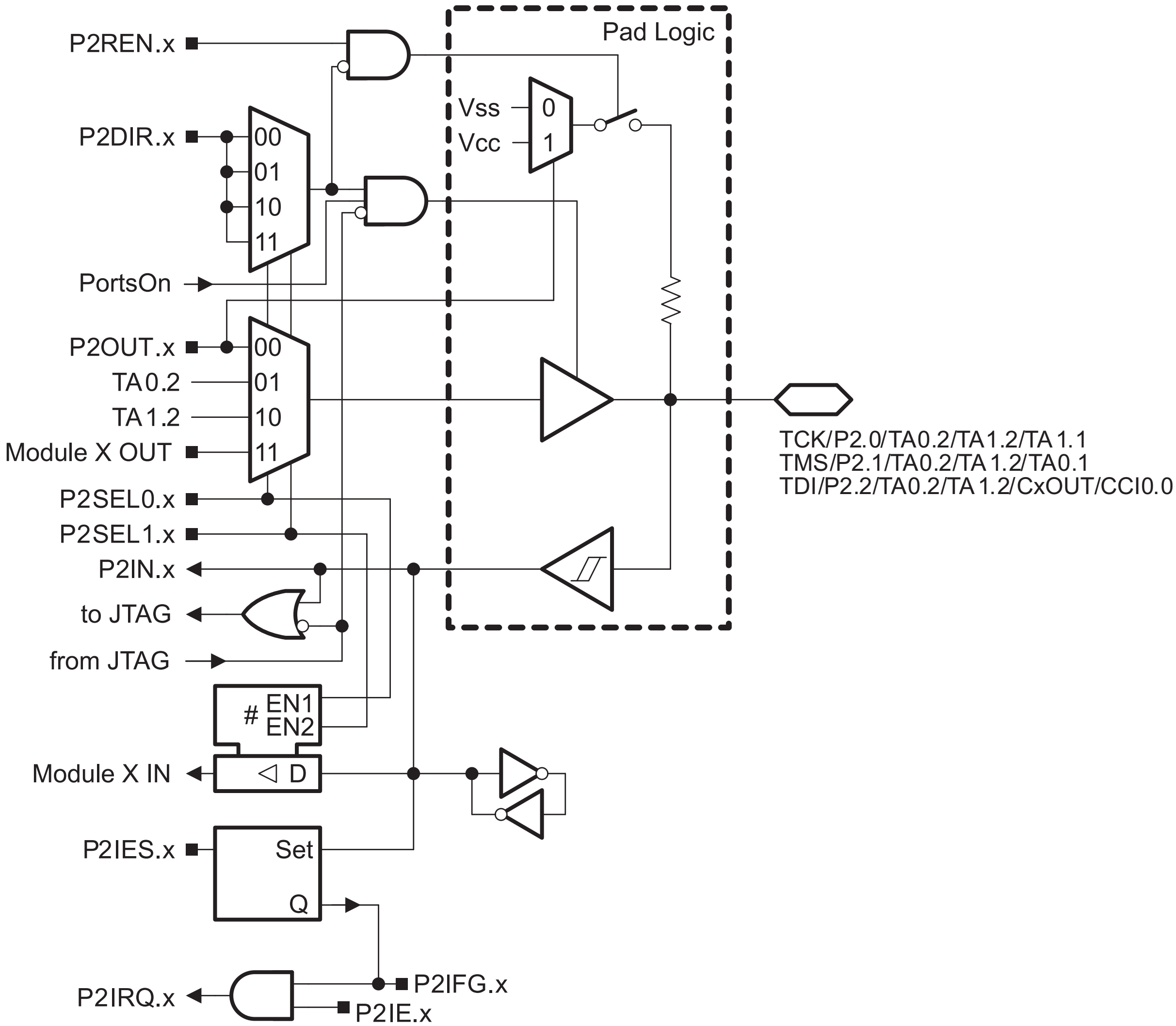


Table 16. Port P2 (P2.0 to P2.2) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	JTAG Mode
TCK/P2.0/TA0.2/ TA1.2/TA1.1	0	P2.0 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		Timer_A1.1	1	1	1	0
		Timer_A0.CCI2A and Timer_A1.CCI2A	0	≠0	≠0	0
		JTAG-TCK (2) (3) (4)	X	X	X	1
TMS/P2.1/TA0.2/ TA1.2/TA0.1	1	P2.1 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		Timer_A0.1	1	1	1	0
		Timer_A0.CCI2B and Timer_A1.CCI2B	0	≠0	≠0	0
		JTAG-TMS (2) (3) (4)	X	X	X	1
TDI/P2.2/TA0.2/TA1.2/ CxOUT/CCI0.0	2	P2.2 (I/O)	I:0, O:1	0	0	0
		Timer_A0.2	1	0	1	0
		Timer_A1.2	1	1	0	0
		CxOUT	1	1	1	0
		Timer_A0.CCI0A	0	≠0	≠0	0
		JTAG-TDI (2) (3) (4)	X	X	X	1

(1) X = Don't care
(2) JTAG signals TMS,TCK and TDI read as "1" when nor configured as explicit JTAG terminals
(3) JTAG overrides digital output control when configured as explicit JTAG terminals
(4) JTAG function with enabled pullup resistors is default after power up

Port P2, P2.3, Input/Output

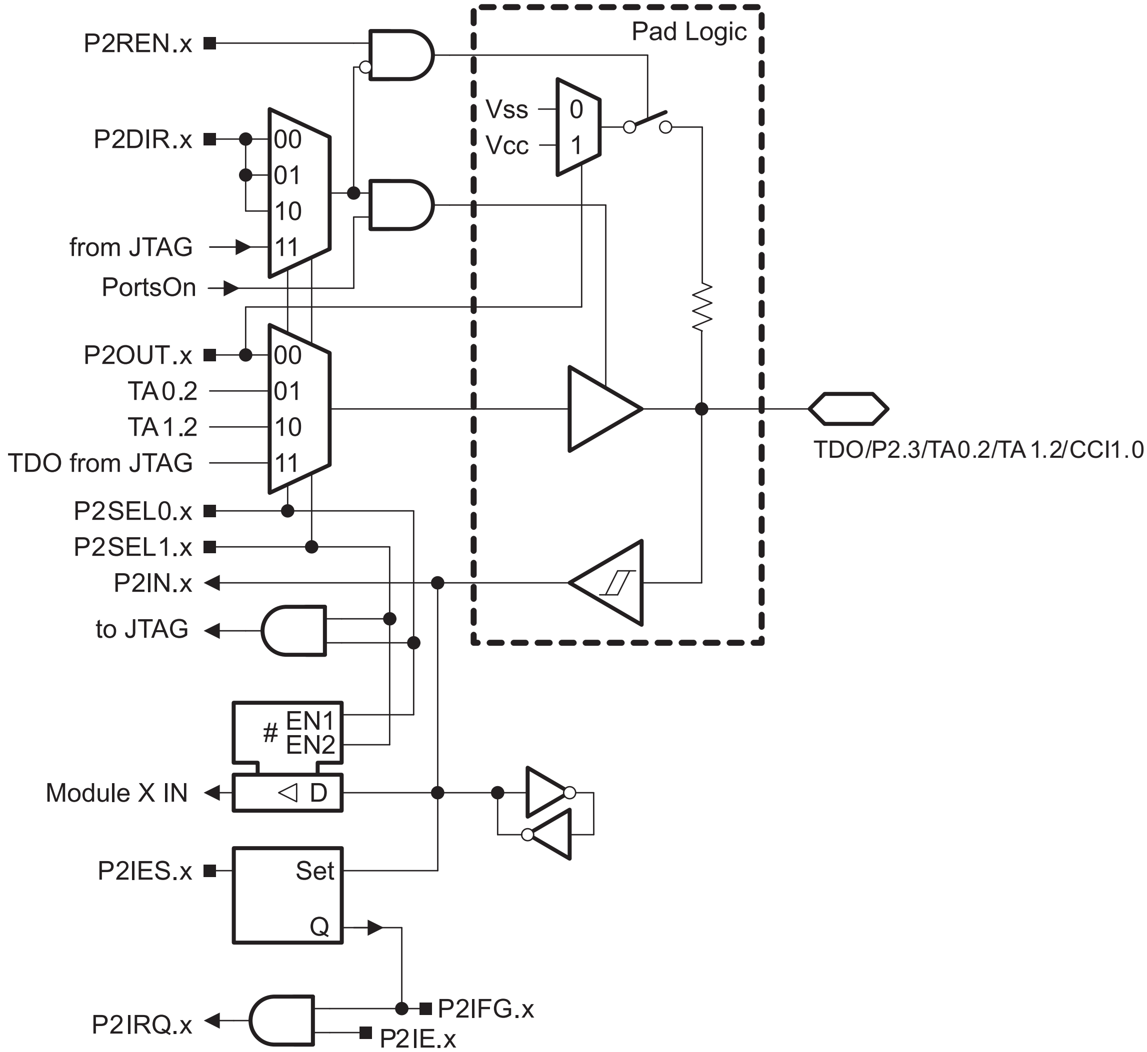


Table 17. Port P2 (P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P2DIR.x	P2SEL1.x	P2SEL0.x
TDO/P2.0/TA0.2/TA1.2/ CCI1.0	3	P2.0 (I/O)	I:0, O:1	0	0
		Timer_A0.2	1	0	1
		Timer_A1.2	1	1	0
		JTAG-TDO(2)(3)	1	1	1
		Timer_A1.CCI0A	0	≠0	≠0

(1) X = Don't care

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430L092CY	PREVIEW	DIESALE	Y	0		TBD	Call TI	Call TI	
MSP430L092SPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
MSP430L092SPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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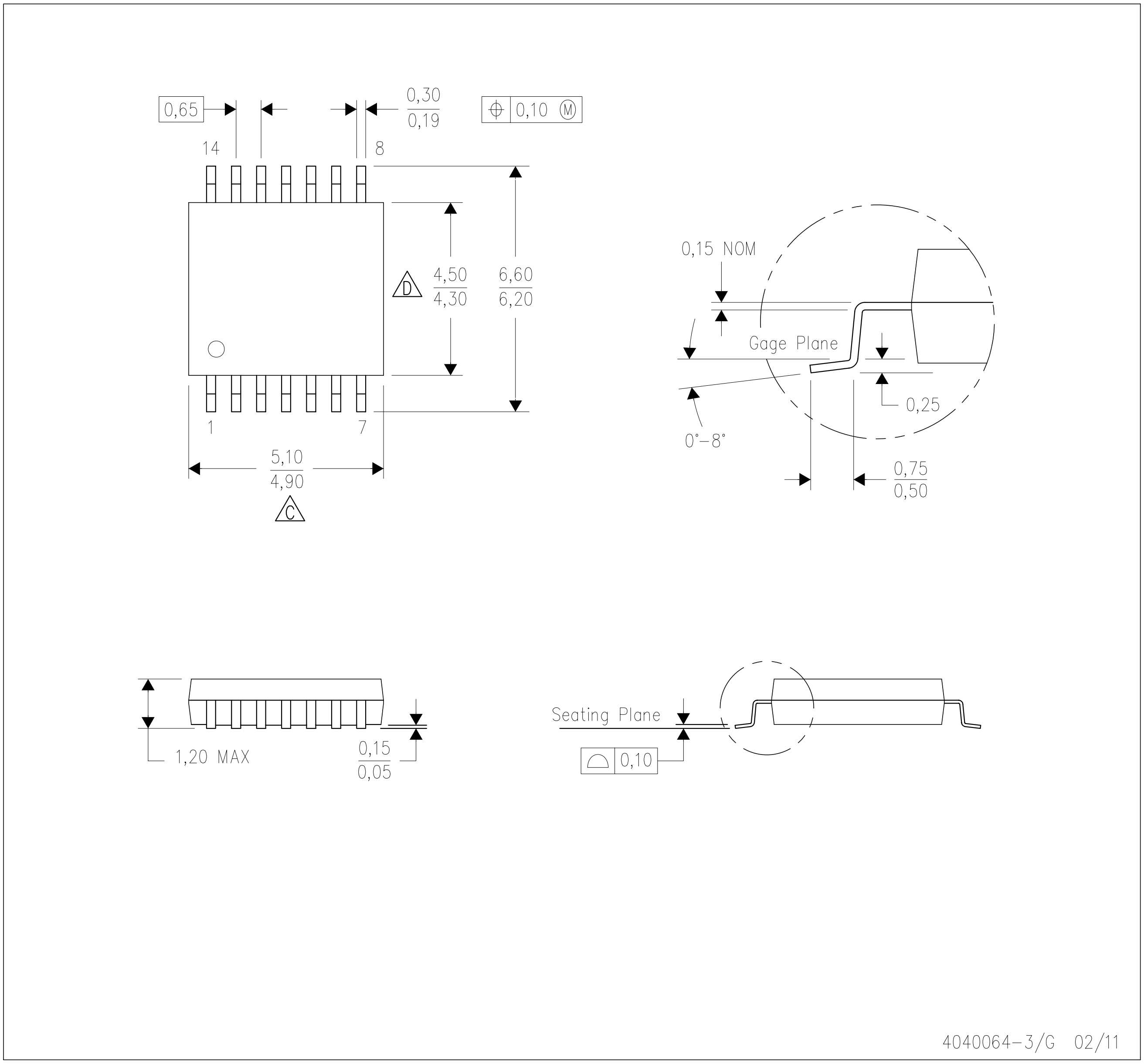
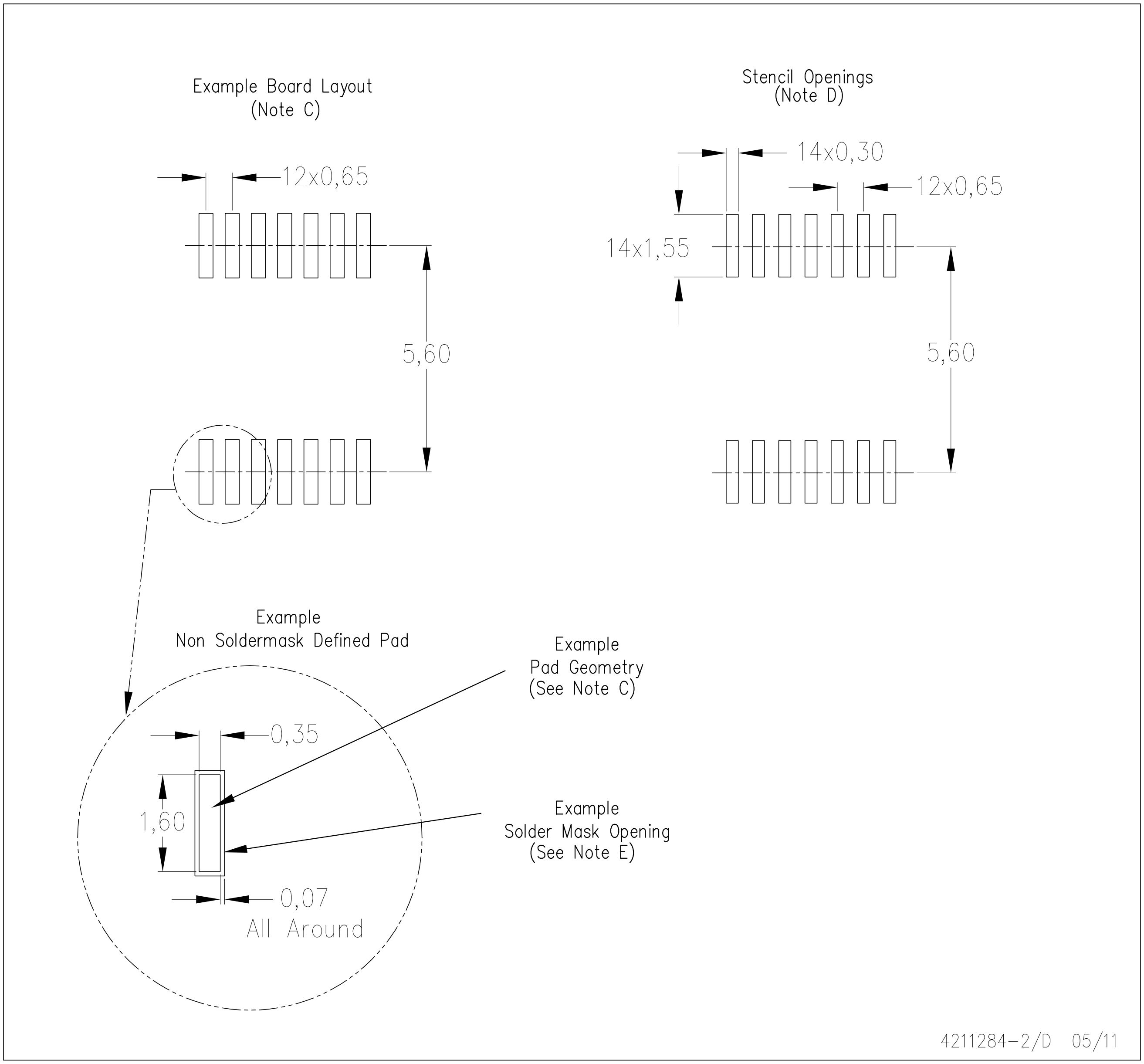
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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