MSP430C313, MSP430P313
MIXED SIGNAL µCONTROLLER

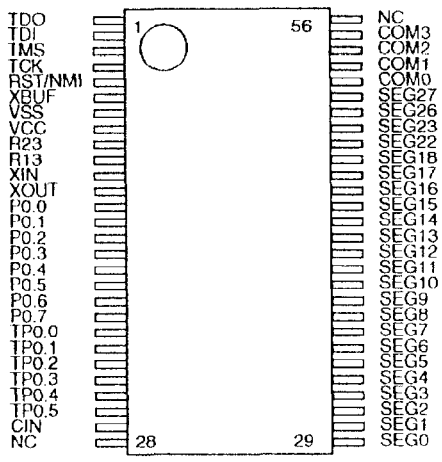
SLASE08 January 1996

- Low supply voltage range 2.5 ... 5.5 V
- Low operation current 400 µA at 1 MHz, 3V
- Ultra-Low Power consumption, in standby mode downto 0.1 µA
- Five power saving modes
- 16 bit RISC architecture 300 ns instruction cycle time
- Built-in LCD Driver for upto 92 segments
- Slope A/D converter possible with external components
- Family members

  MSP430C313: 8K Byte ROM, 256 byte RAM

  MSP430P313: 8K Byte OTP, 256 byte RAM

- EPROM version available for prototyping: MSP430E313

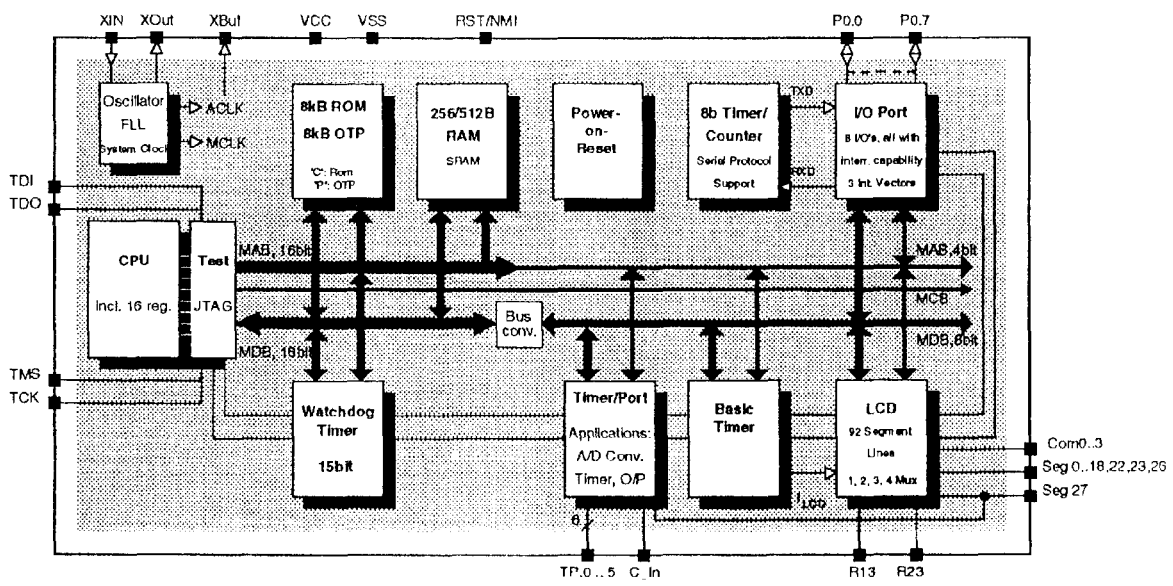


description

The MSP430 is a Microcontroller Family with several members. Each member features a different set of modules targeted to various applications. The MSP430C/P31X series is a µController with a built in LCD drive and the capability to perform Analog-to-Digital conversions via the integrated Timer Port. The µController is designed to be battery operated for an extended periode of time.

Typical applications are sensor systems which pick up analog signals, convert these signals to digital values, process these data and then display them or transmit them to host systems.

block diagram



PRODUCT PREVIEW

TEXAS INSTRUMENTS

short-form description

processing unit

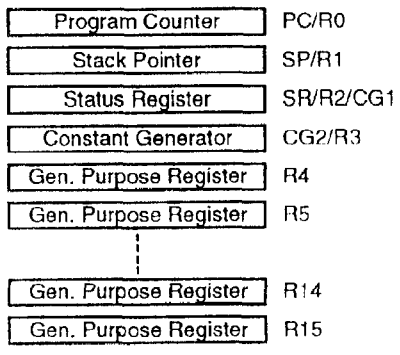
The processing unit is based on a consequent regular and orthogonal designed CPU and instruction set. This design structure results in a **RISC**-like architecture highly transparent for the application development and is distinguished due to ease of programming. All operations beside program flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four for destination operand.

cpu

All **sixteen registers** are located inside the CPU to increase the instruction execution frequency. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register and constant generator.

Peripherals are connected to CPU via data, address and control bus and can be handled easily with all instructions for memory operations.



PRODUCT PREVIEW

instruction set

The instruction set applied to register-register architecture gives a powerful and easy to use assembler language. The instruction set consists of 52 instructions of different functional types with three formats and seven addressing modes:

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g. CALL R8	PC -->(TOS), SR --> (TOS), R8--> PC
Relative jump, un-/conditional	e.g. JNE	Jump on equal bit = 0

Each instruction that can operate on word and byte data is convenient and will be identified by the suffix '.B'.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	ede,toni	MOV.B	ede,toni
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	---	

TEXAS INSTRUMENTS

Adress mode	s	d	Syntax	Example	Operation
* register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 --> R11
* indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
* symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) --> M(TONI)
* absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
* indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
* indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2 --> R10
* immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

Computed branches and subroutine calls are possible using standard instructions. The CALL and BR instructions use the same addressing modes as the other instructions. The addressing modes allow indirect 'indirect' addressing, ideally suited for computed branches and calls. The full use of this programming technique permits a program structure different to conventional 8 and 16bit controllers. Routines can easily work with pointers and stack instead of 'Flag' type program flow control.

operation modes and interrupts

The MSP430 operating modes support in an advanced manner various requirements for ultra-low power and ultra-low energy consumption. It is achieved by the intelligent management of the operations during the different operation mode of modules and CPU states and is fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and return with the RETI instruction to the mode that was selected before the interrupt event. The used clocks are ACLK and MCLK. ACLK is the crystal's frequency and MCLK is a multiple of ACLK and used for the system clock.

There are five operating modes the software can configure:

- Active Mode AM, with different combination of active peripheral modules
- Low Power Mode 0 **LPM0**,
  the CPU is disabled, peripherals operation is not halted, ACLK and MCLK signals are active. loop control for MCLK is active.
- Low Power Mode 1 **LPM1**,
  the CPU is disabled, peripherals operation is not halted, ACLK and MCLK signals are active. loop control for MCLK is inactive.
- Low Power Mode 2 **LPM2**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is active. MCLK and loop control for MCLK are inactive.
- Low Power Mode 3 **LPM3**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is active. MCLK and loop control for MCLK are inactive, DC generator of the DCO (-> MCLK generator) is switched off.
- Low Power Mode 4 **LPM4**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, DC generator of the DCO (-> MCLK generator) is switched off, the crystal oscillator is stopped.

The special function registers SFR's include module enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some current saving functions have been implemented into peripherals which are accessed via the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral that is turned on or off via one register bit.

TEXAS INSTRUMENTS

The most general bits that influence the current consumption and support fast turn-on from low power operating modes are located in the status register SR. There are four bits that control the CPU and the system clock generator, SCG1, SCG0, OscOff and CPUOff:

15 9	8	7							0
reserved for future enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM, address range 0FFFFh - 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

Interrupt source	Interrupt flag	System Interrupt	Word Address	Priority
Power-up ext. Reset Watchdog	 RSTI *) WDI *)	Reset	0FFFEh	15, highest
NMI Osc. fault	RSTI *) OFIFG *)	non-maskable (non)-maskable	0FFFCh	14
Dedicated I/O	P0.0IFG	maskable	0FFFAh	13
Dedicated I/O	P0.1IFG	maskable	0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
			0FFECh	6
Timer/Port	**)	maskable	0FFEAh	5
			0FFE8h	4
			0FFE6h	3
			0FFE4h	2
Basic Timer	BTIFG	maskable	0FFE2h	1
I/O Port 0	P0.27IFG *)	maskable	0FFE0h	0, lowest

*) multiple source flags
**) Timer/Port interrrupt flags are located in the T/P registers

PRODUCT PREVIEW

TEXAS INSTRUMENTS

Special Function Registers

Most of interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple SW access is provided with this arrangement.

Interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h					P0IE.1	P0IE.0	OFIE	WDTIE
					rw-0	rw-0	rw-0	rw-0

WDTIE: Watchdog Timer enable signal
OFIE: Oscillator fault enable signal
P0IE.0: Dedicated I/O P0.0
P0IE.1: P0.1 or 8bitTimer/Counter,RXD

Address	7	6	5	4	3	2	1	0
01h	BTIE					TPIE		
	rw-0					rw-0		

TPIE: Timer/Port enable signal
BTIE: Basic Timer enable signal

Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	P0IFG.1	P0IFG.0	OFIFG	WDTIFG
				rw-0	rw-0	rw-0	rw-1	rw-0

WDTIFG: Set on overflow or security key violation
OR
Reset on VCC power-on or reset condition at RST/NMI-pin
OFIFG Flag set on oscillator fault
P0.0IFG Dedicated I/O P0.0
P0.1IFG P0.1 or 8bit Timer/Counter,RXD
NMIIFG Signal at RST/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG							
	rw							

BTIFG: Basic Timer flag

Module Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
04h								

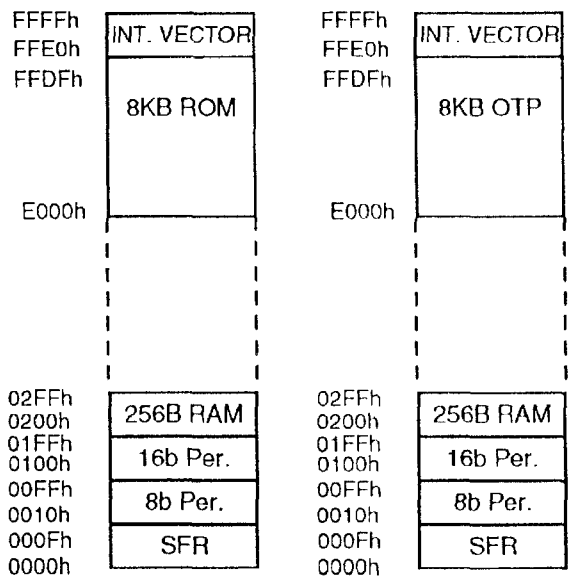
Address	7	6	5	4	3	2	1	0
05h								
	rw							

Legend: rw: Bit can be read and written
rw-0: Bit can be read and written. It is reset by PUC.
SFR bit not present in device

PRODUCT PREVIEW

TEXAS INSTRUMENTS

memory organisation



peripherals

Peripherals are connected to CPU via data, address and control bus and can be handled easily with all instructions for memory operation.

oscillator and system clock

Two clocks are used in the system, the system (Master) clock MCLK and the auxiliary clock ACLK. The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator's frequency. The special design of the oscillator supports feature of low current consumption and the use of a 32 768Hz crystal. The crystal is connected to two pins without any other external components.

The oscillator starts after applying VCC due to reset of the control bit OscOff in the Status Register SR. It can be stopped by setting the OscOff bit. The auxiliary clock ACLK, ACLK/2, ACLK/4 or MCLK frequency can be used externally from the output pin XBUF.

The System Clock of controllers has to operate with different requirements according to the application and system conditions:

- High frequency to react fast onto system hardware requests or events
- Low frequency to minimize current consumption, EMI, ...
- Stable frequency for timer applications e.g. real time clock RTC
- Enable start-stop operation with minimum delay to operation.

All the contrary but essential requirements can not be met neither with high-Q, fast frequency crystals nor with low-Q RC-type oscillators. Proper current consumption and the frequency stability need the application of a low frequency crystal. The compromise used in the MSP430 is to use a low frequency crystal and to multiply its frequency up to the nominal operating range:

$$f_{System} = N \times f_{crystal}$$

The multiplication of the crystal's frequency uses a Frequency-Locked-Loop (FLL) technique. The factor N is recommended to be 32. The FLL technique in combination with a digital controlled oscillator (DCO) provides immediate start-up together with long term crystal stability. The short term variation of clock periods (machine cycles) is less than 20%.

The start-up operation of the system clock depends on the previous machine state. During a PUC the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after removing PUC condition. Proper working condition for the control logic needs the presence of stable crystal oscillation.

digital I/O

There is one eight bit I/O port - Port0 - implemented. Six control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output and interrupt condition is possible.
- Interrupt processing of external events is fully implemented for all eight bits of the port P0.
- Read/write access to all registers with all instructions.

The six registers are:

- Input register 8bits
- Output register 8bits
- Direction register 8bits
- Interrupt Flags 6bits
- Interrupt Edge Select 8bits
- Interrupt Enable 6bits

All these registers contain eight bits except the interrupt flag register and the interrupt enable register. The two LSB's of interrupt flag and enable register are located in the special function register SFR.Three interrupt vectors are implemented, one for Port0.0, one for Port0.1 and one commonly used for any interrupt event on Port0.2 to Port0.7. The Port0.1 and Port0.2 pin function is shared with the 8bit Timer/Counter.

lcd-drive

LC-Displays for static, 2-, 3- and 4-mux operation can be driven directly. The operation of the controller's LCD logic will be defined by SW via memory bit manipulation.The LCD memory is part of the LCD module and apart of the data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily performed using 'table' programming technique combined with the right addressing mode. The segment information is stored into LCD memory using instructions for memory operation.

The drive capability is mainly defined by the external resistor divider that supports the analog levels for 2-, 3- and 4-mux operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430C/P31X has the four common signals and 23 segment lines.

timer/port

The Timer/Port module has two eight bit counters, an input that triggers one counter and six digital outputs with 3-state capability. Both counters have an independent clock selector for selecting an external signal or one of the internal clocks ACLK or MCLK. One of the counters has an extended control capability to halt, count continously or gate the counter by selecting one of two external signals. This gate signal will set the interrupt flag if an external signal is selected and the gate stops the counter.

Both timers can be read and written by software.The two eight bit counters can be cascaded to a sixteen bit counter. A common interrupt vector is implemented and the interrupt flag is set from three events in the eight bit counter mode (gate signal, overflow from the counters) or it is set from two events in the sixteen bit counter mode (gate signal, overflow from MSB of the cascaded counter).

slope A/D converter

The slope A/D conversion can be done with the timer/port module using external resistor(s) for reference (Rref), resistor to be measured (Rmeas) and an external capacitor. The external components are driven by software in a way that the internal counter measures the time that is needed to charge or discharge the capacitor. The reference resistor's (Rref) charge or discharge time are represented by Nref counts. The unknown resistor's (Rmeas) charge or discharge time are represented by Nmeas counts. The unknown resistor's value Rmeas is the value of the reference resistor Rref multiplied by the relative number of counts Nmeas/Nref. It is useful for determine resistive sensor's values that correspond to the physical data e.g. temperature when an NTC or PTC resistor is used.

basic timer

The Basic Timer BT divides the frequency of MCLK or ACLK - selected with signal SSEL - to gain low frequency control signals. This is done within the system with one central divider, the basic timer, to support low current applications.The control register BTCTL holds the flags to control or select the different operational functions. When supply voltage is applied, a reset of the device (RST/NMI pin) or a watchdog overflow or a watchdog security key violation occurred all bits in the register hold undefined or unchanged status. The user's software usually configures the operational conditions on the BT during initialization.

The basic timer has two eight bit timers that can be cascaded to a sixteen bit timer. Both timers can be read and written by software. Three bits in the SFR address range handle the system control interaction according to the function implemented in the basic timer. These three bits are the Basic Timer Module Enable bit BTME, the Basic Timer Interrupt Flag BTIFG and the Basic Timer Interrupt Enable bit BTIE.

watchdog timer

The primary function of the Watchdog Timer module WDT is, to perform a controlled system restart after a S/W hangup has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The watchdog timer counter WDTCNT is a 16bit up-counter, which is not directly accessible by S/W. The WDTCNT is controlled through the watchdog timer control register WDTCTL, which is a 8bit read/write-register. Writing to WDTCTL is, in both operating modes (watchdog or timer), only possible in conjunction with the correct password. A write access to WDTCTL is only possible using the correct password in the high-byte. The low-byte keeps data to be written to WDTCTL and the high-byte has to be the password which is 05Ah. If any other value than 05Ah is written to the high-byte of the WDTCTL a system reset PUC is generated. A read access to WDTCTL is only possible by writing 05Ah as password in the high-byte of the WDTCTL. This avoids an accidental write access on the WDTCTL. Additionally to the Watchdog Timer control bits there are two bits that configure the NMI pin included in the WDTCTL.

8bit timer/counter

The 8bit interval timer supports three major functions for the application:

- serial communication or data exchange
- puls counting or puls accumulation
- timer

The 8bit Timer/Counter peripheral includes following major blocks: an 8bit Up-Counter with pre-load register, an 8bit Control Register, an Input clock selector, an Edge detection (e.g. Start bit detection at asynchronous protocols) and an input and output data latch, triggered by carry-out-signal from 8bit counter.

The 8bit counter counts up with the input clock selected via two control bits of the control register. The four sources are the system clock MCLK, the auxiliary clock ACLK, the external signal from pin P0.1 and the signal from the logical .AND. of MCLK and pin P0.1.

TEXAS INSTRUMENTS

Two inputs at the counter (Load, Enable) control the operation. A load operation loads the counter with the data of the pre-load register. A write access to the counter results in loading the pre-load register content into the counter. The software writes or reads the pre-load register with all instructions. The pre-load register acts as a buffer and can be written immediately after the load of the counter has completed.The second of the two inputs enables the count operation. When the enable signal is set to high the counter will count-up each time a positive clock edge is applied to the clock input of the counter.

Serial protocols like UART protocol need the start bit edge detection to determine at the receiver the start of a data transmission. When this function is activated the counter starts counting after start bit condition is detected. The first signal level is sampled into the RXD input data latch after completing the first timing interval prgrammed into the counter.Two latches for input and output data, RXD_FF and TXD_FF, are clocked by the counter after the programmed timing interval is elapsed.

uart

The serial communication can be realized with software and the 8bit Timer/Counter hardware. The hardware supports the output of the serial data stream bit by bit with the timing determined by the counter. The software/hardware interface connects the mixed signal controller to external devices, systems or networks.

electrical description

absolute maximum ratings

Voltage applied at VCC to VSS	-0.3V to + 6.0V
Voltage applied to any pin (referenced to VSS)	-0.3V to VCC+0.3V
Diode current at any device terminal	± 2 mA
Storage Temperature (unprogrammed device)	-55 ºC to 150 ºC
Storage Temperature (programmed device) -	-40 ºC to 85 ºC

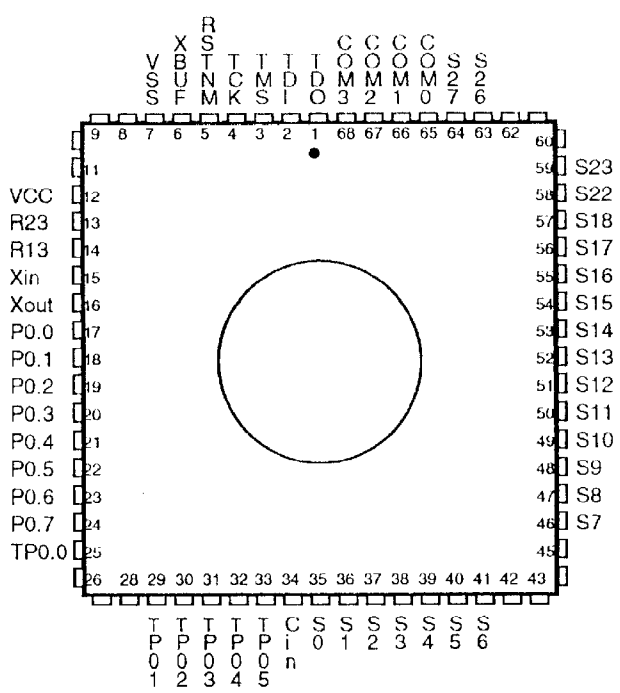
operating conditions

Parameter		MIN	NOM	MAX	Units
Supply Voltage MSP430Cxxx	VCC	2.5		5.5	V
Supply Voltage MSP430P/Exxx		2.7		5.5	
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Operating free-air temperature range:					
Suffix I		-40		+85	°C
XTAL Frequency			32 768		Hz
Processor Frequency	f_{system}				
	VCC=3V	DC		1.1	MHz
	VCC=5V	DC		3.3	MHz

PRODUCT PREVIEW

TEXAS INSTRUMENTS

pinning MSP430E313



PRODUCT PREVIEW

TEXAS INSTRUMENTS

MSP430C323, MSP430P325
MIXED SIGNAL µCONTROLLER

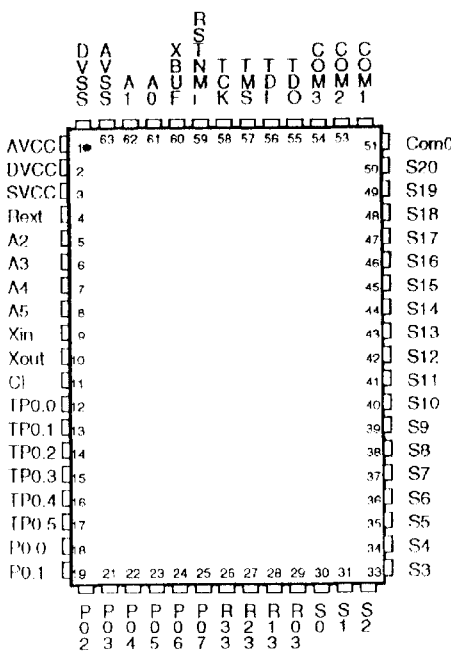
SLASE06 JULY 1995

- Low supply voltage range 2.5 ... 5.5 V
- Low operation current 500 µA at 1 MHz, 3V
- Ultra-Low Power consumption
- Five power saving modes
- 16 bit RISC architecture 1 µs instruction cycle time
- Built-in LCD Driver
- 12+2 bit A/D converter
- Family members

  MSP430C323: 8KB ROM, 256 Byte RAM

  MSP430P325: 16KB OTP, 512 Byte RAM

- EPROM available, MSP430E325

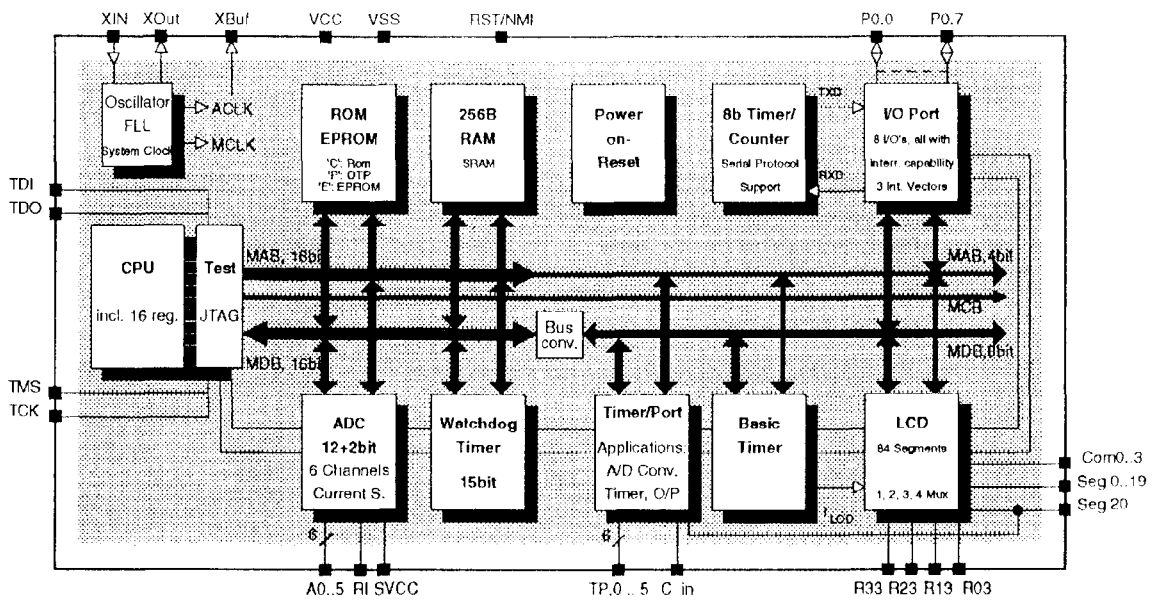


description

The MSP430 is a Microcontroller Family with several members. Each member is featuring a different set of modules targeted to various applications. The µController is designed to be battery operated for an extended period of time.

Typical applications are sensor systems which pick up analog signals, convert these signals to digital values, process these data and then display them or transmit them to host systems.

block diagram



PRODUCT PREVIEW

TEXAS INSTRUMENTS

short-form description

processing unit

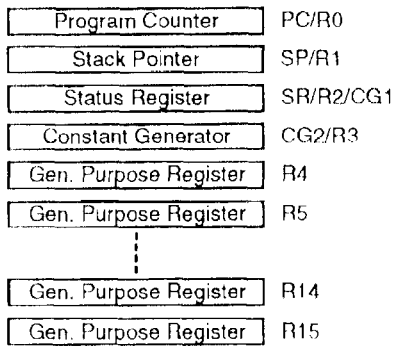
The processing unit is based on a consequent regular and orthogonal designed CPU and instruction set. This design structure results in a **RISC**-like architecture highly transparent for the application development and is distinguished due to ease of programming. All operations beside program flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four for destination operand.

cpu

All **sixteen registers** are located inside the CPU to increase the instruction execution frequency. This reduces a register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register and constant generator.

Peripherals are connected to CPU via data, address and control bus and can be handled easily with all instructions for memory manipulation.



instruction set

The instruction set applied to register-register architecture gives a powerful and easy to use assembler language. The instruction set consists of 52 instructions of different functional types with three formats and seven addressing modes:

Dual operands, source-destination	e.g. ADD	R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g. CALL	R8	PC -->(TOS), SR --> (TOS), R8--> PC
Relative jump, un-/conditional	e.g. JNE		Jump on equal bit = 0

Each instruction that can operate on word and byte data is convenient and will be identified by the suffix '.B'.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	ede,toni	MOV.B	ede,toni
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	---	

TEXAS INSTRUMENTS

Adress mode	s	d	Syntax	Example	Operation
* register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 --> R11
* indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)--> M(6+R6)
* symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) --> M(TONI)
* absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) --> M(TCDAT)
* indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) --> M(Tab+R6)
* indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) --> R11 R10 + 2--> R10
* immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 --> M(TONI)

Computed branches and subroutine calls are possible using standard instructions. The CALL and BR instructions use the same addressing modes as the other instructions. The addressing modes allow indirect 'indirect' addressing, ideally suited for computed branches and calls. The fully use of this programming technique permits a program structure different to conventional 8 and 16bit controllers. A lot of routines can easily deal with pointers and stack instead of 'Flag' type program flow control.

operation modes and interrupts

The MSP430 operating modes support in an advanced manner various requirements for ultra-low power and ultra-low energy consumption. It is achieved by the intelligent management of the operations during the different operation mode of modules and CPU states and is fully supported during interrupt event handling. An interrupt event awakes the system from each of the various operating modes and return with the RETI instruction to the mode that was selected before the interrupt event. The used clocks are ACLK and MCLK. ACLK is the crystal's frequency and MCLK is a multiple of ACLK and used for the system clock.

There are five operating modes the software can configure:

- Active Mode AM, with different combination of active peripheral modules
- Low Power Mode 0 **LPM0**,
  the CPU is disabled, peripherals operation is not halted, ACLK and MCLK signals are active. loop control for MCLK is active.
- Low Power Mode 1 **LPM1**,
  the CPU is disabled, peripherals operation is not halted, ACLK and MCLK signals are active. loop control for MCLK is inactive.
- Low Power Mode 2 **LPM2**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is active. MCLK and loop control for MCLK are inactive.
- Low Power Mode 3 **LPM3**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is active. MCLK and loop control for MCLK are inactive, DC generator of the DCO (-> MCLK generator) is switched off.
- Low Power Mode 4 **LPM4**,
  the CPU is disabled, peripherals operation is not halted, ACLK signal is inactive (crystal oscillator stopped), MCLK and loop control for MCLK are inactive, DC generator of the DCO (-> MCLK generator) is switched off, the crystal oscillator is stopped.

The special function registers SFR's include module enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. Some current saving functions however have been implemented into peripherals that are accessed via the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral that is turned on or off via one register bit.

The most general bits that influence the current consumption and support fast turn-on from low power operating modes are located in the status register SR. There are four bits that control the CPU and the system clock generator, SCG1, SCG0, OscOff and CPUOff:

15 9	8	7							0
reserved for future enhancements	V	**SCG1**	**SCG0**	**OscOff**	**CPUOff**	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM, address range 0FFFFh - 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

Interrupt source	Interrupt flag	System Interrupt	Word Address	Priority
Power-up ext. Reset Watchdog	 RSTI *) WDI *)	Reset	0FFFEh	15, highest
NMI Osc. fault	RSTI *) OFIFG *)	non-maskable (non)-maskable	0FFFCh	14
Dedicated I/O	P0.0IFG	maskable	0FFFAh	13
Dedicated I/O	P0.1IFG	maskable	0FFF8h	12
			0FFF6h	11
Watchdog timer	WDTIFG	maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
			0FFECh	6
ADC	ADCIFG	maskable	0FFEAh	5
Timer/Port	**)	maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
Basic Timer	BTIFG	maskable	0FFE2h	1
I/O Port 0	P0.27IFG *)	maskable	0FFE0h	0, lowest

*) multiple source flags
**) Timer/Port interrupt flags are located in the module

Special Function Registers

Most of interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple SW access is provided with this arrangement.

Interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h					P0IE.1	P0IE.0	OFIE	WDTIE
					rw-0	rw-0	rw-0	rw-0

WDTIE: Watchdog Timer enable signal
OFIE: Oscillator fault enable signal
P0IE.0: Dedicated I/O P0.0
P0IE.1: P0.1 or 8bitTimer/Counter,RXD

Address	7	6	5	4	3	2	1	0
01h	BTIE				TPIE	ADIE		
	rw-0				rw-0	rw-0		

ADIE: A/D converter enable signal
TPIE: Timer/Port enable signal
BTIE: Basic Timer enable signal

Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	P0IFG.1	P0IFG.0	OFIFG	WDTIFG
				rw-0	rw-0	rw-0	rw-1	rw-0

WDTIFG: Set on overflow or security key violation
OR
Reset on VCC power-on or reset condition at`RST/NMI-pin
OFIFG Flag set on oscillator fault
P0.0IFG Dedicated I/O P0.0
P0.1IFG P0.1 or 8bit Timer/Counter,RXD
NMIIFG Signal at`RST/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG							
	rw							

BTIFG: Basic Timer flag

Module Enable Register 1 and 2

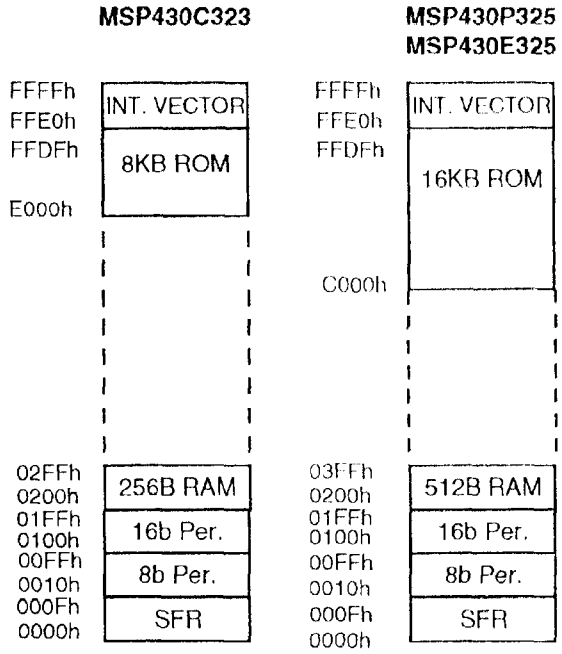
Address	7	6	5	4	3	2	1	0
04h								

Address	7	6	5	4	3	2	1	0
05h								
	rw							

Legend: rw: Bit can be read and written
rw-0: Bit can be read and written. It is reset by PUC.
SFR bit not present in device

PRODUCT PREVIEW

memory organisation



peripherals

Peripherals are connected to CPU via data, address and control bus and can be handled easily with all instructions for memory manipulation.

oscillator and system clock

Two clocks are used in the system, the system (Master) clock MCLK and the auxiliary clock ACLK. The MCLK is a multiple of the ACLK. The ACLK runs with the crystal oscillator's frequency. The special design of the oscillator supports feature of low current consumption and the use of a 32 768Hz crystal. The crystal is connected to two pins without any other external components.

The oscillator starts after applying VCC due to reset of the control bit OscOff in the Status Register SR. It can be stopped by setting the OscOff bit The auxiliary clock ACLK, ACLK/2, ACLK/4 or MCLK frequency can be used externally from the output pin XBUF.

The System Clock of controllers has to deal with different requirements according to the application and system conditions:

- High frequency to react fast onto system hardware requests or events
- Low frequency to minimize current consumption, EMI, ...
- Stable frequency for timer applications e.g. real time clock RTC
- Enable start-stop operation with minimum delay to operation.

All the contrary but essential requirements can not be met neither with high-Q, fast frequency crystals nor with low-Q RC-type oscillators. Proper current consumption and the frequency stability need the application of a low frequency crystal. The compromise used in the MSP430 is to use a low frequency crystal and to multiply its frequency up to the nominal operating range:

$$f_{System} = N \times f_{crystal}$$

The multiplication of the crystal's frequency uses a Frequency-Locked-Loop (FLL) technique. The factor N is recommended to be 32. The FLL technique in combination with a digital controlled oscillator (DCO) provides immediate start-up together with long term crystal stability. The short term variation of clock periods (machine cycles) is less than 20%.

The start-up operation of the system clock depends on the previous machine state. During a PUC the DCO is reset to its lowest possible frequency. The control logic starts operation immediately after removing PUC condition. Proper working condition for the control logic needs the presence of stable crystal oscillation.

digital I/O

There is one eight bit I/O port - Port0 - implemented. Six control registers give maximum flexibility of digital input/output to the application:

- All individual I/O bits are programmable independently.
- Any combination of input, output and interrupt condition is possible.
- Interrupt processing of external events is fully implemented for all eight bits of the port P0.
- Read/write access to all registers with all instructions.

The six registers are:

- Input register 8bits
- Output register 8bits
- Direction register 8bits
- Interrupt Flags 6bits
- Interrupt Edge Select 8bits
- Interrupt Enable 6bits

All these registers contain eight bits except the interrupt flag register and the interrupt enable register. The two LSB's of interrupt flag and enable register are located in the special function register SFR.Three interrupt vectors are implemented, one for Port0.0, one for Port0.1 and one commonly used for any interrupt event on Port0.2 to Port0.7. The Port0.1 and Port0.2 pin function is shared with the 8bit Timer/Counter.

lcd-drive

LC-Displays for static, 2-, 3- and 4-mux operation can be driven directly. The operation of the controller's LCD logic will be defined by SW via memory bit manipulation.The LCD memory is part of the LCD module and apart of the data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily performed using 'table' programming technique combined with the proper addressing mode. The segment information is stored into LCD memory using instructions for memory manipulation.

The drive capability is mainly defined by the external resistor divider that supports the analog levels for 2-, 3- and 4-mux operation. Groups of the LCD segment lines can be selected for digital output signals. The MSP430C310 has the four common signals and 23 segment lines.

a/d converter

The A/D converter is realized as a cascaded converter type and converts analog signals from VCC to GND. It is a 12+2 bit converter with a SW or automatically controlled range select. Five inputs can be selected for analog or digital function. A ratiometric current source can be used on four of the analog pins. The current is adjusted by an external resistor and is enabled/disabled by bits located in the control registers.
The conversion is started by setting the start-of-conversion bit SOC in the control register and the end-of-conversion sets the interrupt flag. The analog input signal is sampled starting with SOC during the next twelve MCLK clocks.
The power-down bit in the control register controls the operating mode of the ADC peripheral. The current consumption and operation is stopped when it is set. The systen reset PUC set the power-down bit.

basic timer

The Basic Timer BT divides the frequency of MCLK or ACLK - selected with signal SSEL - to gain low frequency control signals. This is done within the system with one central divider, the basic timer, to support low current applications.The control register BTCTL holds the flags to control or select the different operational functions. When supply voltage is applied, a reset of the device (RST/NMI pin) or a watchdog overflow or a watchdog security key violation occurred all bits in the register hold undefined or unchanged status. The user's software usually configures the operational conditions on the BT during initialization.

The basic timer has two eight bit timers that can be cascaded for a sixteen bit timer. Both timers can be read and written by software. Three bits in the SFR address range handle the system control interaction according to the function implemented in the basic timer. These three bits are the Basic Timer Module Enable bit BTME, the Basic Timer Interrupt Flag BTIFG and the Basic Timer Interrupt Enable bit BTIE.

watchdog timer

The primary function of the Watchdog Timer module WDT is, to perform a controlled system restart after a S/W upset has occurred. If the selected time interval expires, a system reset is generated. If this watchdog function is not needed in an application, the module can work as an interval timer, which generates an interrupt after the selected time interval.

The watchdog timer counter WDTCNT is a 16bit up-counter, which is not directly accessible by S/W. The WDTCNT is controlled through the watchdog timer control register WDTCTL, which is a 8bit read/write-register. Writing to WDTCTL is, in both operating modes (watchdog or timer), only possible in conjunction with the correct password. A write access to WDTCTL is only possible using the correct password in the high-byte. The low-byte keeps data to be written to WDTCTL and the high-byte has to be the password which is 05Ah. If any other value than 05Ah is written to the high-byte of the WDTCTL a system reset PUC is generated. When the password is read its value is 069h that minimize accidentally write operation to the WDTCTL register.Additionally to the Watchdog Timer control bits there are two bits that configure the NMI pin included in the WDTCTL.

8bit timer/counter

The 8bit interval timer supports three major functions for the application:

- serial communication or data exchange
- puls counting or puls accumulation
- timer

The 8bit Timer/Counter peripheral includes following major blocks: an 8bit Up-Counter with pre-load register, an 8bit Control Register, an Input clock selector, an Edge detection (e.g. Start bit detection at asynchronous protocols) and an input and output data latch, triggered by carry-out-signal from 8bit counter.

The 8bit counter counts up with the input clock selected via two control bits of the control register. The four sources are the system clock MCLK, the auxiliary clock ACLK, the external signal from pin P0.1 and the signal from the logical .AND. of MCLK and pin P0.1.

Two inputs at the counter (Load, Enable) control the operation. A load operation loads the counter with the data of the pre-load register. A write access to the counter results in loading the pre-load register content into the counter. The software writes or reads the pre-load register with all instructions. The pre-load register acts as a buffer and can be written immediately after the load of the counter has completed.The second of the two inputs enable the count operation. When the enable signal is set to high the counter will count-up each time a positive clock edge is applied to the clock input of the counter.

Serial protocols like UART protocol need the start bit edge detection to determine at the receiver the start of a data transmission. When this function is activated the counter starts counting after start bit condition is detected. The first signal level is sampled into the RXD input data latch after completing the first timing interval prgrammed into the counter.Two latches for input and output data, RXD_FF and TXD_FF, are clocked by the counter after the programmed timing interval is elapsed.

uart

The serial communication can be realized by software together with the 8bit Timer/Counter hardware. The hardware supports the output of the serial data stream bit by bit with the timing determined by the counter. The software/hardware interface connects the mixed signal controller to external devices, systems or networks.

timer/port

The Timer/Port module has two eight bit counters, an input that gates one counter and six digital outputs with 3-state capability. Both counters have an independent clock selector for selecting an external signal or one of the internal clocks ACLK or MCLK. One of the counters has an extended control capability to halt, count continuously or gate the counter by selecting one of two external signals. This gate signal will set the interrupt flag if an external signal is selected and the gate stops the counter.

Both timers can be read and written by software.The two eight bit counters can be cascaded to form a sixteen bit counter. A common interrupt vector is implemented and the interrupt flag is set from three events in the eight bit counter mode (gate signal, overflow from the counters) or it is set from two events in the sixteen bit counter mode (gate signal, overflow from MSB of the cascaded counter).

electrical description

absolute maximum ratings

Voltage applied at VCC to VSS	-0.3V to + 6.0V
Voltage applied to any pin (referenced to VSS)	-0.3V to VCC+0.3V
Diode current at any device terminal	+ 2 mA
Storage Temperature (unprogrammed device)	-55 °C to 150 °C
Storage Temperature (programmed device) -	-40 °C to 85 °C

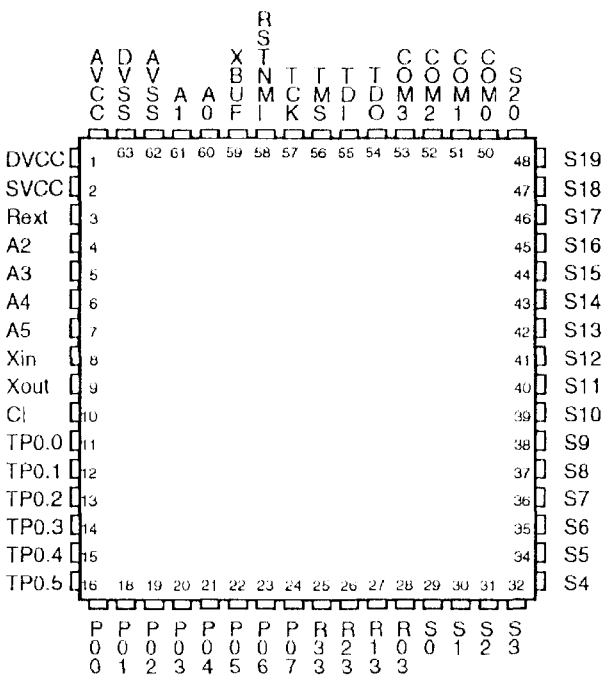
operating conditions

PRODUCT PREVIEW

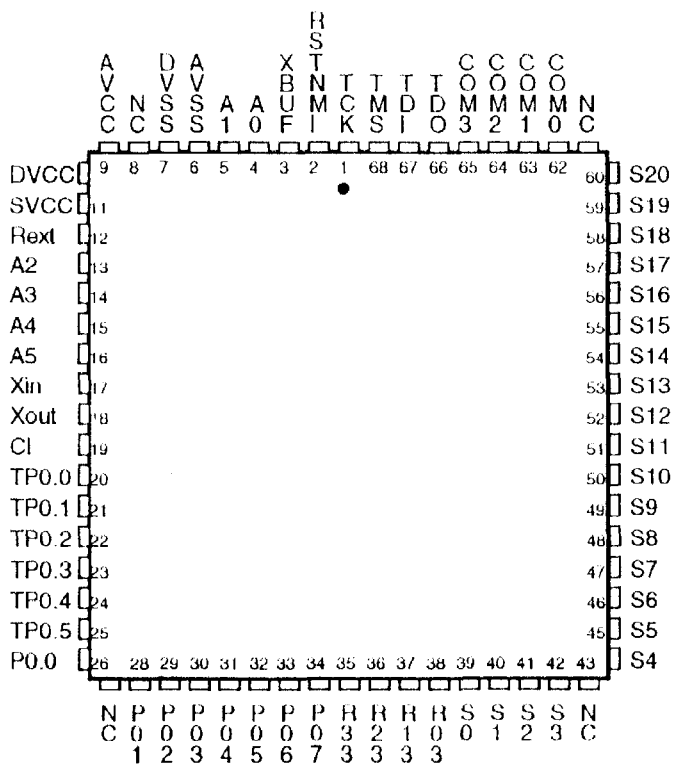
Parameter		MIN	NOM	MAX	Units
Supply Voltage MSP430Cxxx	VCC	2.5		5.5	V
Supply Voltage MSP430P/Exxx		2.7		5.5	
Supply Voltage MSP433Cxxx	V_{CC}	2.5	3.0	3.8	V
Supply Voltage MSP433P/Exxx		2.7	3.0	3.8	
Supply Voltage MSP435Xxxx	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Operating free-air temperature range:					
Suffix Q		-40		+85	°C
XTAL Frequency			32.768		Hz
Processor Frequency ()	f_{system}				
	VCC=3V	DC		1.1	MHz
	VCC=5V	DC		2.2	MHz

TEXAS INSTRUMENTS

pinning MSP43C323, MSP430P325 (PM package)



pinning MSP430E325 (FZ package)



PRODUCT PREVIEW