

## MIXED SIGNAL MICROCONTROLLER

### FEATURES

- **Dual-Supply Voltage Device**
  - Primary Supply (AVCC, DVCC):
    - Powered From External Supply: 3.6 V Down to 1.8 V
    - Up to 22 General-Purpose I/O With up to Four External Interrupts
  - Low-Voltage Interface Supply (DVIO):
    - Powered From Separate External Supply: 1.62 V to 1.98 V
    - Up to 31 General-Purpose I/O With up to Twelve External Interrupts
    - Serial Communications
- **Ultra-Low Power Consumption**
  - Active Mode (AM):
    - All System Clocks Active
    - 290  $\mu$ A/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    - 150  $\mu$ A/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    - Real-Time Clock With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up: 1.9  $\mu$ A at 2.2 V, 2.1  $\mu$ A at 3.0 V (Typical)
    - Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up: 1.4  $\mu$ A at 3.0 V (Typical)
  - Off Mode (LPM4):
    - Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up: 1.1  $\mu$ A at 3.0 V (Typical)
  - Shutdown Mode (LPM4.5):
    - 0.18  $\mu$ A at 3.0 V (Typical)
- **Wake-Up From Standby Mode in 3.5  $\mu$ s (Typical)**
- **16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock**
- **Flexible Power Management System**
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- **Unified Clock System**
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Watch Crystals (XT1)
  - High-Frequency Crystals up to 32 MHz (XT2)
- **16-Bit Timer TA0, Timer\_A With Five Capture/Compare Registers**
- **16-Bit Timer TA1, Timer\_A With Three Capture/Compare Registers**
- **16-Bit Timer TA2, Timer\_A With Three Capture/Compare Registers**
- **16-Bit Timer TB0, Timer\_B With Seven Capture/Compare Shadow Registers**
- **Two Universal Serial Communication Interfaces**
  - USCI\_A0 and USCI\_A1 Each Support:
    - Enhanced UART With Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI\_B0 and USCI\_B1 Each Support:
    - I<sup>2</sup>C™
    - Synchronous SPI
- **10-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold**
- **Comparator**
- **Hardware Multiplier Supports 32-Bit Operations**
- **Serial Onboard Programming, No External Programming Voltage Needed**
- **Three Channel Internal DMA**
- **Basic Timer With Real-Time Clock Feature**
- **Family Members are Summarized in [Table 1](#)**
- **For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* ([SLAU208](#))**
- **For Design Guidelines, See *Designing with MSP430F522x Devices* ([SLAA558](#))**



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## DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in 3.5  $\mu$ s (typical).

The MSP430F522x series are microcontroller configurations with four 16-bit timers, a high-performance 10-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, DMA, comparator, and real-time clock module with alarm capabilities. The MSP430F521x series include all the peripherals of the MSP430F522x series with the exception of the ADC. All devices have a split I/O supply system that allows for a seamless interface to other devices that have a nominal 1.8-V I/O interface without the need for external level translation.

Typical applications include analog and digital sensor systems, data loggers, and various general-purpose applications.

Family members available are summarized in [Table 1](#).

**Table 1. Family Members**

| Device      | Flash (KB) | SRAM (KB) | Timer_A <sup>(1)</sup> | Timer_B <sup>(2)</sup> | USCI                       |                                  | ADC10_A (Ch)  | Comp_B (Ch) | I/O DVCC <sup>(3)</sup> | I/O DVIO <sup>(4)</sup> | Package Type                              |
|-------------|------------|-----------|------------------------|------------------------|----------------------------|----------------------------------|---------------|-------------|-------------------------|-------------------------|-------------------------------------------|
|             |            |           |                        |                        | Channel A: UART, IrDA, SPI | Channel B: SPI, I <sup>2</sup> C |               |             |                         |                         |                                           |
| MSP430F5229 | 128        | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | 10 ext, 2 int | 8           | 22                      | 31                      | 64 RGC<br>64 YFF <sup>(5)</sup><br>80 ZQE |
| MSP430F5227 | 64         | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | 10 ext, 2 int | 8           | 22                      | 31                      | 64 RGC<br>64 YFF <sup>(5)</sup><br>80 ZQE |
| MSP430F5224 | 128        | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | 8 ext, 2 int  | 6           | 20                      | 17                      | 48 RGZ                                    |
| MSP430F5222 | 64         | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | 8 ext, 2 int  | 6           | 20                      | 17                      | 48 RGZ                                    |
| MSP430F5219 | 128        | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | -             | 8           | 22                      | 31                      | 64 RGC<br>64 YFF <sup>(5)</sup><br>80 ZQE |
| MSP430F5217 | 64         | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | -             | 8           | 22                      | 31                      | 64 RGC<br>64 YFF <sup>(5)</sup><br>80 ZQE |
| MSP430F5214 | 128        | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | -             | 6           | 20                      | 17                      | 48 RGZ                                    |
| MSP430F5212 | 64         | 8         | 5, 3, 3                | 7                      | 2                          | 2                                | -             | 6           | 20                      | 17                      | 48 RGZ                                    |

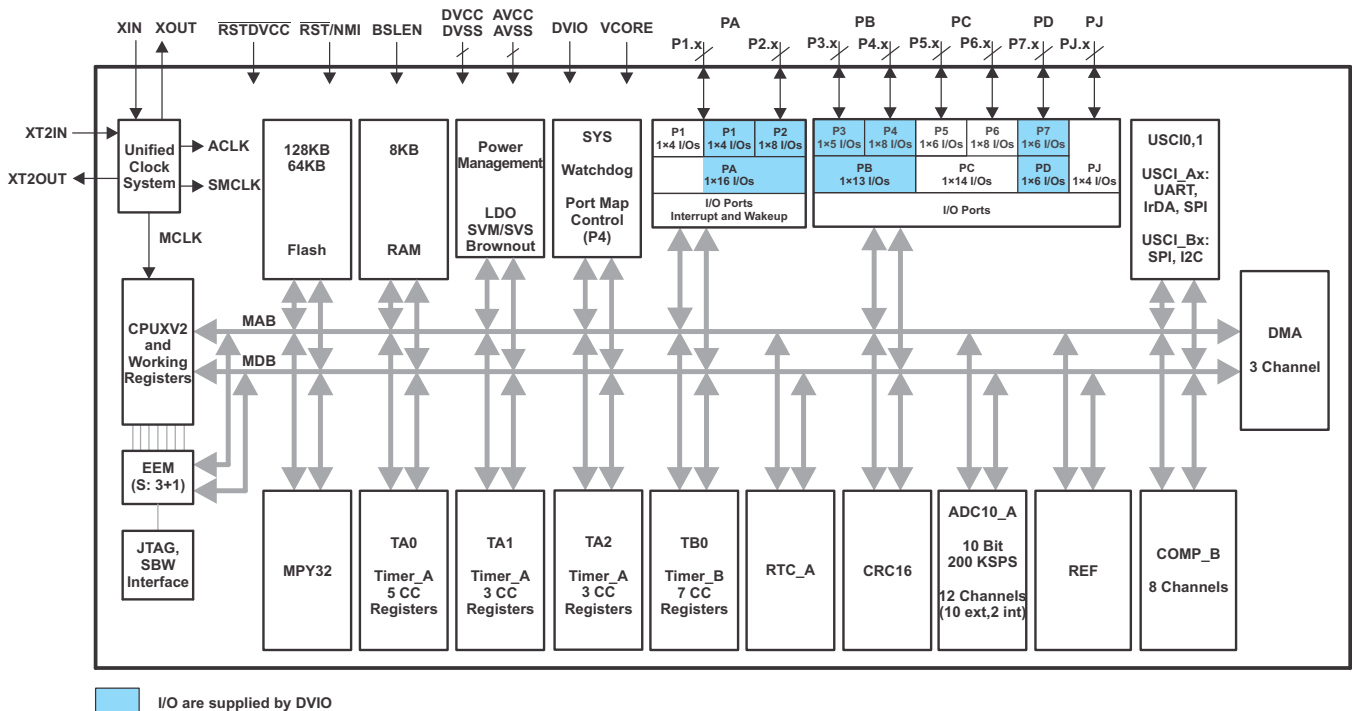
- (1) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) All of these I/O reside on a single voltage rail supplied by DVCC.
- (4) All of these I/O reside on a single voltage rail supplied by DVIO.
- (5) Product Preview

**Table 2. Ordering Information<sup>(1)</sup>**

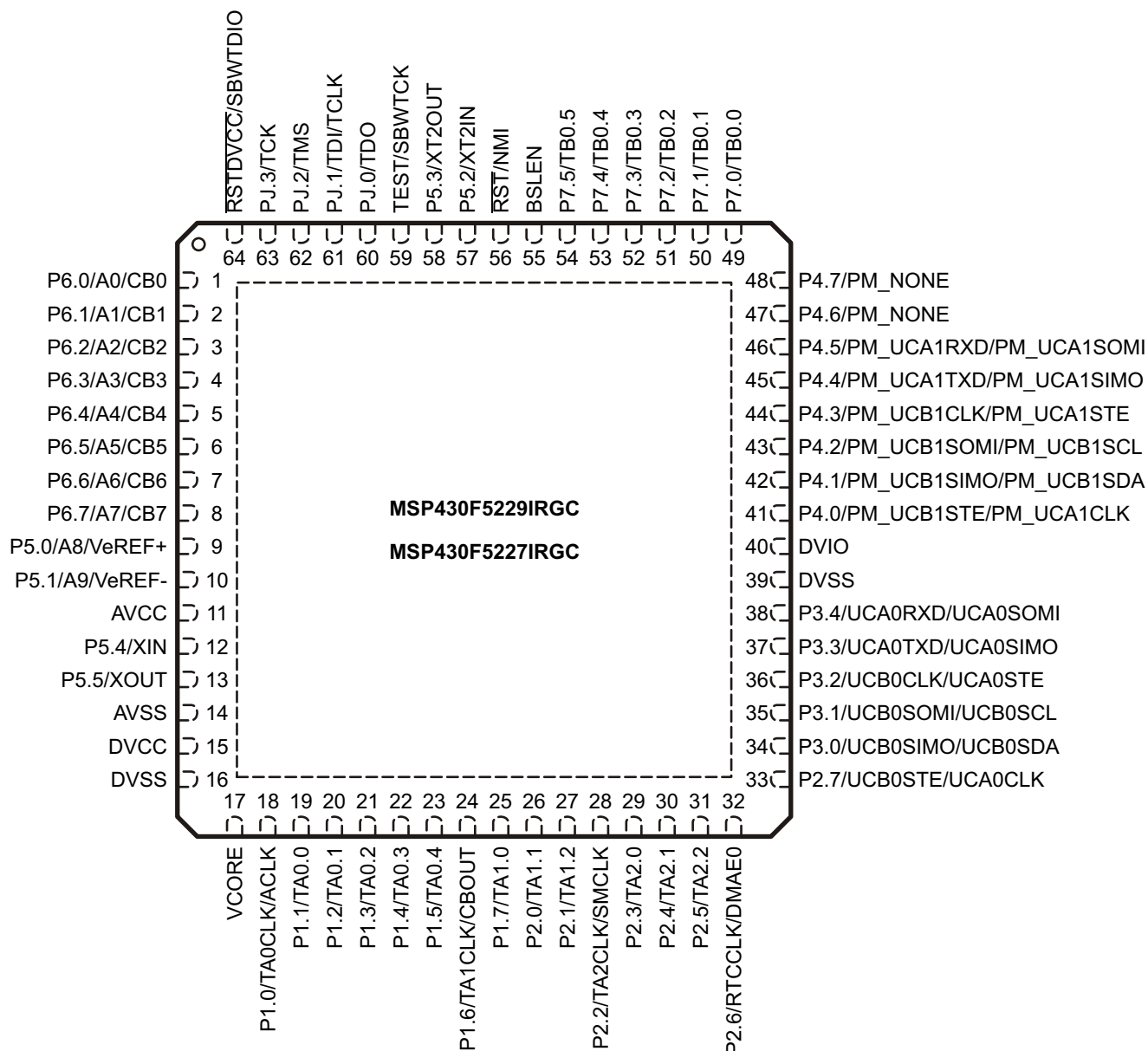
| T <sub>A</sub> | PACKAGED DEVICES <sup>(2)</sup> |                           |                           |                                |
|----------------|---------------------------------|---------------------------|---------------------------|--------------------------------|
|                | PLASTIC 64-PIN VQFN (RGC)       | PLASTIC 48-PIN VQFN (RGZ) | PLASTIC 80-BALL BGA (ZQE) | PLASTIC 64-BALL DSBGA (YFF)    |
| –40°C to 85°C  | MSP430F5229IRGC                 | MSP430F5224IRGZ           | MSP430F5229IZQE           | MSP430F5229IYFF <sup>(3)</sup> |
|                | MSP430F5227IRGC                 | MSP430F5222IRGZ           | MSP430F5227IZQE           | MSP430F5227IYFF <sup>(3)</sup> |
|                | MSP430F5219IRGC                 | MSP430F5214IRGZ           | MSP430F5219IZQE           | MSP430F5219IYFF <sup>(3)</sup> |
|                | MSP430F5217IRGC                 | MSP430F5212IRGZ           | MSP430F5217IZQE           | MSP430F5217IYFF <sup>(3)</sup> |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) Product Preview

## Functional Block Diagram – F5229, F5227 – RGC, ZQE, YFF Packages

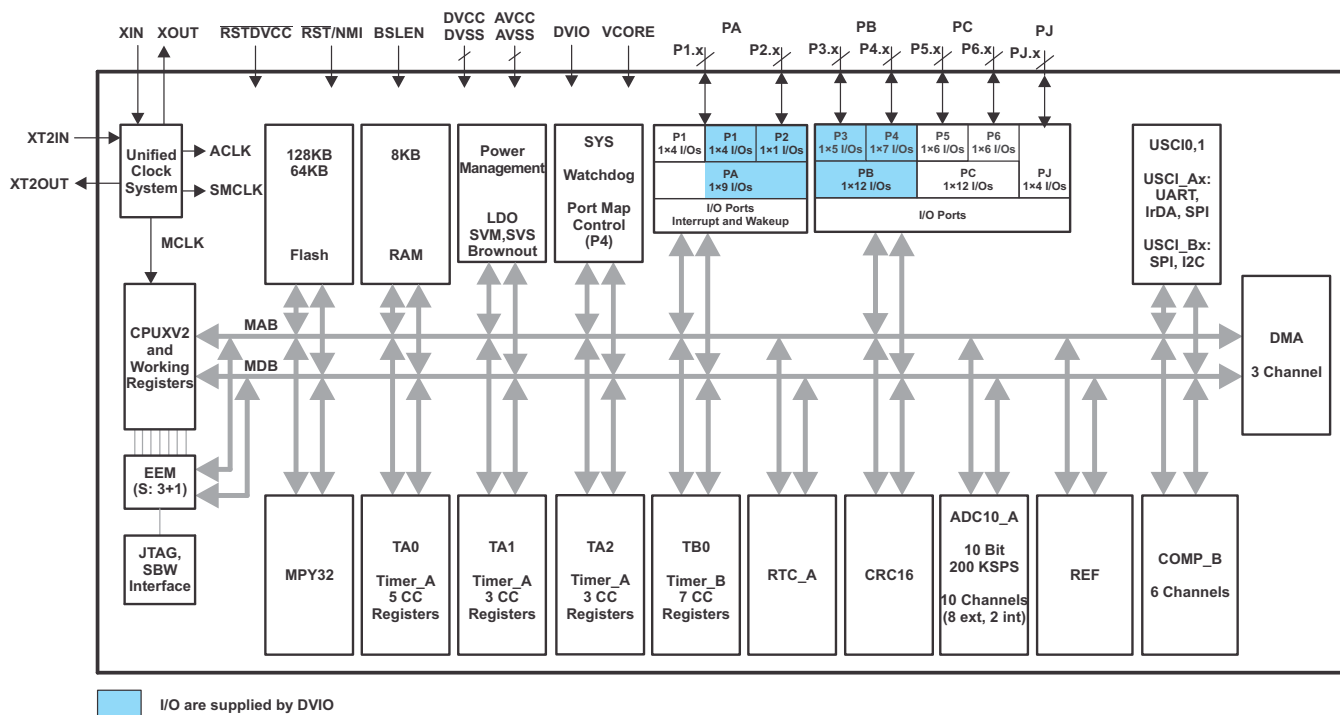


## Pin Designation – F5229, F5227 – RGC Package

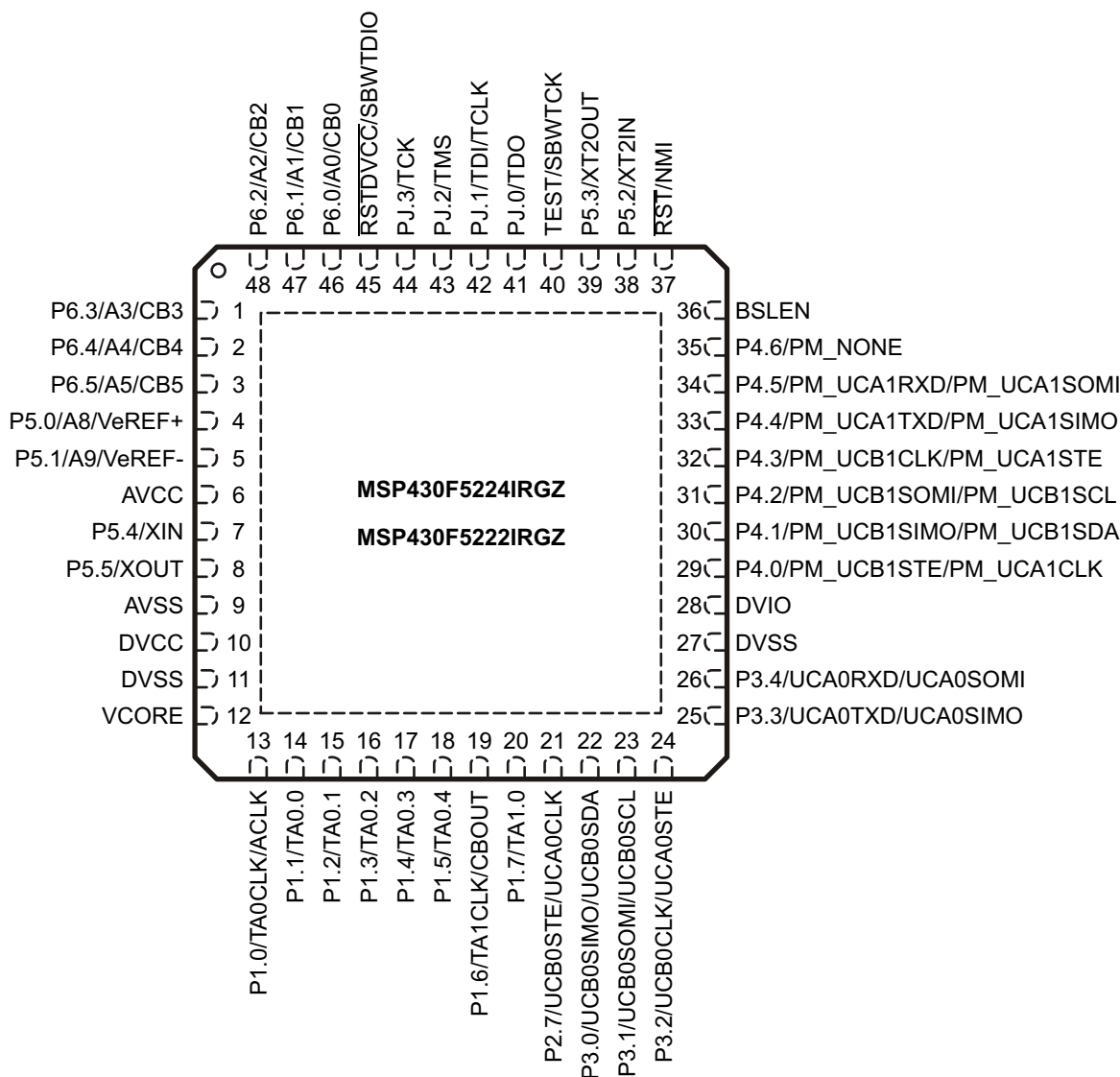


NOTE: Connection of exposed thermal pad to V<sub>SS</sub> is recommended.

## Functional Block Diagram – F5224, F5222 – RGZ Package

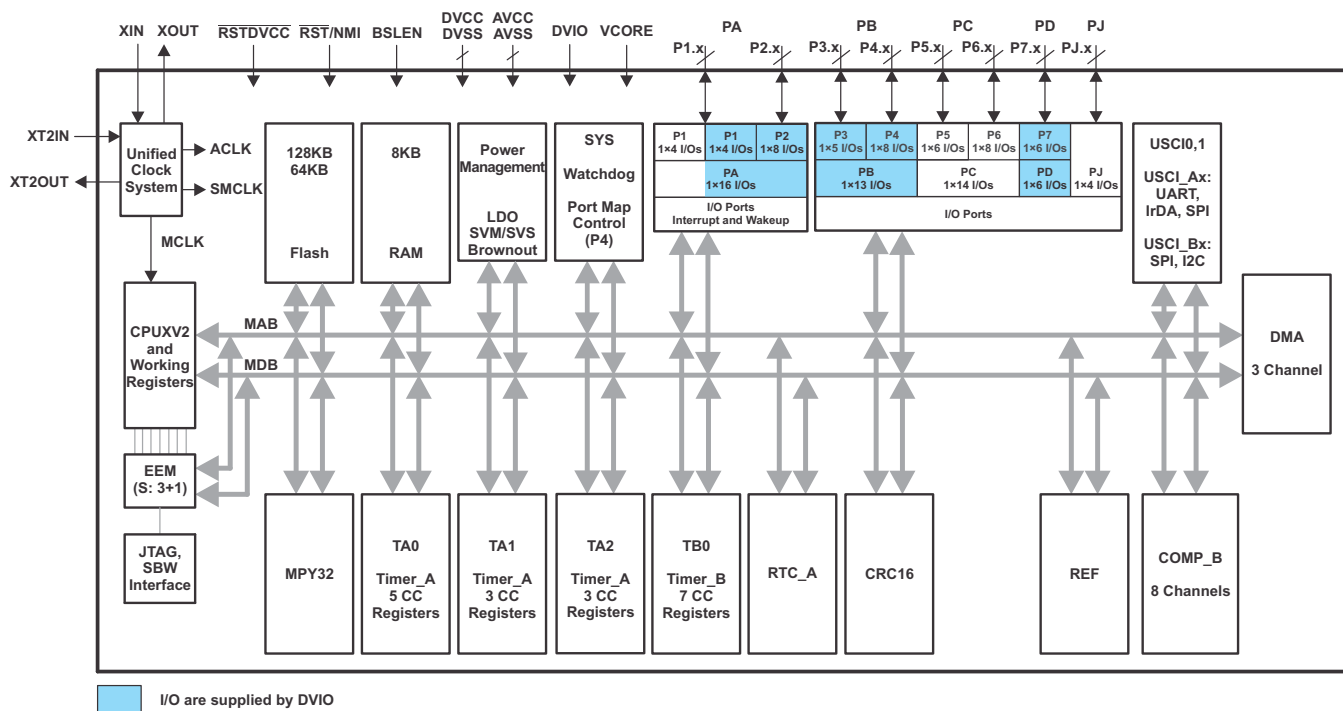


## Pin Designation – F5224, F5222 – RGZ Package

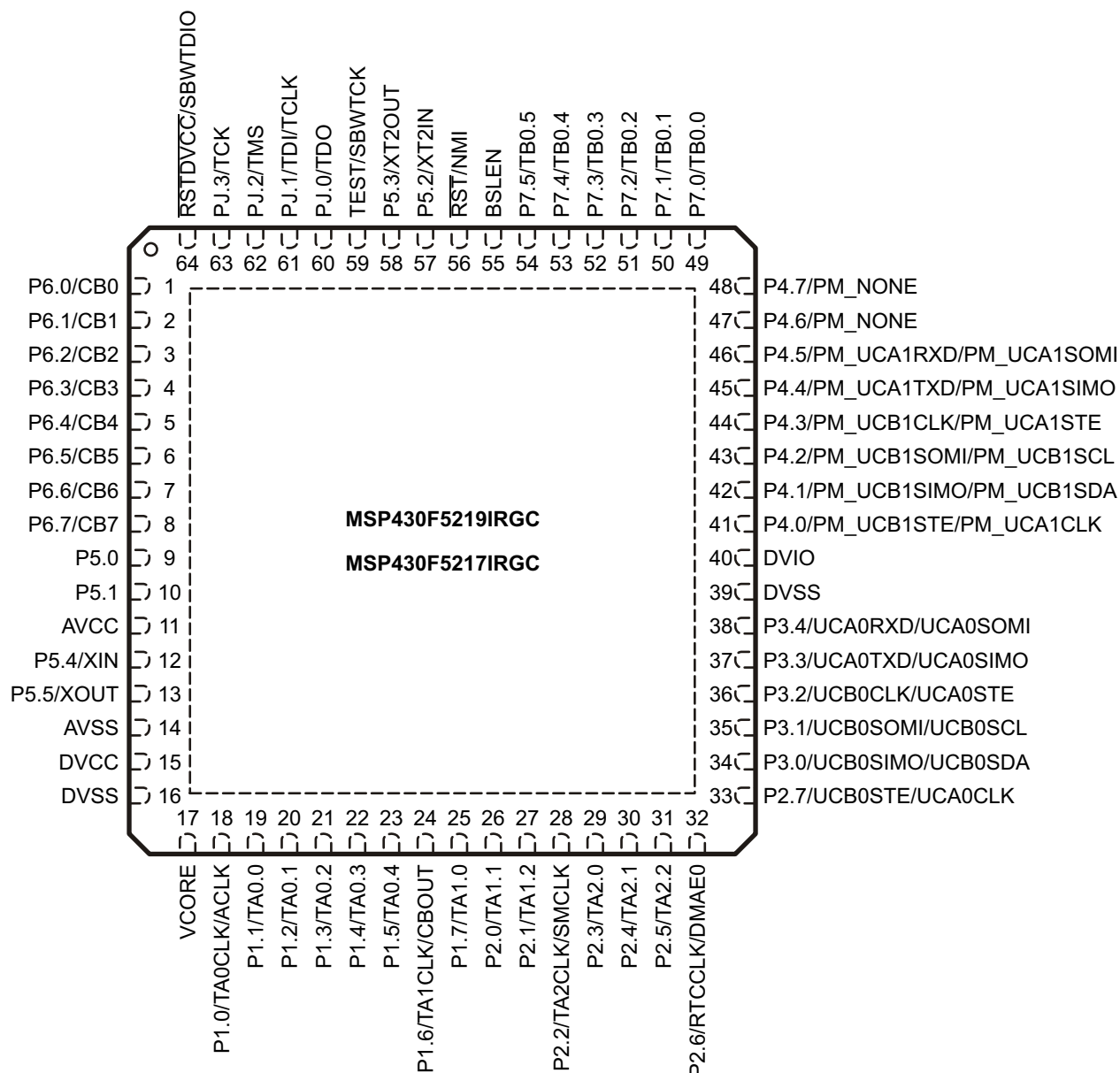


NOTE: Connection of exposed thermal pad to V<sub>SS</sub> is recommended.

## Functional Block Diagram – F5219, F5217 – RGC, ZQE, YFF Packages



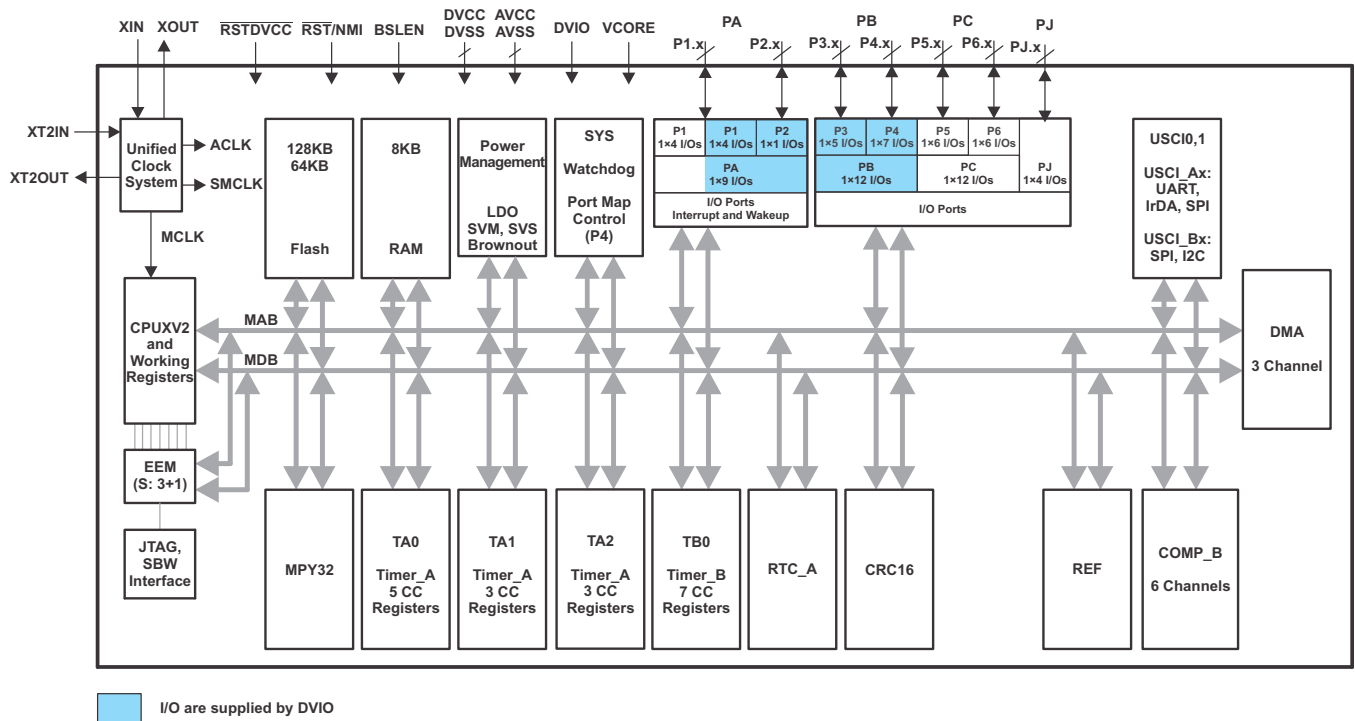
## Pin Designation – F5219, F5217 – RGC Package



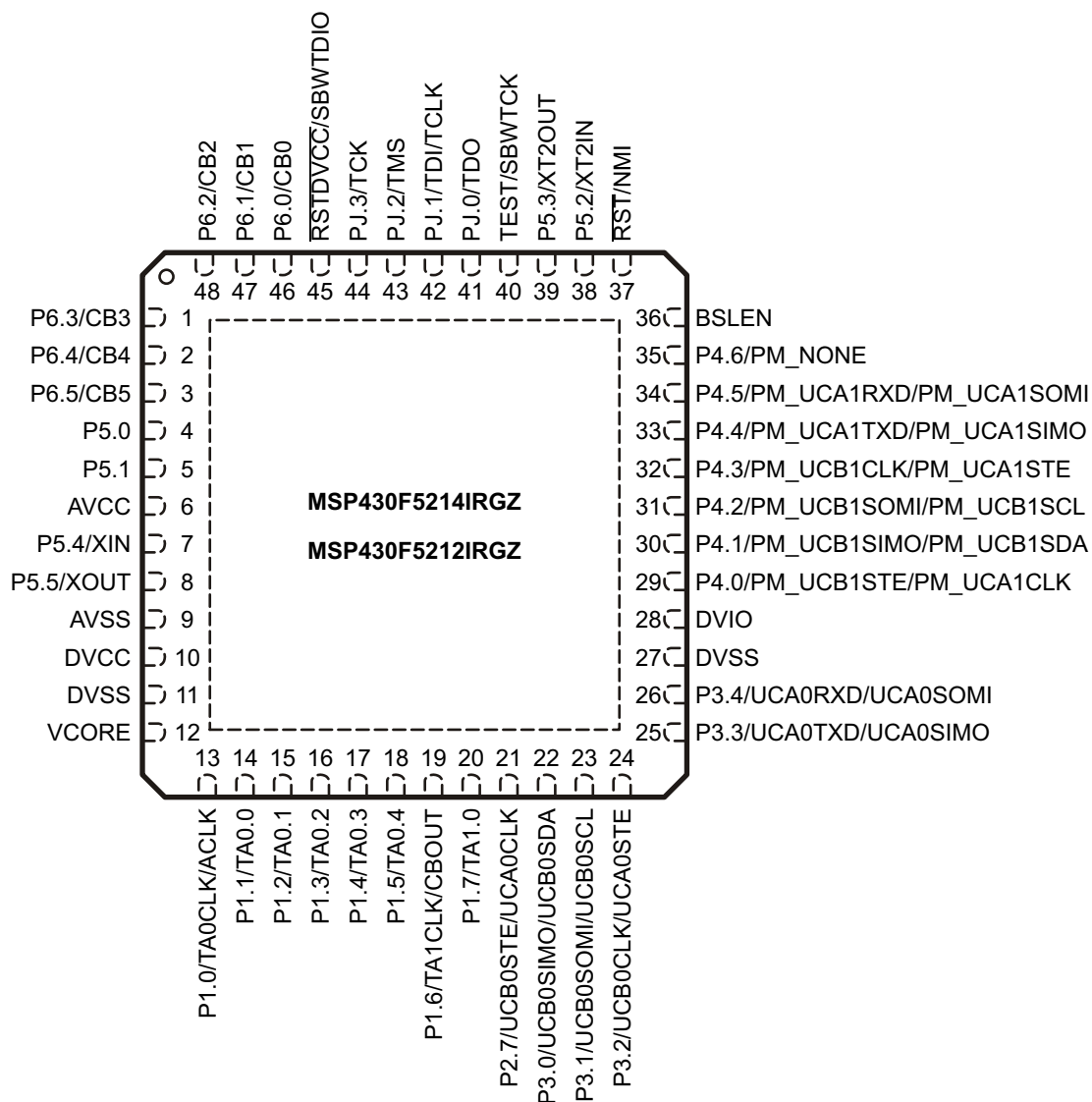
NOTE: Connection of exposed thermal pad to V<sub>SS</sub> is recommended.



## Functional Block Diagram – F5214, F5212 – RGZ Package



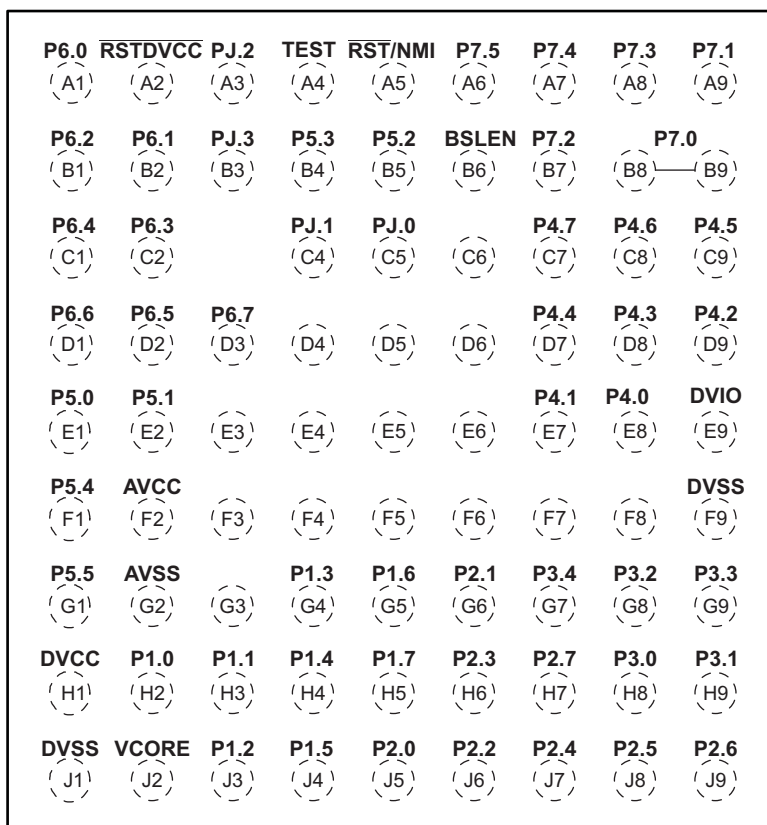
## Pin Designation – F5214, F5212 – RGZ Package



NOTE: Connection of exposed thermal pad to V<sub>SS</sub> is recommended.

**Pin Designation – F5229, F5227, F5219, F5217 – ZQE Package**

**ZQE PACKAGE  
(TOP VIEW)**



**Pin Designation – F5229, F5227, F5219, F5217 – YFF Package**

**YFF PACKAGE  
(TOP VIEW)**

|              |               |                                     |                                     |              |              |              |               |
|--------------|---------------|-------------------------------------|-------------------------------------|--------------|--------------|--------------|---------------|
| P6.1<br>(A1) | P6.4<br>(A2)  | P6.7<br>(A3)                        | P5.1<br>(A4)                        | P5.4<br>(A5) | P5.5<br>(A6) | DVCC<br>(A7) | DVSS<br>(A8)  |
| PJ.3<br>(B1) | P6.2<br>(B2)  | P6.5<br>(B3)                        | P5.0<br>(B4)                        | AVCC<br>(B5) | AVSS<br>(B6) | P1.0<br>(B7) | VCORE<br>(B8) |
| PJ.1<br>(C1) | P6.0<br>(C2)  | P6.3<br>(C3)                        | P6.6<br>(C4)                        | P1.4<br>(C5) | P1.3<br>(C6) | P1.1<br>(C7) | P1.2<br>(C8)  |
| P5.3<br>(D1) | PJ.0<br>(D2)  | PJ.2<br>(D3)                        | $\overline{\text{RSTDVCC}}$<br>(D4) | P2.1<br>(D5) | P1.7<br>(D6) | P1.6<br>(D7) | P1.5<br>(D8)  |
| P5.2<br>(E1) | BSLEN<br>(E2) | $\overline{\text{RST/NMI}}$<br>(E3) | TEST<br>(E4)                        | P4.2<br>(E5) | P2.4<br>(E6) | P2.2<br>(E7) | P2.0<br>(E8)  |
| P7.5<br>(F1) | P7.4<br>(F2)  | P7.2<br>(F3)                        | P4.5<br>(F4)                        | P4.0<br>(F5) | P2.7<br>(F6) | P2.5<br>(F7) | P2.3<br>(F8)  |
| P7.3<br>(G1) | P7.1<br>(G2)  | P4.7<br>(G3)                        | P4.3<br>(G4)                        | P3.4<br>(G5) | P3.2<br>(G6) | P3.1<br>(G7) | P2.6<br>(G8)  |
| P7.0<br>(H1) | P4.6<br>(H2)  | P4.4<br>(H3)                        | P4.1<br>(H4)                        | DVIO<br>(H5) | DVSS<br>(H6) | P3.3<br>(H7) | P3.0<br>(H8)  |

**Package Dimensions:** The package dimensions for the YFF package are shown in [Table 3](#). See the package drawing at the end of this datasheet for more details.

**Table 3. YFF Package Dimensions**

| PACKAGED DEVICES | D            | E            |
|------------------|--------------|--------------|
| MSP430F5229IYFF  | 3.415 ± 0.03 | 3.535 ± 0.03 |
| MSP430F5227IYFF  |              |              |
| MSP430F5219IYFF  |              |              |
| MSP430F5217IYFF  |              |              |

**Table 4. Terminal Functions**

| TERMINAL             |     |     |     |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                 |
|----------------------|-----|-----|-----|-----|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                 | NO. |     |     |     |                    |                                                                                                                                                                                                                             |
|                      | RGC | ZQE | YFF | RGZ |                    |                                                                                                                                                                                                                             |
| P6.4/CB4/A4          | 5   | C1  | A2  | 2   | I/O                | General-purpose digital I/O<br>Comparator_B input CB4<br>Analog input A4 – ADC (not available on all device types)                                                                                                          |
| P6.5/CB5/A5          | 6   | D2  | B3  | 3   | I/O                | General-purpose digital I/O<br>Comparator_B input CB5<br>Analog input A5 – ADC (not available on all device types)                                                                                                          |
| P6.6/CB6/A6          | 7   | D1  | C4  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>Comparator_B input CB6 (not available on all device types)<br>Analog input A6 – ADC (not available on all device types)                                  |
| P6.7/CB7/A7          | 8   | D3  | A3  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>Comparator_B input CB7 (not available on all device types)<br>Analog input A7 – ADC (not available on all device types)                                  |
| P5.0/A8/VeREF+       | 9   | E1  | B4  | 4   | I/O                | General-purpose digital I/O<br>Analog input A8 – ADC (not available on all device types)<br>Input for an external reference voltage to the ADC (not available on all device types)                                          |
| P5.1/A9/VeREF-       | 10  | E2  | A4  | 5   | I/O                | General-purpose digital I/O<br>Analog input A9 – ADC (not available on all device types)<br>Negative terminal for the ADC's reference voltage for an external applied reference voltage (not available on all device types) |
| AVCC                 | 11  | F2  | B5  | 6   |                    | Analog power supply                                                                                                                                                                                                         |
| P5.4/XIN             | 12  | F1  | A5  | 7   | I/O                | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1 <sup>(2)</sup>                                                                                                                                     |
| P5.5/XOUT            | 13  | G1  | A6  | 8   | I/O                | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1                                                                                                                                                    |
| AVSS                 | 14  | G2  | B6  | 9   |                    | Analog ground supply                                                                                                                                                                                                        |
| DVCC                 | 15  | H1  | A7  | 10  |                    | Digital power supply                                                                                                                                                                                                        |
| DVSS                 | 16  | J1  | A8  | 11  |                    | Digital ground supply                                                                                                                                                                                                       |
| VCORE <sup>(3)</sup> | 17  | J2  | B8  | 12  |                    | Regulated core power supply output (internal use only, no external current loading)                                                                                                                                         |
| P1.0/TA0CLK/ACLK     | 18  | H2  | B7  | 13  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 clock signal TA0CLK input<br>ACLK output (divided by 1, 2, 4, 8, 16, or 32)                                                                                          |
| P1.1/TA0.0           | 19  | H3  | C7  | 14  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>BSL transmit output                                                                                               |
| P1.2/TA0.1           | 20  | J3  | C8  | 15  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>BSL receive input                                                                                                 |
| P1.3/TA0.2           | 21  | G4  | C6  | 16  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR2 capture: CCI2A input, compare: Out2 output                                                                                                                      |

(1) I = input, O = output, N/A = not available

(2) When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, it is required that the pin be configured properly for the intended input swing.

(3) VCore is for internal use only. No external current loading is possible. VCore should only be connected to the recommended capacitor value, C<sub>VCore</sub>.

**Table 4. Terminal Functions (continued)**

| TERMINAL                             |     |     |     |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                   |
|--------------------------------------|-----|-----|-----|-----|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                 | NO. |     |     |     |                    |                                                                                                                                                                                                                               |
|                                      | RGC | ZQE | YFF | RGZ |                    |                                                                                                                                                                                                                               |
| P1.4/TA0.3 <sup>(4)</sup>            | 22  | H4  | C5  | 17  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR3 capture: CCI3A input compare: Out3 output                                                                                                                         |
| P1.5/TA0.4 <sup>(4)</sup>            | 23  | J4  | D8  | 18  | I/O                | General-purpose digital I/O with port interrupt<br>TA0 CCR4 capture: CCI4A input, compare: Out4 output                                                                                                                        |
| P1.6/TA1CLK/CBOUT <sup>(4)</sup>     | 24  | G5  | D7  | 19  | I/O                | General-purpose digital I/O with port interrupt<br>TA1 clock signal TA1CLK input<br>Comparator_B output                                                                                                                       |
| P1.7/TA1.0 <sup>(4)</sup>            | 25  | H5  | D6  | 20  | I/O                | General-purpose digital I/O with port interrupt<br>TA1 CCR0 capture: CCI0A input, compare: Out0 output                                                                                                                        |
| P2.0/TA1.1 <sup>(4)</sup>            | 26  | J5  | E8  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA1 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types)                                                |
| P2.1/TA1.2 <sup>(4)</sup>            | 27  | G6  | D5  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA1 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types)                                                |
| P2.2/TA2CLK/SMCLK <sup>(5)</sup>     | 28  | J6  | E7  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA2 clock signal TA2CLK input ; SMCLK output (not available on all device types)                                                       |
| P2.3/TA2.0 <sup>(5)</sup>            | 29  | H6  | F8  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA2 CCR0 capture: CCI0A input, compare: Out0 output (not available on all device types)                                                |
| P2.4/TA2.1 <sup>(5)</sup>            | 30  | J7  | E6  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA2 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types)                                                |
| P2.5/TA2.2 <sup>(5)</sup>            | 31  | J8  | F7  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>TA2 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types)                                                |
| P2.6/RTCCLK/DMAE0 <sup>(5)</sup>     | 32  | J9  | G8  | N/A | I/O                | General-purpose digital I/O with port interrupt (not available on all device types)<br>RTC clock output for calibration (not available on all device types)<br>DMA external trigger input (not available on all device types) |
| P2.7/UCB0STE/UCA0CLK <sup>(5)</sup>  | 33  | H7  | F6  | 21  | I/O                | General-purpose digital I/O<br>Slave transmit enable – USCI_B0 SPI mode<br>Clock signal input – USCI_A0 SPI slave mode<br>Clock signal output – USCI_A0 SPI master mode                                                       |
| P3.0/UCB0SIMO/UCB0SDA <sup>(5)</sup> | 34  | H8  | H8  | 22  | I/O                | General-purpose digital I/O<br>Slave in, master out – USCI_B0 SPI mode<br>I2C data – USCI_B0 I2C mode                                                                                                                         |
| P3.1/UCB0SOMI/UCB0SCL <sup>(5)</sup> | 35  | H9  | G7  | 23  | I/O                | General-purpose digital I/O<br>Slave out, master in – USCI_B0 SPI mode<br>I2C clock – USCI_B0 I2C mode                                                                                                                        |

(4) This pin function is supplied by DVIO. See [Electrical Characteristics](#) for input and output requirements.

(5) This pin function is supplied by DVIO. See [Electrical Characteristics](#) for input and output requirements.

**Table 4. Terminal Functions (continued)**

| TERMINAL                                       |     |     |     |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                    |
|------------------------------------------------|-----|-----|-----|-----|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                           | NO. |     |     |     |                    |                                                                                                                                                                                                                                                                                |
|                                                | RGC | ZQE | YFF | RGZ |                    |                                                                                                                                                                                                                                                                                |
| P3.2/UCB0CLK/UCA0STE <sup>(5)</sup>            | 36  | G8  | G6  | 24  | I/O                | General-purpose digital I/O<br>Clock signal input – USCI_B0 SPI slave mode<br>Clock signal output – USCI_B0 SPI master mode<br>Slave transmit enable – USCI_A0 SPI mode                                                                                                        |
| P3.3/UCA0TXD/UCA0SIMO <sup>(5)</sup>           | 37  | G9  | H7  | 25  | I/O                | General-purpose digital I/O<br>Transmit data – USCI_A0 UART mode<br>Slave in, master out – USCI_A0 SPI mode                                                                                                                                                                    |
| P3.4/UCA0RXD/UCA0SOMI <sup>(5)</sup>           | 38  | G7  | G5  | 26  | I/O                | General-purpose digital I/O<br>Receive data – USCI_A0 UART mode<br>Slave out, master in – USCI_A0 SPI mode                                                                                                                                                                     |
| DVSS                                           | 39  | F9  | H6  | 27  |                    | Digital ground supply                                                                                                                                                                                                                                                          |
| DVIO <sup>(6)</sup>                            | 40  | E9  | H5  | 28  |                    | Digital I/O power supply                                                                                                                                                                                                                                                       |
| P4.0/PM_UCB1STE/<br>PM_UCA1CLK <sup>(5)</sup>  | 41  | E8  | F5  | 29  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave transmit enable – USCI_B1 SPI mode<br>Default mapping: Clock signal input – USCI_A1 SPI slave mode<br>Default mapping: Clock signal output – USCI_A1 SPI master mode |
| P4.1/PM_UCB1SIMO/<br>PM_UCB1SDA <sup>(7)</sup> | 42  | E7  | H4  | 30  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave in, master out – USCI_B1 SPI mode<br>Default mapping: I2C data – USCI_B1 I2C mode                                                                                    |
| P4.2/PM_UCB1SOMI/<br>PM_UCB1SCL <sup>(7)</sup> | 43  | D9  | E5  | 31  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Slave out, master in – USCI_B1 SPI mode<br>Default mapping: I2C clock – USCI_B1 I2C mode                                                                                   |
| P4.3/PM_UCB1CLK/<br>PM_UCA1STE <sup>(7)</sup>  | 44  | D8  | G4  | 32  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Clock signal input – USCI_B1 SPI slave mode<br>Default mapping: Clock signal output – USCI_B1 SPI master mode<br>Default mapping: Slave transmit enable – USCI_A1 SPI mode |
| P4.4/PM_UCA1TXD/<br>PM_UCA1SIMO <sup>(7)</sup> | 45  | D7  | H3  | 33  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Transmit data – USCI_A1 UART mode<br>Default mapping: Slave in, master out – USCI_A1 SPI mode                                                                              |
| P4.5/PM_UCA1RXD/<br>PM_UCA1SOMI <sup>(7)</sup> | 46  | C9  | F4  | 34  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: Receive data – USCI_A1 UART mode<br>Default mapping: Slave out, master in – USCI_A1 SPI mode                                                                               |
| P4.6/PM_NONE <sup>(7)</sup>                    | 47  | C8  | H2  | 35  | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function<br>Default mapping: no secondary function                                                                                                                                                      |
| P4.7/PM_NONE <sup>(7)</sup>                    | 48  | C7  | G3  | N/A | I/O                | General-purpose digital I/O with reconfigurable port mapping secondary function (not available on all device types)<br>Default mapping: no secondary function (not available on all device types)                                                                              |

(6) The voltage on DVIO is not supervised or monitored.

(7) This pin function is supplied by DVIO. See [Electrical Characteristics](#) for input and output requirements.

**Table 4. Terminal Functions (continued)**

| TERMINAL                                          |     |        |     |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                                                                |
|---------------------------------------------------|-----|--------|-----|-----|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                              | NO. |        |     |     |                    |                                                                                                                                                            |
|                                                   | RGC | ZQE    | YFF | RGZ |                    |                                                                                                                                                            |
| P7.0/TB0.0 <sup>(7)</sup>                         | 49  | B8, B9 | H1  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR0 capture: CCI0A input, compare: Out0 output (not available on all device types) |
| P7.1/TB0.1 <sup>(7)</sup>                         | 50  | A9     | G2  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types) |
| P7.2/TB0.2 <sup>(7)</sup>                         | 51  | B7     | F3  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types) |
| P7.3/TB0.3 <sup>(7)</sup>                         | 52  | A8     | G1  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR3 capture: CCI3A input, compare: Out3 output (not available on all device types) |
| P7.4/TB0.4 <sup>(7)</sup>                         | 53  | A7     | F2  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR4 capture: CCI4A input, compare: Out4 output (not available on all device types) |
| P7.5/TB0.5 <sup>(7)</sup>                         | 54  | A6     | F1  | N/A | I/O                | General-purpose digital I/O (not available on all device types)<br>TB0 CCR5 capture: CCI5A input, compare: Out5 output (not available on all device types) |
| BSLEN <sup>(8)</sup>                              | 55  | B6     | E2  | 36  | I                  | BSL enable with internal pulldown                                                                                                                          |
| $\overline{\text{RST}}/\text{NMI}^{(8)}$          | 56  | A5     | E3  | 37  | I                  | Reset input active low <sup>(9)</sup><br>Non-maskable interrupt input <sup>(9)</sup>                                                                       |
| P5.2/XT2IN                                        | 57  | B5     | E1  | 38  | I/O                | General-purpose digital I/O<br>Input terminal for crystal oscillator XT2 <sup>(10)</sup>                                                                   |
| P5.3/XT2OUT                                       | 58  | B4     | D1  | 39  | I/O                | General-purpose digital I/O<br>Output terminal of crystal oscillator XT2                                                                                   |
| TEST/SBWTCK <sup>(11)</sup>                       | 59  | A4     | E4  | 40  | I                  | Test mode pin – Selects four wire JTAG operation<br>Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated                                           |
| PJ.0/TDO <sup>(12)</sup>                          | 60  | C5     | D2  | 41  | I/O                | General-purpose digital I/O<br>JTAG test data output port                                                                                                  |
| PJ.1/TDI/TCLK <sup>(12)</sup>                     | 61  | C4     | C1  | 42  | I/O                | General-purpose digital I/O<br>JTAG test data input or test clock input                                                                                    |
| PJ.2/TMS <sup>(12)</sup>                          | 62  | A3     | D3  | 43  | I/O                | General-purpose digital I/O<br>JTAG test mode select                                                                                                       |
| PJ.3/TCK <sup>(12)</sup>                          | 63  | B3     | B1  | 44  | I/O                | General-purpose digital I/O<br>JTAG test clock                                                                                                             |
| $\overline{\text{RSTDVCC}}/\text{SBWTDIO}^{(12)}$ | 64  | A2     | D4  | 45  | I/O                | Reset input active low <sup>(13)</sup><br>Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated                                               |

(8) This pin function is supplied by DVIO. See [Electrical Characteristics](#) for input and output requirements.

(9) This pin is configurable as reset or NMI and resides on the DVIO supply domain. When driven from external, the input swing levels from DVSS to DVIO are required.

(10) When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, it is required that the pin be configured properly for the intended input swing.

(11) See [Bootstrap Loader \(BSL\)](#) and [JTAG Operation](#) for use with BSL and JTAG functions.

(12) See [JTAG Operation](#) for use with JTAG function.

(13) This non-configurable reset resides on the DVCC supply domain and has an internal pullup to DVCC. When driven from external, input swing levels from DVSS to DVCC are required. This reset must be used for Spy-Bi-Wire communication and is not the same RST/NMI reset as found on other devices in the MSP430 family. Refer to [Bootstrap Loader \(BSL\)](#) and [JTAG Operation](#) for details regarding the usage of this pin.



**Table 4. Terminal Functions (continued)**

| TERMINAL    |     |                 |     |     | I/O <sup>(1)</sup> | DESCRIPTION                                                                                                        |
|-------------|-----|-----------------|-----|-----|--------------------|--------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |                 |     |     |                    |                                                                                                                    |
|             | RGC | ZQE             | YFF | RGZ |                    |                                                                                                                    |
| P6.0/CB0/A0 | 1   | A1              | C2  | 46  | I/O                | General-purpose digital I/O<br>Comparator_B input CB0<br>Analog input A0 – ADC (not available on all device types) |
| P6.1/CB1/A1 | 2   | B2              | A1  | 47  | I/O                | General-purpose digital I/O<br>Comparator_B input CB1<br>Analog input A1 – ADC (not available on all device types) |
| P6.2/CB2/A2 | 3   | B1              | B2  | 48  | I/O                | General-purpose digital I/O<br>Comparator_B input CB2<br>Analog input A2 – ADC (not available on all device types) |
| P6.3/CB3/A3 | 4   | C2              | C3  | 1   | I/O                | General-purpose digital I/O<br>Comparator_B input CB3<br>Analog input A3 – ADC (not available on all device types) |
| Reserved    | N/A | <sup>(14)</sup> | N/A | N/A |                    | Reserved                                                                                                           |
| QFN Pad     | Pad | N/A             | N/A | Pad |                    | QFN package pad. Connection to V <sub>SS</sub> recommended.                                                        |

(14) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

## SHORT-FORM DESCRIPTION

**CPU** ([Link to user's guide](#))

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

## Operating Modes

The MSP430 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wakeup from  $\overline{\text{RST}}$ /NMI, P1, and P2.

## Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 5. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE                                                                                                                                       | INTERRUPT FLAG                                                                                             | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY    |
|--------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|------------------|--------------|-------------|
| <b>System Reset</b><br>Power-Up<br>External Reset<br>Watchdog Timeout, Password Violation<br>Flash Memory Password Violation<br>PMM Password Violation | WDTIFG, KEYV (SYSRSTIV) <sup>(1)(2)</sup>                                                                  | Reset            | 0FFFEh       | 63, highest |
| <b>System NMI</b><br>PMM<br>Vacant Memory Access<br>JTAG Mailbox                                                                                       | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRILIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) <sup>(1)</sup> | (Non)maskable    | 0FFFCh       | 62          |
| <b>User NMI</b><br>NMI<br>Oscillator Fault<br>Flash Memory Access Violation                                                                            | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) <sup>(1)(2)</sup>                                                 | (Non)maskable    | 0FFFAh       | 61          |
| COMP_B                                                                                                                                                 | Comparator B interrupt flags (CBIV) <sup>(1)(3)</sup>                                                      | Maskable         | 0FFF8h       | 60          |
| TB0                                                                                                                                                    | TB0CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFF6h       | 59          |
| TB0                                                                                                                                                    | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) <sup>(1)(3)</sup>                                         | Maskable         | 0FFF4h       | 58          |
| Watchdog Timer_A Interval Timer Mode                                                                                                                   | WDTIFG                                                                                                     | Maskable         | 0FFF2h       | 57          |
| USCI_A0 Receive or Transmit                                                                                                                            | UCA0RXIFG, UCA0TXIFG (UCA0IV) <sup>(1)(3)</sup>                                                            | Maskable         | 0FFF0h       | 56          |
| USCI_B0 Receive or Transmit                                                                                                                            | UCB0RXIFG, UCB0TXIFG (UCB0IV) <sup>(1)(3)</sup>                                                            | Maskable         | 0FFEEh       | 55          |
| ADC10_A                                                                                                                                                | ADC10IFG0 <sup>(1)(3)(4)</sup>                                                                             | Maskable         | 0FFECCh      | 54          |
| TA0                                                                                                                                                    | TA0CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFEAh       | 53          |
| TA0                                                                                                                                                    | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) <sup>(1)(3)</sup>                                         | Maskable         | 0FFE8h       | 52          |
| Reserved                                                                                                                                               | Reserved                                                                                                   | Maskable         | 0FFE6h       | 51          |
| DMA                                                                                                                                                    | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) <sup>(1)(3)</sup>                                                        | Maskable         | 0FFE4h       | 50          |
| TA1                                                                                                                                                    | TA1CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFE2h       | 49          |
| TA1                                                                                                                                                    | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) <sup>(1)(3)</sup>                                         | Maskable         | 0FFE0h       | 48          |
| I/O Port P1                                                                                                                                            | P1IFG.0 to P1IFG.7 (P1IV) <sup>(1)(3)</sup>                                                                | Maskable         | 0FFDEh       | 47          |
| USCI_A1 Receive or Transmit                                                                                                                            | UCA1RXIFG, UCA1TXIFG (UCA1IV) <sup>(1)(3)</sup>                                                            | Maskable         | 0FFDCh       | 46          |
| USCI_B1 Receive or Transmit                                                                                                                            | UCB1RXIFG, UCB1TXIFG (UCB1IV) <sup>(1)(3)</sup>                                                            | Maskable         | 0FFDAh       | 45          |
| TA2                                                                                                                                                    | TA2CCR0 CCIFG0 <sup>(3)</sup>                                                                              | Maskable         | 0FFD8h       | 44          |
| TA2                                                                                                                                                    | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) <sup>(1)(3)</sup>                                         | Maskable         | 0FFD6h       | 43          |
| I/O Port P2                                                                                                                                            | P2IFG.0 to P2IFG.7 (P2IV) <sup>(1)(3)</sup>                                                                | Maskable         | 0FFD4h       | 42          |
| RTC_A                                                                                                                                                  | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) <sup>(1)(3)</sup>                                | Maskable         | 0FFD2h       | 41          |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Only on devices with ADC, otherwise reserved

**Table 5. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG          | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY  |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved         | Reserved <sup>(5)</sup> |                  | 0FFD0h       | 40        |
|                  |                         |                  | ⋮            | ⋮         |
|                  |                         |                  | 0FF80h       | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

## Memory Organization

**Table 6. Memory Organization<sup>(1)</sup>**

|                                          |            | MSP430F5227<br>MSP430F5222<br>MSP430F5217<br>MSP430F5212 | MSP430F5229<br>MSP430F5224<br>MSP430F5219<br>MSP430F5214 |
|------------------------------------------|------------|----------------------------------------------------------|----------------------------------------------------------|
| Memory (flash)<br>Main: interrupt vector | Total Size | 64 KB<br>00FFFFh–00FF80h                                 | 128 KB<br>00FFFFh–00FF80h                                |
| Main: code memory                        | Bank D     | N/A                                                      | 32 KB<br>0243FFh–01C400h                                 |
|                                          | Bank C     | N/A                                                      | 32 KB<br>01C3FFh–014400h                                 |
|                                          | Bank B     | 32 KB<br>0143FFh–00C400h                                 | 32 KB<br>0143FFh–00C400h                                 |
|                                          | Bank A     | 32 KB<br>00C3FFh–004400h                                 | 32 KB<br>00C3FFh–004400h                                 |
| RAM                                      | Sector 3   | 2 KB<br>0043FFh–003C00h                                  | 2 KB<br>0043FFh–003C00h                                  |
|                                          | Sector 2   | 2 KB<br>003BFFh–003400h                                  | 2 KB<br>003BFFh–003400h                                  |
|                                          | Sector 1   | 2 KB<br>0033FFh–002C00h                                  | 2 KB<br>0033FFh–002C00h                                  |
|                                          | Sector 0   | 2 KB<br>002BFFh–002400h                                  | 2 KB<br>002BFFh–002400h                                  |
| TI factory memory (ROM)                  | A          | 128 B<br>001BFFh–001B80h                                 | 128 B<br>001BFFh–001B80h                                 |
|                                          | B          | 128 B<br>001B7Fh–001B00h                                 | 128 B<br>001B7Fh–001B00h                                 |
|                                          | C          | 128 B<br>001AFFh–001A80h                                 | 128 B<br>001AFFh–001A80h                                 |
|                                          | D          | 128 B<br>001A7Fh–001A00h                                 | 128 B<br>001A7Fh–001A00h                                 |
| Information memory (flash)               | Info A     | 128 B<br>0019FFh–001980h                                 | 128 B<br>0019FFh–001980h                                 |
|                                          | Info B     | 128 B<br>00197Fh–001900h                                 | 128 B<br>00197Fh–001900h                                 |
|                                          | Info C     | 128 B<br>0018FFh–001880h                                 | 128 B<br>0018FFh–001880h                                 |
|                                          | Info D     | 128 B<br>00187Fh–001800h                                 | 128 B<br>00187Fh–001800h                                 |

(1) N/A = Not available

**Table 6. Memory Organization<sup>(1)</sup> (continued)**

|                                       |       | <b>MSP430F5227<br/>MSP430F5222<br/>MSP430F5217<br/>MSP430F5212</b> | <b>MSP430F5229<br/>MSP430F5224<br/>MSP430F5219<br/>MSP430F5214</b> |
|---------------------------------------|-------|--------------------------------------------------------------------|--------------------------------------------------------------------|
| Bootstrap loader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh–001600h                                           | 512 B<br>0017FFh–001600h                                           |
|                                       | BSL 2 | 512 B<br>0015FFh–001400h                                           | 512 B<br>0015FFh–001400h                                           |
|                                       | BSL 1 | 512 B<br>0013FFh–001200h                                           | 512 B<br>0013FFh–001200h                                           |
|                                       | BSL 0 | 512 B<br>0011FFh–001000h                                           | 512 B<br>0011FFh–001000h                                           |
| Peripherals                           | Size  | 4 KB<br>000FFFh–0h                                                 | 4 KB<br>000FFFh–0h                                                 |

## Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory via the BSL is protected by an user-defined password. Because the F522x and F521x have split I/O power domains, it is possible to interface with the BSL from either the DVCC or DVIO supply domains. This is useful when the MSP430 is interfacing to a host on the DVIO supply domain. The BSL interface on the DVIO supply domain (see [Table 7](#)) uses the USCI\_A0 module configured as a UART. The BSL interface on the DVCC supply domain (see [Table 8](#)) uses a timer-based UART.

### NOTE

Devices from TI come factory programmed with the timer-based UART BSL only. If the USCI-based BSL is preferred, it is also available, but it must be programmed by the user.

When using the DVIO supply domain for the BSL, entry to the BSL requires a specific sequence on the  $\overline{\text{RST}}/\text{NMI}$  and BLEN pins. [Table 7](#) shows the required pins and their functions. For further details on interfacing to development tools and device programmers, see the *MSP430™ Hardware Tools User's Guide* ([SLAU278](#)). For a complete description of the features of the BSL and its implementation, see the *MSP430™ Programming Via the Bootstrap Loader User's Guide* ([SLAU319](#)). The BSL on the DVIO supply domain uses the USCI\_A0 module configured as a UART.

**Table 7. DVIO BSL Pin Requirements and Functions**

| DEVICE SIGNAL                      | BSL FUNCTION        |
|------------------------------------|---------------------|
| $\overline{\text{RST}}/\text{NMI}$ | External reset      |
| BLEN                               | Enable BSL          |
| P3.3                               | Data transmit       |
| P3.4                               | Data receive        |
| DVCC, AVCC                         | Device power supply |
| DVIO                               | I/O power supply    |
| DVSS                               | Ground supply       |

### NOTE

To invoke the BSL from the DVIO domain, the  $\overline{\text{RST}}/\text{NMI}$  and BLEN pins must be used for the entry sequence (see [DVIO BSL Entry](#)). It is critical not to confuse the  $\overline{\text{RST}}/\text{NMI}$  pin with the  $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$  pin. In other MSP430 devices, SBWTDIO is shared with the  $\overline{\text{RST}}/\text{NMI}$  pin and  $\overline{\text{RSTDVCC}}$  does not exist. Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* ([SLAA558](#)).

For applications in which it is desirable to have BSL communication based on the DVCC supply domain, entry to the BSL requires a specific sequence on the  $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$  and TEST/SBWTK pins. [Table 8](#) shows the required pins and their function.

**Table 8. DVCC BSL Pin Requirements and Functions**

| DEVICE SIGNAL                              | BSL FUNCTION        |
|--------------------------------------------|---------------------|
| $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ | External reset      |
| TEST/SBWTK                                 | Enable BSL          |
| P1.1                                       | Data transmit       |
| P1.2                                       | Data receive        |
| DVCC, AVCC                                 | Device power supply |
| DVIO                                       | I/O power supply    |
| DVSS                                       | Ground supply       |

**NOTE**

To invoke the BSL from the DVCC domain, the RSTDVCC/SBWTIO and TEST/SBWTCK pins must be used for the entry sequence. It is critical not to confuse the RST/NMI pin with the RSTDVCC/SBWTIO pin. In other MSP430 devices, SBWTIO is shared with the RST/NMI pin and RSTDVCC does not exist. Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* (SLAA558).

**JTAG Operation****JTAG Standard Interface**

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RSTDVCC/SBWTIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 9. For further details on interfacing to development tools and device programmers, see the *MSP430™ Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430™ Programming Via the JTAG Interface* (SLAU320). Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* (SLAA558).

**Table 9. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL         | DIRECTION | FUNCTION                    |
|-----------------------|-----------|-----------------------------|
| PJ.3/TCK              | IN        | JTAG clock input            |
| PJ.2/TMS              | IN        | JTAG state control          |
| PJ.1/TDI/TCLK         | IN        | JTAG data input, TCLK input |
| PJ.0/TDO              | OUT       | JTAG data output            |
| TEST/SBWTCK           | IN        | Enable JTAG pins            |
| <u>RSTDVCC/SBWTIO</u> | IN        | External reset              |
| DVCC, AVCC            |           | Device power supply         |
| DVIO                  |           | I/O power supply            |
| DVSS                  |           | Ground supply               |

**NOTE**

Traditionally, on other MSP430 devices, the RST/NMI pin is used for SBWTIO, so care must be taken not to mistakenly use the incorrect pin. On the F522x and F521x series of devices, it is required to use RSTDVCC for SBWTIO as shown in Table 9. Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* (SLAA558).

**Spy-Bi-Wire Interface**

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 10. For further details on interfacing to development tools and device programmers, see the *MSP430™ Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320). Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* (SLAA558).

**Table 10. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL         | DIRECTION | FUNCTION                      |
|-----------------------|-----------|-------------------------------|
| TEST/SBWTCK           | IN        | Spy-Bi-Wire clock input       |
| <u>RSTDVCC/SBWTIO</u> | IN, OUT   | Spy-Bi-Wire data input/output |
| DVCC, AVCC            |           | Device power supply           |



**Table 10. Spy-Bi-Wire Pin Requirements and Functions (continued)**

| DEVICE SIGNAL | DIRECTION | FUNCTION         |
|---------------|-----------|------------------|
| DVIO          |           | I/O power supply |
| DVSS          |           | Ground supply    |

#### **NOTE**

Traditionally, on other MSP430 devices, the RST/NMI pin is used for SBWTDIO, so care must be taken not to mistakenly use the incorrect pin. On the F522x and F521x series of devices, it is required to use RSTDVCC for SBWTDIO as shown in [Table 10](#). Additional information can be found in *Designing with MSP430F522x and MSP430F521x Devices* ([SLAA558](#)).

### **Flash Memory ([Link to user's guide](#))**

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

### **RAM Memory ([Link to user's guide](#))**

The RAM memory is made up of n sectors. Each sector can be completely powered down to reduce leakage; however, all data is lost during power down. Features of the RAM memory include:

- RAM memory has n sectors. The sizes of the sectors can be found in [Memory Organization](#).
- Each sector 0 to n can be complete disabled; however, all data in a sector is lost when it is disabled.
- Each sector 0 to n automatically enters low-power retention mode when possible.

## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)*.

### Digital I/O ([Link to user's guide](#))

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

### Port Mapping Controller ([Link to user's guide](#))

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4.

**Table 11. Port Mapping Mnemonics and Functions**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION                                               | OUTPUT PIN FUNCTION          |
|-------|-----------------|------------------------------------------------------------------|------------------------------|
| 0     | PM_NONE         | None                                                             | DVSS                         |
| 1     | PM_CBOUT0       | -                                                                | COMP_B output                |
|       | PM_TB0CLK       | TB0 clock input                                                  |                              |
| 2     | PM_ADC10CLK     | -                                                                | ADC10CLK                     |
|       | PM_DMAE0        | DMAE0 input                                                      |                              |
| 3     | PM_SVMOUT       | -                                                                | SVM output                   |
|       | PM_TB0OUTH      | TB0 high-impedance input TB0OUTH                                 |                              |
| 4     | PM_TB0CCR0A     | TB0 CCR0 capture input CCI0A                                     | TB0 CCR0 compare output Out0 |
| 5     | PM_TB0CCR1A     | TB0 CCR1 capture input CCI1A                                     | TB0 CCR1 compare output Out1 |
| 6     | PM_TB0CCR2A     | TB0 CCR2 capture input CCI2A                                     | TB0 CCR2 compare output Out2 |
| 7     | PM_TB0CCR3A     | TB0 CCR3 capture input CCI3A                                     | TB0 CCR3 compare output Out3 |
| 8     | PM_TB0CCR4A     | TB0 CCR4 capture input CCI4A                                     | TB0 CCR4 compare output Out4 |
| 9     | PM_TB0CCR5A     | TB0 CCR5 capture input CCI5A                                     | TB0 CCR5 compare output Out5 |
| 10    | PM_TB0CCR6A     | TB0 CCR6 capture input CCI6A                                     | TB0 CCR6 compare output Out6 |
| 11    | PM_UCA1RXD      | USCI_A1 UART RXD (direction controlled by USCI - input)          |                              |
|       | PM_UCA1SOMI     | USCI_A1 SPI slave out master in (direction controlled by USCI)   |                              |
| 12    | PM_UCA1TXD      | USCI_A1 UART TXD (direction controlled by USCI - output)         |                              |
|       | PM_UCA1SIMO     | USCI_A1 SPI slave in master out (direction controlled by USCI)   |                              |
| 13    | PM_UCA1CLK      | USCI_A1 clock input/output (direction controlled by USCI)        |                              |
|       | PM_UCB1STE      | USCI_B1 SPI slave transmit enable (direction controlled by USCI) |                              |
| 14    | PM_UCB1SOMI     | USCI_B1 SPI slave out master in (direction controlled by USCI)   |                              |
|       | PM_UCB1SCL      | USCI_B1 I2C clock (open drain and direction controlled by USCI)  |                              |
| 15    | PM_UCB1SIMO     | USCI_B1 SPI slave in master out (direction controlled by USCI)   |                              |
|       | PM_UCB1SDA      | USCI_B1 I2C data (open drain and direction controlled by USCI)   |                              |
| 16    | PM_UCB1CLK      | USCI_B1 clock input/output (direction controlled by USCI)        |                              |
|       | PM_UCA1STE      | USCI_A1 SPI slave transmit enable (direction controlled by USCI) |                              |
| 17    | PM_CBOUT1       | None                                                             | COMP_B output                |
| 18    | PM_MCLK         | None                                                             | MCLK                         |
| 19    | PM_RTCCLK       | None                                                             | RTCCLK output                |
| 20    | PM_UCA0RXD      | USCI_A0 UART RXD (direction controlled by USCI - input)          |                              |
|       | PM_UCA0SOMI     | USCI_A0 SPI slave out master in (direction controlled by USCI)   |                              |

**Table 11. Port Mapping Mnemonics and Functions (continued)**

| VALUE                    | PxMAPy MNEMONIC | INPUT PIN FUNCTION                                                                                                        | OUTPUT PIN FUNCTION |
|--------------------------|-----------------|---------------------------------------------------------------------------------------------------------------------------|---------------------|
| 21                       | PM_UCA0TXD      | USCI_A0 UART TXD (direction controlled by USCI - output)                                                                  |                     |
|                          | PM_UCA0SIMO     | USCI_A0 SPI slave in master out (direction controlled by USCI)                                                            |                     |
| 22                       | PM_UCA0CLK      | USCI_A0 clock input/output (direction controlled by USCI)                                                                 |                     |
|                          | PM_UCB0STE      | USCI_B0 SPI slave transmit enable (direction controlled by USCI)                                                          |                     |
| 23                       | PM_UCB0SOMI     | USCI_B0 SPI slave out master in (direction controlled by USCI)                                                            |                     |
|                          | PM_UCB0SCL      | USCI_B0 I2C clock (open drain and direction controlled by USCI)                                                           |                     |
| 24                       | PM_UCB0SIMO     | USCI_B0 SPI slave in master out (direction controlled by USCI)                                                            |                     |
|                          | PM_UCB0SDA      | USCI_B0 I2C data (open drain and direction controlled by USCI)                                                            |                     |
| 25                       | PM_UCB0CLK      | USCI_B0 clock input/output (direction controlled by USCI)                                                                 |                     |
|                          | PM_UCA0STE      | USCI_A0 SPI slave transmit enable (direction controlled by USCI)                                                          |                     |
| 26 - 30                  | Reserved        | None                                                                                                                      | DVSS                |
| 31 (0FFh) <sup>(1)</sup> | PM_ANALOG       | Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals |                     |

(1) The value of the PM\_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

**Table 12. Default Mapping**

| PIN                        | PxMAPy MNEMONIC        | INPUT PIN FUNCTION                                                                                                                | OUTPUT PIN FUNCTION |
|----------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------|---------------------|
| P4.0/P4MAP0                | PM_UCB1STE/PM_UCA1CLK  | USCI_B1 SPI slave transmit enable (direction controlled by USCI)<br>USCI_A1 clock input/output (direction controlled by USCI)     |                     |
| P4.1/P4MAP1                | PM_UCB1SIMO/PM_UCB1SDA | USCI_B1 SPI slave in master out (direction controlled by USCI)<br>USCI_B1 I2C data (open drain and direction controlled by USCI)  |                     |
| P4.2/P4MAP2                | PM_UCB1SOMI/PM_UCB1SCL | USCI_B1 SPI slave out master in (direction controlled by USCI)<br>USCI_B1 I2C clock (open drain and direction controlled by USCI) |                     |
| P4.3/P4MAP3                | PM_UCB1CLK/PM_UCA1STE  | USCI_A1 SPI slave transmit enable (direction controlled by USCI)<br>USCI_B1 clock input/output (direction controlled by USCI)     |                     |
| P4.4/P4MAP4                | PM_UCA1TXD/PM_UCA1SIMO | USCI_A1 UART TXD (Direction controlled by USCI - output)<br>USCI_A1 SPI slave in master out (direction controlled by USCI)        |                     |
| P4.5/P4MAP5                | PM_UCA1RXD/PM_UCA1SOMI | USCI_A1 UART RXD (Direction controlled by USCI - input)<br>USCI_A1 SPI slave out master in (direction controlled by USCI)         |                     |
| P4.6/P4MAP6                | PM_NONE                | None                                                                                                                              | DVSS                |
| P4.7/P4MAP7 <sup>(1)</sup> | PM_NONE                | None                                                                                                                              | DVSS                |

(1) Not available on all devices

## Oscillator and System Clock ([Link to user's guide](#))

The clock system in the MSP430F522x, MSP430F521x family of devices is supported by the Unified Clock System (UCS) module, which includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in 3.5  $\mu$ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### **Power Management Module (PMM) ([Link to user's guide](#))**

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

### **Hardware Multiplier ([Link to user's guide](#))**

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

### **Real-Time Clock (RTC\_A) ([Link to user's guide](#))**

The RTC\_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC\_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC\_A also supports flexible alarm functions and offset-calibration hardware.

### **Watchdog Timer (WDT\_A) ([Link to user's guide](#))**

The primary function of the watchdog timer (WDT\_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

## System Module (SYS) [\(Link to user's guide\)](#)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader (BSL) entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism when using JTAG that is called a JTAG mailbox and that can be used in the application.

**Table 13. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER     | ADDRESS | INTERRUPT EVENT                     | VALUE      | PRIORITY |
|-------------------------------|---------|-------------------------------------|------------|----------|
| <b>SYSRSTIV, System Reset</b> | 019Eh   | No interrupt pending                | 00h        |          |
|                               |         | Brownout (BOR)                      | 02h        | Highest  |
|                               |         | $\overline{\text{RST}}$ /NMI (BOR)  | 04h        |          |
|                               |         | PMMSWBOR (BOR)                      | 06h        |          |
|                               |         | Wakeup from LPMx.5                  | 08h        |          |
|                               |         | Security violation (BOR)            | 0Ah        |          |
|                               |         | SVSL (POR)                          | 0Ch        |          |
|                               |         | SVSH (POR)                          | 0Eh        |          |
|                               |         | SVML_OVP (POR)                      | 10h        |          |
|                               |         | SVMH_OVP (POR)                      | 12h        |          |
|                               |         | PMMSWPOR (POR)                      | 14h        |          |
|                               |         | WDT timeout (PUC)                   | 16h        |          |
|                               |         | WDT password violation (PUC)        | 18h        |          |
|                               |         | KEYV flash password violation (PUC) | 1Ah        |          |
|                               |         | Reserved                            | 1Ch        |          |
|                               |         | Peripheral area fetch (PUC)         | 1Eh        |          |
|                               |         | PMM password violation (PUC)        | 20h        |          |
|                               |         | Reserved                            | 22h to 3Eh | Lowest   |
| <b>SYSSNIV, System NMI</b>    | 019Ch   | No interrupt pending                | 00h        |          |
|                               |         | SVMLIFG                             | 02h        | Highest  |
|                               |         | SVMHIFG                             | 04h        |          |
|                               |         | SVSMLDLYIFG                         | 06h        |          |
|                               |         | SVSMHDLYIFG                         | 08h        |          |
|                               |         | VMAIFG                              | 0Ah        |          |
|                               |         | JMBINIFG                            | 0Ch        |          |
|                               |         | JMBOUTIFG                           | 0Eh        |          |
|                               |         | SVMLVLRIFG                          | 10h        |          |
|                               |         | SVMHVLRIFG                          | 12h        |          |
|                               |         | Reserved                            | 14h to 1Eh | Lowest   |
|                               |         |                                     |            |          |
| <b>SYSUNIV, User NMI</b>      | 019Ah   | No interrupt pending                | 00h        |          |
|                               |         | NMIFG                               | 02h        | Highest  |
|                               |         | OFIFG                               | 04h        |          |
|                               |         | ACCVIFG                             | 06h        |          |
|                               |         | Reserved                            | 08h        |          |
|                               |         | Reserved                            | 0Ah to 1Eh | Lowest   |

**DMA Controller ([Link to user's guide](#))**

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10\_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

**Table 14. DMA Trigger Assignments<sup>(1)</sup>**

| TRIGGER | CHANNEL                  |                          |                          |
|---------|--------------------------|--------------------------|--------------------------|
|         | 0                        | 1                        | 2                        |
| 0       | DMAREQ                   | DMAREQ                   | DMAREQ                   |
| 1       | TA0CCR0 CCIFG            | TA0CCR0 CCIFG            | TA0CCR0 CCIFG            |
| 2       | TA0CCR2 CCIFG            | TA0CCR2 CCIFG            | TA0CCR2 CCIFG            |
| 3       | TA1CCR0 CCIFG            | TA1CCR0 CCIFG            | TA1CCR0 CCIFG            |
| 4       | TA1CCR2 CCIFG            | TA1CCR2 CCIFG            | TA1CCR2 CCIFG            |
| 5       | TA2CCR0 CCIFG            | TA2CCR0 CCIFG            | TA2CCR0 CCIFG            |
| 6       | TA2CCR2 CCIFG            | TA2CCR2 CCIFG            | TA2CCR2 CCIFG            |
| 7       | TB0CCR0 CCIFG            | TB0CCR0 CCIFG            | TB0CCR0 CCIFG            |
| 8       | TB0CCR2 CCIFG            | TB0CCR2 CCIFG            | TB0CCR2 CCIFG            |
| 9       | Reserved                 | Reserved                 | Reserved                 |
| 10      | Reserved                 | Reserved                 | Reserved                 |
| 11      | Reserved                 | Reserved                 | Reserved                 |
| 12      | Reserved                 | Reserved                 | Reserved                 |
| 13      | Reserved                 | Reserved                 | Reserved                 |
| 14      | Reserved                 | Reserved                 | Reserved                 |
| 15      | Reserved                 | Reserved                 | Reserved                 |
| 16      | UCA0RXIFG                | UCA0RXIFG                | UCA0RXIFG                |
| 17      | UCA0TXIFG                | UCA0TXIFG                | UCA0TXIFG                |
| 18      | UCB0RXIFG                | UCB0RXIFG                | UCB0RXIFG                |
| 19      | UCB0TXIFG                | UCB0TXIFG                | UCB0TXIFG                |
| 20      | UCA1RXIFG                | UCA1RXIFG                | UCA1RXIFG                |
| 21      | UCA1TXIFG                | UCA1TXIFG                | UCA1TXIFG                |
| 22      | UCB1RXIFG                | UCB1RXIFG                | UCB1RXIFG                |
| 23      | UCB1TXIFG                | UCB1TXIFG                | UCB1TXIFG                |
| 24      | ADC10IFG0 <sup>(2)</sup> | ADC10IFG0 <sup>(2)</sup> | ADC10IFG0 <sup>(2)</sup> |
| 25      | Reserved                 | Reserved                 | Reserved                 |
| 26      | Reserved                 | Reserved                 | Reserved                 |
| 27      | Reserved                 | Reserved                 | Reserved                 |
| 28      | Reserved                 | Reserved                 | Reserved                 |
| 29      | MPY ready                | MPY ready                | MPY ready                |
| 30      | DMA2IFG                  | DMA0IFG                  | DMA1IFG                  |
| 31      | DMAE0                    | DMAE0                    | DMAE0                    |

(1) If a reserved trigger source is selected, no trigger is generated.

(2) Only on devices with ADC; reserved on devices without ADC

**Universal Serial Communication Interface (USCI) (Links to user's guide: [UART Mode](#), [SPI Mode](#), [I2C Mode](#))**

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I<sup>2</sup>C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI\_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI\_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430F522x and MSP430F521x series include two complete USCI modules (n = 0, 1).

## TA0 [\(Link to user's guide\)](#)

TA0 is a 16-bit timer/counter (Timer\_A type) with five capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 15. TA0 Signal Connections**

| INPUT PIN NUMBER    |         | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER                      |                                        |
|---------------------|---------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|----------------------------------------|----------------------------------------|
| RGC, ZQE,<br>YFF    | RGZ     |                           |                           |                 |                            |                            | RGC, ZQE, YFF                          | RGZ                                    |
| 18, H2, G2-<br>P1.0 | 13-P1.0 | TA0CLK                    | TACLK                     | Timer           | NA                         | NA                         |                                        |                                        |
|                     |         | ACLK<br>(internal)        | ACLK                      |                 |                            |                            |                                        |                                        |
|                     |         | SMCLK<br>(internal)       | SMCLK                     |                 |                            |                            |                                        |                                        |
| 18, H2, G2-<br>P1.0 | 13-P1.0 | TA0CLK                    | $\overline{\text{TACLK}}$ |                 |                            |                            |                                        |                                        |
| 19, H3, G3-<br>P1.1 | 14-P1.1 | TA0.0                     | CCI0A                     | CCR0            | TA0                        | TA0.0                      | 19, H3, G3-P1.1                        | 14-P1.1                                |
|                     |         | DVSS                      | CCI0B                     |                 |                            |                            |                                        |                                        |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                                        |                                        |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                        |                                        |
| 20, J3, H3-<br>P1.2 | 15-P1.2 | TA0.1                     | CCI1A                     | CCR1            | TA1                        | TA0.1                      | 20, J3, H3-P1.2                        | 15-P1.2                                |
|                     |         | CBOUT<br>(internal)       | CCI1B                     |                 |                            |                            | ADC10 (internal)<br>ADC10SHSx =<br>{1} | ADC10 (internal)<br>ADC10SHSx =<br>{1} |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                                        |                                        |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                        |                                        |
| 21, G4, F3-<br>P1.3 | 16-P1.3 | TA0.2                     | CCI2A                     | CCR2            | TA2                        | TA0.2                      | 21, G4, F3-P1.3                        | 16-P1.3                                |
|                     |         | ACLK<br>(internal)        | CCI2B                     |                 |                            |                            |                                        |                                        |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                                        |                                        |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                        |                                        |
| 22, H4, E3-<br>P1.4 | 17-P1.4 | TA0.3                     | CCI3A                     | CCR3            | TA3                        | TA0.3                      | 22, H4, E3-P1.4                        | 17-P1.4                                |
|                     |         | DVSS                      | CCI3B                     |                 |                            |                            |                                        |                                        |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                                        |                                        |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                        |                                        |
| 23, J4, H4-<br>P1.5 | 18-P1.5 | TA0.4                     | CCI4A                     | CCR4            | TA4                        | TA0.4                      | 23, J4, H4-P1.5                        | 18-P1.5                                |
|                     |         | DVSS                      | CCI4B                     |                 |                            |                            |                                        |                                        |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                                        |                                        |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                        |                                        |



## TA1 [\(Link to user's guide\)](#)

TA1 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 16. TA1 Signal Connections**

| INPUT PIN NUMBER    |         | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER   |         |
|---------------------|---------|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|---------------------|---------|
| RGC, ZQE,<br>YFF    | RGZ     |                           |                           |                 |                            |                            | RGC, ZQE,<br>YFF    | RGZ     |
| 24, G5, G4-<br>P1.6 | 19-P1.6 | TA1CLK                    | TACLK                     | Timer           | NA                         | NA                         |                     |         |
|                     |         | ACLK<br>(internal)        | ACLK                      |                 |                            |                            |                     |         |
|                     |         | SMCLK<br>(internal)       | SMCLK                     |                 |                            |                            |                     |         |
| 24, G5, G4-<br>P1.6 | 19-P1.6 | TA1CLK                    | $\overline{\text{TACLK}}$ |                 |                            |                            |                     |         |
| 25, H5, F4-<br>P1.7 | 20-P1.7 | TA1.0                     | CCI0A                     | CCR0            | TA0                        | TA1.0                      | 25, H5, F4-<br>P1.7 | 20-P1.7 |
|                     |         | DVSS                      | CCI0B                     |                 |                            |                            |                     |         |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                     |         |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |         |
| 26, J5, H5-<br>P2.0 |         | TA1.1                     | CCI1A                     | CCR1            | TA1                        | TA1.1                      | 26, J5, H5-<br>P2.0 |         |
|                     |         | CBOUT<br>(internal)       | CCI1B                     |                 |                            |                            |                     |         |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                     |         |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |         |
| 27, G6, E4-<br>P2.1 |         | TA1.2                     | CCI2A                     | CCR2            | TA2                        | TA1.2                      | 27, G6, E4-<br>P2.1 |         |
|                     |         | ACLK<br>(internal)        | CCI2B                     |                 |                            |                            |                     |         |
|                     |         | DVSS                      | GND                       |                 |                            |                            |                     |         |
|                     |         | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |         |

## TA2 [\(Link to user's guide\)](#)

TA2 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 17. TA2 Signal Connections**

| INPUT PIN NUMBER    |     | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER   |     |
|---------------------|-----|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|---------------------|-----|
| RGC, ZQE,<br>YFF    | RGZ |                           |                           |                 |                            |                            | RGC, ZQE,<br>YFF    | RGZ |
| 28, J6, G5-<br>P2.2 |     | TA2CLK                    | TACLK                     | Timer           | NA                         | NA                         |                     |     |
|                     |     | ACLK<br>(internal)        | ACLK                      |                 |                            |                            |                     |     |
|                     |     | SMCLK<br>(internal)       | SMCLK                     |                 |                            |                            |                     |     |
| 28, J6, G5-<br>P2.2 |     | TA2CLK                    | $\overline{\text{TACLK}}$ |                 |                            |                            |                     |     |
| 29, H6, H6-<br>P2.3 |     | TA2.0                     | CCI0A                     | CCR0            | TA0                        | TA2.0                      | 29, H6, H6-<br>P2.3 |     |
|                     |     | DVSS                      | CCI0B                     |                 |                            |                            |                     |     |
|                     |     | DVSS                      | GND                       |                 |                            |                            |                     |     |
|                     |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |     |
| 30, J7, F5-<br>P2.4 |     | TA2.1                     | CCI1A                     | CCR1            | TA1                        | TA2.1                      | 30, J7, F5-<br>P2.4 |     |
|                     |     | CBOUT<br>(internal)       | CCI1B                     |                 |                            |                            |                     |     |
|                     |     | DVSS                      | GND                       |                 |                            |                            |                     |     |
|                     |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |     |
| 31, J8, G6-<br>P2.5 |     | TA2.2                     | CCI2A                     | CCR2            | TA2                        | TA2.2                      | 31, J8, G6-<br>P2.5 |     |
|                     |     | ACLK<br>(internal)        | CCI2B                     |                 |                            |                            |                     |     |
|                     |     | DVSS                      | GND                       |                 |                            |                            |                     |     |
|                     |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                     |     |

**TB0 (Link to user's guide)**

TB0 is a 16-bit timer/counter (Timer\_B type) with seven capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 18. TB0 Signal Connections**

| INPUT PIN NUMBER                      |     | DEVICE<br>INPUT<br>SIGNAL | MODULE<br>INPUT<br>SIGNAL | MODULE<br>BLOCK | MODULE<br>OUTPUT<br>SIGNAL | DEVICE<br>OUTPUT<br>SIGNAL | OUTPUT PIN NUMBER                     |                                     |
|---------------------------------------|-----|---------------------------|---------------------------|-----------------|----------------------------|----------------------------|---------------------------------------|-------------------------------------|
| RGC, ZQE,<br>YFF                      | RGZ |                           |                           |                 |                            |                            | RGC, ZQE, YFF                         | RGZ                                 |
| (1)                                   | (1) | TB0CLK                    | TBCLK                     | Timer           | NA                         | NA                         |                                       |                                     |
|                                       |     | ACLK<br>(internal)        | ACLK                      |                 |                            |                            |                                       |                                     |
|                                       |     | SMCLK<br>(internal)       | SMCLK                     |                 |                            |                            |                                       |                                     |
| (1)                                   | (1) | TB0CLK                    | $\overline{\text{TBCLK}}$ |                 |                            |                            |                                       |                                     |
| 49, B8(9), A8-<br>P7.0 <sup>(1)</sup> | (1) | TB0.0                     | CCI0A                     | CCR0            | TB0                        | TB0.0                      | 49, B8(9), A8-<br>P7.0 <sup>(1)</sup> | (1)                                 |
| 49, B8(9), A8-<br>P7.0 <sup>(1)</sup> | (1) | TB0.0                     | CCI0B                     |                 |                            |                            | ADC10 (internal)<br>ADC10SHSx = {2}   | ADC10 (internal)<br>ADC10SHSx = {2} |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| 50, A9, C6-<br>P7.1 <sup>(1)</sup>    | (1) | TB0.1                     | CCI1A                     | CCR1            | TB1                        | TB0.1                      | 50, A9, C6-P7.1 <sup>(1)</sup>        | (1)                                 |
|                                       |     | CBOUT<br>(internal)       | CCI1B                     |                 |                            |                            | ADC10 (internal)<br>ADC10SHSx = {3}   | ADC10 (internal)<br>ADC10SHSx = {3} |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| 51, B7, B7-<br>P7.2 <sup>(1)</sup>    | (1) | TB0.2                     | CCI2A                     | CCR2            | TB2                        | TB0.2                      | 51, B7, B7-P7.2 <sup>(1)</sup>        | (1)                                 |
| 51, B7, B7-<br>P7.2 <sup>(1)</sup>    | (1) | TB0.2                     | CCI2B                     |                 |                            |                            |                                       |                                     |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| 52, A8, B6-<br>P7.3 <sup>(1)</sup>    | (1) | TB0.3                     | CCI3A                     | CCR3            | TB3                        | TB0.3                      | 52, A8, B6-P7.3 <sup>(1)</sup>        | (1)                                 |
| 52, A8, B6-<br>P7.3 <sup>(1)</sup>    | (1) | TB0.3                     | CCI3B                     |                 |                            |                            |                                       |                                     |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| 53, A7, A7-<br>P7.4 <sup>(1)</sup>    | (1) | TB0.4                     | CCI4A                     | CCR4            | TB4                        | TB0.4                      | 53, A7, A7-P7.4 <sup>(1)</sup>        | (1)                                 |
| 53, A7, A7-<br>P7.4 <sup>(1)</sup>    | (1) | TB0.4                     | CCI4B                     |                 |                            |                            |                                       |                                     |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| 54, A6, D5-<br>P7.5 <sup>(1)</sup>    | (1) | TB0.5                     | CCI5A                     | CCR5            | TB5                        | TB0.5                      | 54, A6, D5-P7.5 <sup>(1)</sup>        | (1)                                 |
| 54, A6, D5-<br>P7.5 <sup>(1)</sup>    | (1) | TB0.5                     | CCI5B                     |                 |                            |                            |                                       |                                     |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |
| (1)                                   | (1) | TB0.6                     | CCI6A                     | CCR6            | TB6                        | TB0.6                      | (1)                                   | (1)                                 |
|                                       |     | ACLK<br>(internal)        | CCI6B                     |                 |                            |                            |                                       |                                     |
|                                       |     | DVSS                      | GND                       |                 |                            |                            |                                       |                                     |
|                                       |     | DVCC                      | V <sub>CC</sub>           |                 |                            |                            |                                       |                                     |

(1) Timer functions available via the port mapping controller.

### **Comparator\_B ([Link to user's guide](#))**

The primary function of the Comparator\_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### **ADC10\_A ([Link to user's guide](#))**

The ADC10\_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

### **CRC16 ([Link to user's guide](#))**

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### **REF Voltage Reference ([Link to user's guide](#))**

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

### **Embedded Emulation Module (EEM) (S Version) ([Link to user's guide](#))**

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

## Peripheral File Map

**Table 19. Peripherals**

| MODULE NAME                                                | BASE ADDRESS | OFFSET ADDRESS RANGE |
|------------------------------------------------------------|--------------|----------------------|
| Special Functions (see <a href="#">Table 20</a> )          | 0100h        | 000h-01Fh            |
| PMM (see <a href="#">Table 21</a> )                        | 0120h        | 000h-010h            |
| Flash Control (see <a href="#">Table 22</a> )              | 0140h        | 000h-00Fh            |
| CRC16 (see <a href="#">Table 23</a> )                      | 0150h        | 000h-007h            |
| RAM Control (see <a href="#">Table 24</a> )                | 0158h        | 000h-001h            |
| Watchdog (see <a href="#">Table 25</a> )                   | 015Ch        | 000h-001h            |
| UCS (see <a href="#">Table 26</a> )                        | 0160h        | 000h-01Fh            |
| SYS (see <a href="#">Table 27</a> )                        | 0180h        | 000h-01Fh            |
| Shared Reference (see <a href="#">Table 28</a> )           | 01B0h        | 000h-001h            |
| Port Mapping Control (see <a href="#">Table 29</a> )       | 01C0h        | 000h-002h            |
| Port Mapping Port P4 (see <a href="#">Table 29</a> )       | 01E0h        | 000h-007h            |
| Port P1, P2 (see <a href="#">Table 30</a> )                | 0200h        | 000h-01Fh            |
| Port P3, P4 (see <a href="#">Table 31</a> )                | 0220h        | 000h-00Bh            |
| Port P5, P6 (see <a href="#">Table 32</a> )                | 0240h        | 000h-00Bh            |
| Port P7 (see <a href="#">Table 33</a> )                    | 0260h        | 000h-00Bh            |
| Port PJ (see <a href="#">Table 34</a> )                    | 0320h        | 000h-01Fh            |
| TA0 (see <a href="#">Table 35</a> )                        | 0340h        | 000h-02Eh            |
| TA1 (see <a href="#">Table 36</a> )                        | 0380h        | 000h-02Eh            |
| TB0 (see <a href="#">Table 37</a> )                        | 03C0h        | 000h-02Eh            |
| TA2 (see <a href="#">Table 38</a> )                        | 0400h        | 000h-02Eh            |
| Real-Time Clock (RTC_A) (see <a href="#">Table 39</a> )    | 04A0h        | 000h-01Bh            |
| 32-Bit Hardware Multiplier (see <a href="#">Table 40</a> ) | 04C0h        | 000h-02Fh            |
| DMA General Control (see <a href="#">Table 41</a> )        | 0500h        | 000h-00Fh            |
| DMA Channel 0 (see <a href="#">Table 41</a> )              | 0510h        | 000h-00Ah            |
| DMA Channel 1 (see <a href="#">Table 41</a> )              | 0520h        | 000h-00Ah            |
| DMA Channel 2 (see <a href="#">Table 41</a> )              | 0530h        | 000h-00Ah            |
| USCI_A0 (see <a href="#">Table 42</a> )                    | 05C0h        | 000h-01Fh            |
| USCI_B0 (see <a href="#">Table 43</a> )                    | 05E0h        | 000h-01Fh            |
| USCI_A1 (see <a href="#">Table 44</a> )                    | 0600h        | 000h-01Fh            |
| USCI_B1 (see <a href="#">Table 45</a> )                    | 0620h        | 000h-01Fh            |
| ADC10_A (see <a href="#">Table 46</a> )                    | 0740h        | 000h-01Fh            |
| Comparator_B (see <a href="#">Table 47</a> )               | 08C0h        | 000h-00Fh            |

**Table 20. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION  | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable  | SFRIE1   | 00h    |
| SFR interrupt flag    | SFRIFG1  | 02h    |
| SFR reset pin control | SFRRPCR  | 04h    |

**Table 21. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM Control 0            | PMMCTL0  | 00h    |
| PMM control 1            | PMMCTL1  | 02h    |
| SVS high side control    | SVSMHCTL | 04h    |
| SVS low side control     | SVSMLCTL | 06h    |
| PMM interrupt flags      | PMMIFG   | 0Ch    |
| PMM interrupt enable     | PMMIE    | 0Eh    |
| PMM power mode 5 control | PM5CTL0  | 10h    |

**Table 22. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1      | FCTL1    | 00h    |
| Flash control 3      | FCTL3    | 04h    |
| Flash control 4      | FCTL4    | 06h    |

**Table 23. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input                | CRC16DI   | 00h    |
| CRC data input reverse byte   | CRCDIRB   | 02h    |
| CRC initialization and result | CRCINIRES | 04h    |
| CRC result reverse byte       | CRCRESR   | 06h    |

**Table 24. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0        | RCCTL0   | 00h    |

**Table 25. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION   | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL   | 00h    |

**Table 26. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0        | UCSCTL0  | 00h    |
| UCS control 1        | UCSCTL1  | 02h    |
| UCS control 2        | UCSCTL2  | 04h    |
| UCS control 3        | UCSCTL3  | 06h    |
| UCS control 4        | UCSCTL4  | 08h    |
| UCS control 5        | UCSCTL5  | 0Ah    |
| UCS control 6        | UCSCTL6  | 0Ch    |
| UCS control 7        | UCSCTL7  | 0Eh    |
| UCS control 8        | UCSCTL8  | 10h    |
| UCS control 9        | UCSCTL9  | 12h    |

**Table 27. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION                | REGISTER | OFFSET |
|-------------------------------------|----------|--------|
| System control                      | SYSCTL   | 00h    |
| Bootstrap loader configuration area | SYSBSLC  | 02h    |
| JTAG mailbox control                | SYSJMBC  | 06h    |
| JTAG mailbox input 0                | SYSJMBI0 | 08h    |
| JTAG mailbox input 1                | SYSJMBI1 | 0Ah    |
| JTAG mailbox output 0               | SYSJMBO0 | 0Ch    |
| JTAG mailbox output 1               | SYSJMBO1 | 0Eh    |
| User NMI vector generator           | SYSUNIV  | 1Ah    |
| System NMI vector generator         | SYSSNIV  | 1Ch    |
| Reset vector generator              | SYSRSTIV | 1Eh    |

**Table 28. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION     | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL   | 00h    |

**Table 29. Port Mapping Registers  
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

| REGISTER DESCRIPTION          | REGISTER  | OFFSET |
|-------------------------------|-----------|--------|
| Port mapping key/ID register  | PMAPKEYID | 00h    |
| Port mapping control register | PMAPCTL   | 02h    |
| Port P4.0 mapping register    | P4MAP0    | 00h    |
| Port P4.1 mapping register    | P4MAP1    | 01h    |
| Port P4.2 mapping register    | P4MAP2    | 02h    |
| Port P4.3 mapping register    | P4MAP3    | 03h    |
| Port P4.4 mapping register    | P4MAP4    | 04h    |
| Port P4.5 mapping register    | P4MAP5    | 05h    |
| Port P4.6 mapping register    | P4MAP6    | 06h    |
| Port P4.7 mapping register    | P4MAP7    | 07h    |

**Table 30. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION              | REGISTER | OFFSET |
|-----------------------------------|----------|--------|
| Port P1 input                     | P1IN     | 00h    |
| Port P1 output                    | P1OUT    | 02h    |
| Port P1 direction                 | P1DIR    | 04h    |
| Port P1 pullup or pulldown enable | P1REN    | 06h    |
| Port P1 drive strength            | P1DS     | 08h    |
| Port P1 selection                 | P1SEL    | 0Ah    |
| Port P1 interrupt vector word     | P1IV     | 0Eh    |
| Port P1 interrupt edge select     | P1IES    | 18h    |
| Port P1 interrupt enable          | P1IE     | 1Ah    |
| Port P1 interrupt flag            | P1IFG    | 1Ch    |
| Port P2 input                     | P2IN     | 01h    |
| Port P2 output                    | P2OUT    | 03h    |
| Port P2 direction                 | P2DIR    | 05h    |
| Port P2 pullup or pulldown enable | P2REN    | 07h    |
| Port P2 drive strength            | P2DS     | 09h    |
| Port P2 selection                 | P2SEL    | 0Bh    |

**Table 30. Port P1, P2 Registers (Base Address: 0200h) (continued)**

| REGISTER DESCRIPTION          | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P2 interrupt vector word | P2IV     | 1Eh    |
| Port P2 interrupt edge select | P2IES    | 19h    |
| Port P2 interrupt enable      | P2IE     | 1Bh    |
| Port P2 interrupt flag        | P2IFG    | 1Dh    |

**Table 31. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION              | REGISTER | OFFSET |
|-----------------------------------|----------|--------|
| Port P3 input                     | P3IN     | 00h    |
| Port P3 output                    | P3OUT    | 02h    |
| Port P3 direction                 | P3DIR    | 04h    |
| Port P3 pullup or pulldown enable | P3REN    | 06h    |
| Port P3 drive strength            | P3DS     | 08h    |
| Port P3 selection                 | P3SEL    | 0Ah    |
| Port P4 input                     | P4IN     | 01h    |
| Port P4 output                    | P4OUT    | 03h    |
| Port P4 direction                 | P4DIR    | 05h    |
| Port P4 pullup or pulldown enable | P4REN    | 07h    |
| Port P4 drive strength            | P4DS     | 09h    |
| Port P4 selection                 | P4SEL    | 0Bh    |

**Table 32. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION              | REGISTER | OFFSET |
|-----------------------------------|----------|--------|
| Port P5 input                     | P5IN     | 00h    |
| Port P5 output                    | P5OUT    | 02h    |
| Port P5 direction                 | P5DIR    | 04h    |
| Port P5 pullup or pulldown enable | P5REN    | 06h    |
| Port P5 drive strength            | P5DS     | 08h    |
| Port P5 selection                 | P5SEL    | 0Ah    |
| Port P6 input                     | P6IN     | 01h    |
| Port P6 output                    | P6OUT    | 03h    |
| Port P6 direction                 | P6DIR    | 05h    |
| Port P6 pullup or pulldown enable | P6REN    | 07h    |
| Port P6 drive strength            | P6DS     | 09h    |
| Port P6 selection                 | P6SEL    | 0Bh    |

**Table 33. Port P7 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION              | REGISTER | OFFSET |
|-----------------------------------|----------|--------|
| Port P7 input                     | P7IN     | 00h    |
| Port P7 output                    | P7OUT    | 02h    |
| Port P7 direction                 | P7DIR    | 04h    |
| Port P7 pullup or pulldown enable | P7REN    | 06h    |
| Port P7 drive strength            | P7DS     | 08h    |
| Port P7 selection                 | P7SEL    | 0Ah    |



**Table 34. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION              | REGISTER | OFFSET |
|-----------------------------------|----------|--------|
| Port PJ input                     | PJIN     | 00h    |
| Port PJ output                    | PJOUT    | 02h    |
| Port PJ direction                 | PJDIR    | 04h    |
| Port PJ pullup or pulldown enable | PJREN    | 06h    |
| Port PJ drive strength            | PJDS     | 08h    |

**Table 35. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control                | TA0CTL   | 00h    |
| Capture/compare control 0  | TA0CCTL0 | 02h    |
| Capture/compare control 1  | TA0CCTL1 | 04h    |
| Capture/compare control 2  | TA0CCTL2 | 06h    |
| Capture/compare control 3  | TA0CCTL3 | 08h    |
| Capture/compare control 4  | TA0CCTL4 | 0Ah    |
| TA0 counter register       | TA0R     | 10h    |
| Capture/compare register 0 | TA0CCR0  | 12h    |
| Capture/compare register 1 | TA0CCR1  | 14h    |
| Capture/compare register 2 | TA0CCR2  | 16h    |
| Capture/compare register 3 | TA0CCR3  | 18h    |
| Capture/compare register 4 | TA0CCR4  | 1Ah    |
| TA0 expansion register 0   | TA0EX0   | 20h    |
| TA0 interrupt vector       | TA0IV    | 2Eh    |

**Table 36. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 control                | TA1CTL   | 00h    |
| Capture/compare control 0  | TA1CCTL0 | 02h    |
| Capture/compare control 1  | TA1CCTL1 | 04h    |
| Capture/compare control 2  | TA1CCTL2 | 06h    |
| TA1 counter register       | TA1R     | 10h    |
| Capture/compare register 0 | TA1CCR0  | 12h    |
| Capture/compare register 1 | TA1CCR1  | 14h    |
| Capture/compare register 2 | TA1CCR2  | 16h    |
| TA1 expansion register 0   | TA1EX0   | 20h    |
| TA1 interrupt vector       | TA1IV    | 2Eh    |

**Table 37. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION      | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control               | TB0CTL   | 00h    |
| Capture/compare control 0 | TB0CCTL0 | 02h    |
| Capture/compare control 1 | TB0CCTL1 | 04h    |
| Capture/compare control 2 | TB0CCTL2 | 06h    |
| Capture/compare control 3 | TB0CCTL3 | 08h    |
| Capture/compare control 4 | TB0CCTL4 | 0Ah    |
| Capture/compare control 5 | TB0CCTL5 | 0Ch    |
| Capture/compare control 6 | TB0CCTL6 | 0Eh    |
| TB0 register              | TB0R     | 10h    |

**Table 37. TB0 Registers (Base Address: 03C0h) (continued)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| Capture/compare register 0 | TB0CCR0  | 12h    |
| Capture/compare register 1 | TB0CCR1  | 14h    |
| Capture/compare register 2 | TB0CCR2  | 16h    |
| Capture/compare register 3 | TB0CCR3  | 18h    |
| Capture/compare register 4 | TB0CCR4  | 1Ah    |
| Capture/compare register 5 | TB0CCR5  | 1Ch    |
| Capture/compare register 6 | TB0CCR6  | 1Eh    |
| TB0 expansion register 0   | TB0EX0   | 20h    |
| TB0 interrupt vector       | TB0IV    | 2Eh    |

**Table 38. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION       | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA2 control                | TA2CTL   | 00h    |
| Capture/compare control 0  | TA2CCTL0 | 02h    |
| Capture/compare control 1  | TA2CCTL1 | 04h    |
| Capture/compare control 2  | TA2CCTL2 | 06h    |
| TA2 counter register       | TA2R     | 10h    |
| Capture/compare register 0 | TA2CCR0  | 12h    |
| Capture/compare register 1 | TA2CCR1  | 14h    |
| Capture/compare register 2 | TA2CCR2  | 16h    |
| TA2 expansion register 0   | TA2EX0   | 20h    |
| TA2 interrupt vector       | TA2IV    | 2Eh    |

**Table 39. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION               | REGISTER       | OFFSET |
|------------------------------------|----------------|--------|
| RTC control 0                      | RTCCTL0        | 00h    |
| RTC control 1                      | RTCCTL1        | 01h    |
| RTC control 2                      | RTCCTL2        | 02h    |
| RTC control 3                      | RTCCTL3        | 03h    |
| RTC prescaler 0 control            | RTCPS0CTL      | 08h    |
| RTC prescaler 1 control            | RTCPS1CTL      | 0Ah    |
| RTC prescaler 0                    | RTCPS0         | 0Ch    |
| RTC prescaler 1                    | RTCPS1         | 0Dh    |
| RTC interrupt vector word          | RTCIV          | 0Eh    |
| RTC seconds/counter register 1     | RTCSEC/RTCNT1  | 10h    |
| RTC minutes/counter register 2     | RTCMIN/RTCNT2  | 11h    |
| RTC hours/counter register 3       | RTCHOUR/RTCNT3 | 12h    |
| RTC day of week/counter register 4 | RTCDOW/RTCNT4  | 13h    |
| RTC days                           | RTCDAY         | 14h    |
| RTC month                          | RTCMON         | 15h    |
| RTC year low                       | RTCYEARL       | 16h    |
| RTC year high                      | RTCYEARH       | 17h    |
| RTC alarm minutes                  | RTCAMIN        | 18h    |
| RTC alarm hours                    | RTCAHOUR       | 19h    |
| RTC alarm day of week              | RTCADOW        | 1Ah    |
| RTC alarm days                     | RTCADAY        | 1Bh    |

**Table 40. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION                                    | REGISTER  | OFFSET |
|---------------------------------------------------------|-----------|--------|
| 16-bit operand 1 – multiply                             | MPY       | 00h    |
| 16-bit operand 1 – signed multiply                      | MPYS      | 02h    |
| 16-bit operand 1 – multiply accumulate                  | MAC       | 04h    |
| 16-bit operand 1 – signed multiply accumulate           | MACS      | 06h    |
| 16-bit operand 2                                        | OP2       | 08h    |
| 16 × 16 result low word                                 | RESLO     | 0Ah    |
| 16 × 16 result high word                                | RESHI     | 0Ch    |
| 16 × 16 sum extension register                          | SUMEXT    | 0Eh    |
| 32-bit operand 1 – multiply low word                    | MPY32L    | 10h    |
| 32-bit operand 1 – multiply high word                   | MPY32H    | 12h    |
| 32-bit operand 1 – signed multiply low word             | MPYS32L   | 14h    |
| 32-bit operand 1 – signed multiply high word            | MPYS32H   | 16h    |
| 32-bit operand 1 – multiply accumulate low word         | MAC32L    | 18h    |
| 32-bit operand 1 – multiply accumulate high word        | MAC32H    | 1Ah    |
| 32-bit operand 1 – signed multiply accumulate low word  | MACS32L   | 1Ch    |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H   | 1Eh    |
| 32-bit operand 2 – low word                             | OP2L      | 20h    |
| 32-bit operand 2 – high word                            | OP2H      | 22h    |
| 32 × 32 result 0 – least significant word               | RES0      | 24h    |
| 32 × 32 result 1                                        | RES1      | 26h    |
| 32 × 32 result 2                                        | RES2      | 28h    |
| 32 × 32 result 3 – most significant word                | RES3      | 2Ah    |
| MPY32 control register 0                                | MPY32CTL0 | 2Ch    |

**Table 41. DMA Registers (Base Address DMA General Control: 0500h,  
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION                   | REGISTER | OFFSET |
|----------------------------------------|----------|--------|
| DMA channel 0 control                  | DMA0CTL  | 00h    |
| DMA channel 0 source address low       | DMA0SAL  | 02h    |
| DMA channel 0 source address high      | DMA0SAH  | 04h    |
| DMA channel 0 destination address low  | DMA0DAL  | 06h    |
| DMA channel 0 destination address high | DMA0DAH  | 08h    |
| DMA channel 0 transfer size            | DMA0SZ   | 0Ah    |
| DMA channel 1 control                  | DMA1CTL  | 00h    |
| DMA channel 1 source address low       | DMA1SAL  | 02h    |
| DMA channel 1 source address high      | DMA1SAH  | 04h    |
| DMA channel 1 destination address low  | DMA1DAL  | 06h    |
| DMA channel 1 destination address high | DMA1DAH  | 08h    |
| DMA channel 1 transfer size            | DMA1SZ   | 0Ah    |
| DMA channel 2 control                  | DMA2CTL  | 00h    |
| DMA channel 2 source address low       | DMA2SAL  | 02h    |
| DMA channel 2 source address high      | DMA2SAH  | 04h    |
| DMA channel 2 destination address low  | DMA2DAL  | 06h    |
| DMA channel 2 destination address high | DMA2DAH  | 08h    |
| DMA channel 2 transfer size            | DMA2SZ   | 0Ah    |
| DMA module control 0                   | DMACTL0  | 00h    |
| DMA module control 1                   | DMACTL1  | 02h    |

**Table 41. DMA Registers (Base Address DMA General Control: 0500h,  
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 2 | DMACTL2  | 04h    |
| DMA module control 3 | DMACTL3  | 06h    |
| DMA module control 4 | DMACTL4  | 08h    |
| DMA interrupt vector | DMAIV    | 0Eh    |

**Table 42. USCI\_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI control 1             | UCA0CTL1   | 00h    |
| USCI control 0             | UCA0CTL0   | 01h    |
| USCI baud rate 0           | UCA0BR0    | 06h    |
| USCI baud rate 1           | UCA0BR1    | 07h    |
| USCI modulation control    | UCA0MCTL   | 08h    |
| USCI status                | UCA0STAT   | 0Ah    |
| USCI receive buffer        | UCA0RXBUF  | 0Ch    |
| USCI transmit buffer       | UCA0TXBUF  | 0Eh    |
| USCI LIN control           | UCA0ABCTL  | 10h    |
| USCI IrDA transmit control | UCA0IRTCTL | 12h    |
| USCI IrDA receive control  | UCA0IRRCTL | 13h    |
| USCI interrupt enable      | UCA0IE     | 1Ch    |
| USCI interrupt flags       | UCA0IFG    | 1Dh    |
| USCI interrupt vector word | UCA0IV     | 1Eh    |

**Table 43. USCI\_B0 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1       | UCB0CTL1  | 00h    |
| USCI synchronous control 0       | UCB0CTL0  | 01h    |
| USCI synchronous bit rate 0      | UCB0BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB0BR1   | 07h    |
| USCI synchronous status          | UCB0STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB0RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh    |
| USCI I2C own address             | UCB0I2COA | 10h    |
| USCI I2C slave address           | UCB0I2CSA | 12h    |
| USCI interrupt enable            | UCB0IE    | 1Ch    |
| USCI interrupt flags             | UCB0IFG   | 1Dh    |
| USCI interrupt vector word       | UCB0IV    | 1Eh    |

**Table 44. USCI\_A1 Registers (Base Address: 0600h)**

| REGISTER DESCRIPTION    | REGISTER  | OFFSET |
|-------------------------|-----------|--------|
| USCI control 1          | UCA1CTL1  | 00h    |
| USCI control 0          | UCA1CTL0  | 01h    |
| USCI baud rate 0        | UCA1BR0   | 06h    |
| USCI baud rate 1        | UCA1BR1   | 07h    |
| USCI modulation control | UCA1MCTL  | 08h    |
| USCI status             | UCA1STAT  | 0Ah    |
| USCI receive buffer     | UCA1RXBUF | 0Ch    |

**Table 44. USCI\_A1 Registers (Base Address: 0600h) (continued)**

| REGISTER DESCRIPTION       | REGISTER   | OFFSET |
|----------------------------|------------|--------|
| USCI transmit buffer       | UCA1TXBUF  | 0Eh    |
| USCI LIN control           | UCA1ABCTL  | 10h    |
| USCI IrDA transmit control | UCA1IRTCTL | 12h    |
| USCI IrDA receive control  | UCA1IRRCTL | 13h    |
| USCI interrupt enable      | UCA1IE     | 1Ch    |
| USCI interrupt flags       | UCA1IFG    | 1Dh    |
| USCI interrupt vector word | UCA1IV     | 1Eh    |

**Table 45. USCI\_B1 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION             | REGISTER  | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1       | UCB1CTL1  | 00h    |
| USCI synchronous control 0       | UCB1CTL0  | 01h    |
| USCI synchronous bit rate 0      | UCB1BR0   | 06h    |
| USCI synchronous bit rate 1      | UCB1BR1   | 07h    |
| USCI synchronous status          | UCB1STAT  | 0Ah    |
| USCI synchronous receive buffer  | UCB1RXBUF | 0Ch    |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh    |
| USCI I2C own address             | UCB1I2COA | 10h    |
| USCI I2C slave address           | UCB1I2CSA | 12h    |
| USCI interrupt enable            | UCB1IE    | 1Ch    |
| USCI interrupt flags             | UCB1IFG   | 1Dh    |
| USCI interrupt vector word       | UCB1IV    | 1Eh    |

**Table 46. ADC10\_A Registers (Base Address: 0740h)**

| REGISTER DESCRIPTION                     | REGISTER   | OFFSET |
|------------------------------------------|------------|--------|
| ADC10_A Control register 0               | ADC10CTL0  | 00h    |
| ADC10_A Control register 1               | ADC10CTL1  | 02h    |
| ADC10_A Control register 2               | ADC10CTL2  | 04h    |
| ADC10_A Window Comparator Low Threshold  | ADC10LO    | 06h    |
| ADC10_A Window Comparator High Threshold | ADC10HI    | 08h    |
| ADC10_A Memory Control Register 0        | ADC10MCTL0 | 0Ah    |
| ADC10_A Conversion Memory Register       | ADC10MEM0  | 12h    |
| ADC10_A Interrupt Enable                 | ADC10IE    | 1Ah    |
| ADC10_A Interrupt Flags                  | ADC10IGH   | 1Ch    |
| ADC10_A Interrupt Vector Word            | ADC10IV    | 1Eh    |

**Table 47. Comparator\_B Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION         | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control register 0    | CBCTL0   | 00h    |
| Comp_B control register 1    | CBCTL1   | 02h    |
| Comp_B control register 2    | CBCTL2   | 04h    |
| Comp_B control register 3    | CBCTL3   | 06h    |
| Comp_B interrupt register    | CBINT    | 0Ch    |
| Comp_B interrupt vector word | CBIV     | 0Eh    |

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                                   |                            |
|-------------------------------------------------------------------|----------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$                           | -0.3 V to 4.1 V            |
| Voltage applied to any pin (excluding $V_{CORE}$ ) <sup>(2)</sup> | -0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device pin                                   | $\pm 2$ mA                 |
| Storage temperature range, $T_{stg}$ <sup>(3)</sup>               | -55°C to 150°C             |

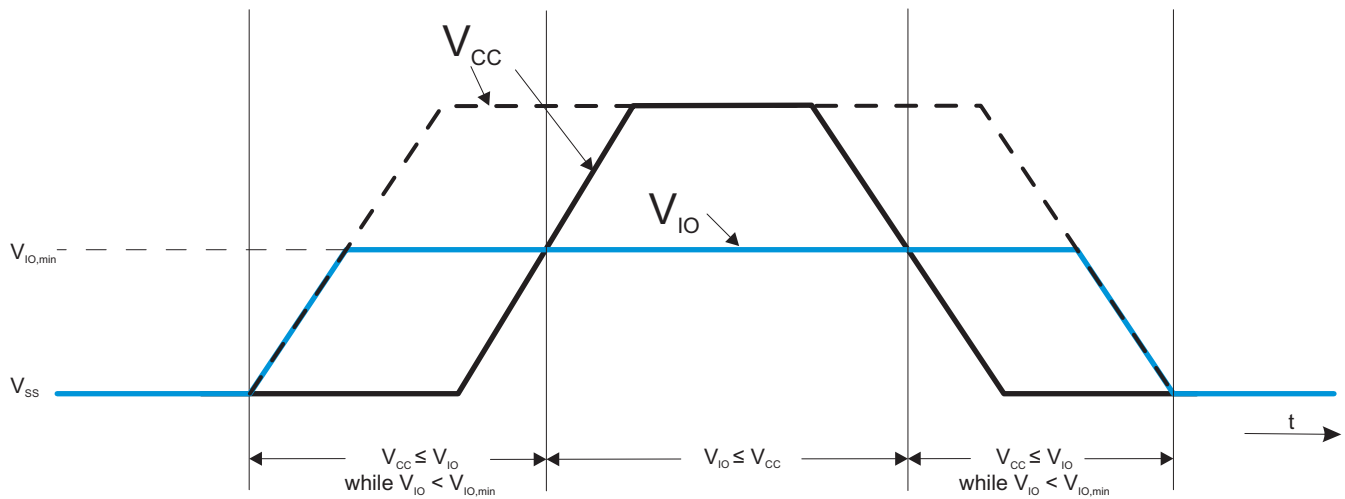
- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ .  $V_{CORE}$  is for internal device use only. No external DC loading or voltage should be applied.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## Recommended Operating Conditions

Typical values are specified at  $V_{CC} = 3.3$  V and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

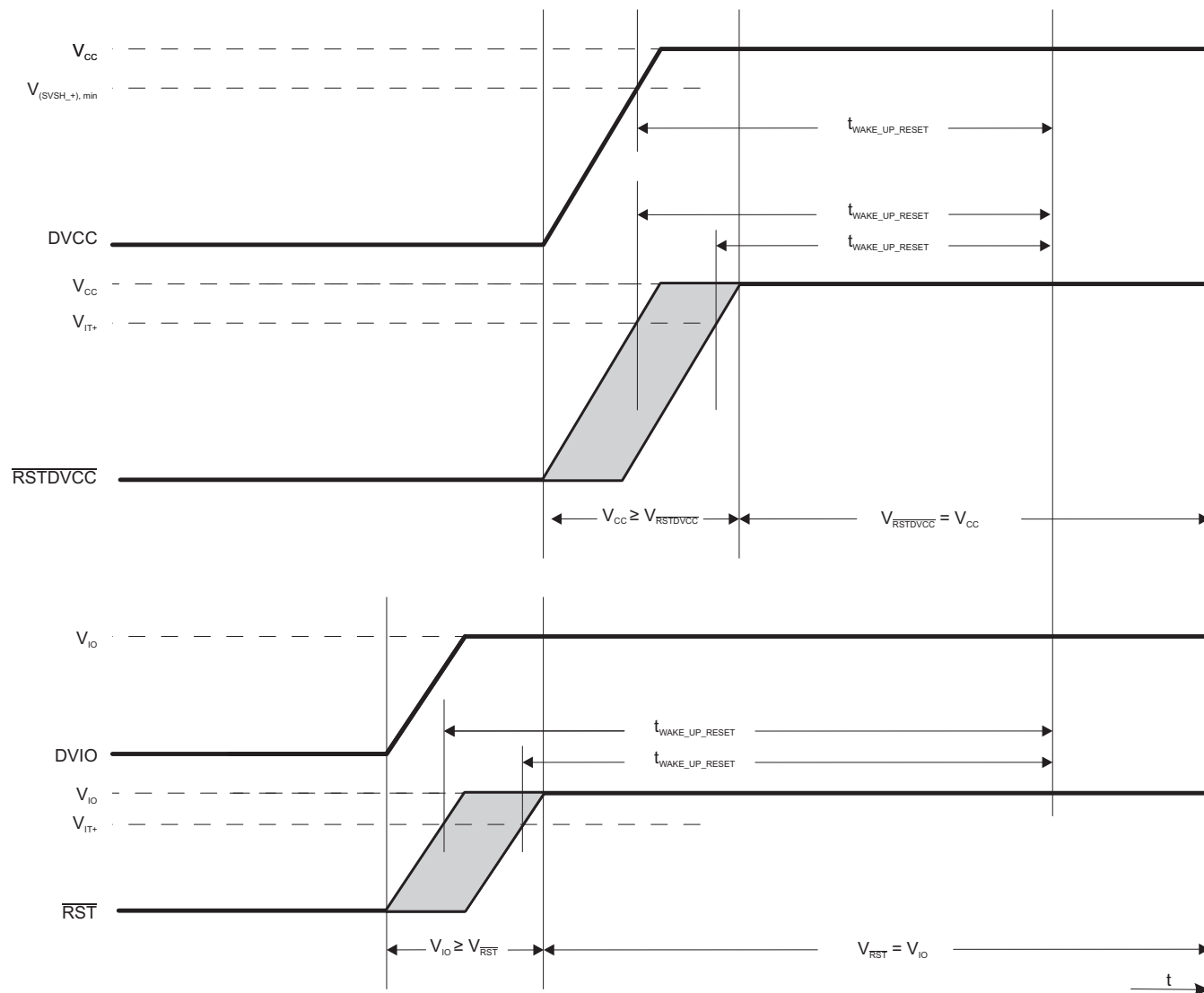
|                            |                                                                                                           | MIN                                                                                | NOM | MAX  | UNIT |
|----------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----|------|------|
| $V_{CC}$                   | Supply voltage during program execution and flash programming( $AV_{CC} = DV_{CC}$ ) <sup>(1)(2)(3)</sup> | PMMCOREVx = 0                                                                      | 1.8 | 3.6  | V    |
|                            |                                                                                                           | PMMCOREVx = 0, 1                                                                   | 2.0 | 3.6  | V    |
|                            |                                                                                                           | PMMCOREVx = 0, 1, 2                                                                | 2.2 | 3.6  | V    |
|                            |                                                                                                           | PMMCOREVx = 0, 1, 2, 3                                                             | 2.4 | 3.6  | V    |
| $V_{IO}$                   | Supply voltage applied to DVIO referenced to $V_{SS}$ <sup>(2)</sup>                                      | 1.62                                                                               |     | 1.98 | V    |
| $V_{SS}$                   | Supply voltage ( $AV_{SS} = DV_{SS}$ )                                                                    |                                                                                    | 0   |      | V    |
| $T_A$                      | Operating free-air temperature                                                                            | I version                                                                          | -40 | 85   | °C   |
| $T_J$                      | Operating junction temperature                                                                            | I version                                                                          | -40 | 85   | °C   |
| $C_{V_{CORE}}$             | Recommended capacitor at $V_{CORE}$                                                                       |                                                                                    | 470 |      | nF   |
| $C_{DV_{CC}}/C_{V_{CORE}}$ | Capacitor ratio of $DV_{CC}$ to $V_{CORE}$                                                                |                                                                                    | 10  |      |      |
| $f_{SYSTEM}$               | Processor frequency (maximum MCLK frequency) <sup>(4)</sup><br>(see <a href="#">Figure 3</a> )            | PMMCOREVx = 0 (default condition),<br>$1.8\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | 0   | 8.0  | MHz  |
|                            |                                                                                                           | PMMCOREVx = 1,<br>$2.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$                     | 0   | 12.0 |      |
|                            |                                                                                                           | PMMCOREVx = 2,<br>$2.2\text{ V} \leq V_{CC} \leq 3.6\text{ V}$                     | 0   | 20.0 |      |
|                            |                                                                                                           | PMMCOREVx = 3,<br>$2.4\text{ V} \leq V_{CC} \leq 3.6\text{ V}$                     | 0   | 25.0 |      |

- (1) It is recommended to power  $AV_{CC}$  and  $DV_{CC}$  from the same source. A maximum difference of 0.3 V between  $AV_{CC}$  and  $DV_{CC}$  can be tolerated during power up and operation.
- (2) During  $V_{CC}$  and  $V_{IO}$  power up, it is required that  $V_{IO} \geq V_{CC}$  during the ramp up phase of  $V_{IO}$ . During  $V_{CC}$  and  $V_{IO}$  power down, it is required that  $V_{IO} \geq V_{CC}$  during the ramp down phase of  $V_{IO}$  (see [Figure 1](#)).
- (3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [PMM, SVS High Side](#) threshold parameters for the exact values and further details.
- (4) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The device supports continuous operation with  $V_{CC} = V_{SS}$  while  $V_{IO}$  is fully within its specification. During this time, the general-purpose I/Os that reside on the  $V_{IO}$  supply domain are configured as inputs and pulled down to  $V_{SS}$  through their internal pulldown resistors.  $\overline{RST}/NMI$  is high impedance.  $BSLEN$  is configured as an input and is pulled down to  $V_{SS}$  through its internal pulldown resistor. When  $V_{CC}$  reaches above the BOR threshold, the general-purpose I/Os become high-impedance inputs (no pullup or pulldown enabled),  $\overline{RST}/NMI$  becomes an input pulled up to  $V_{IO}$  through its internal pullup resistor, and  $BSLEN$  remains pulled down to  $V_{SS}$  through its internal pulldown resistor.

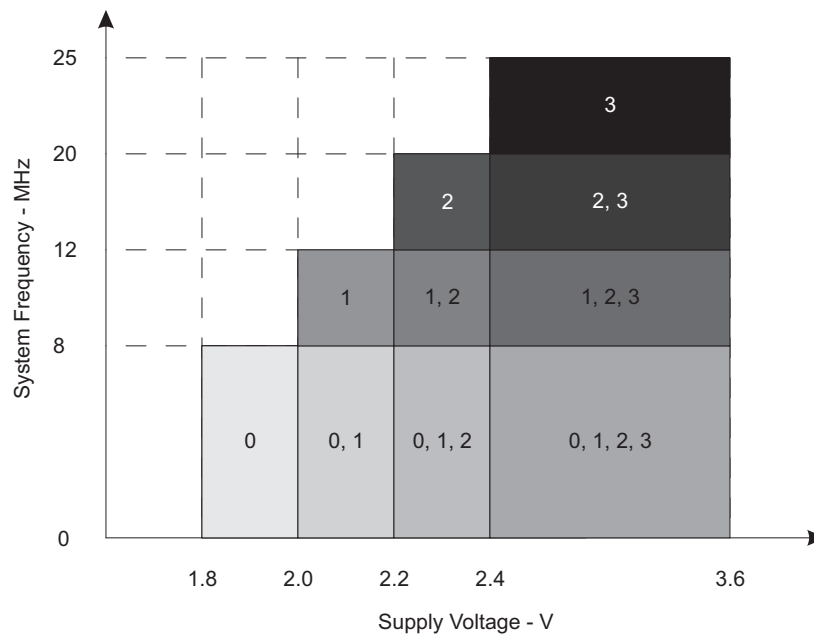
**Figure 1.  $V_{CC}$  and  $V_{IO}$  Power Sequencing**



NOTE: The device remains in reset based on the conditions of the  $\overline{RSTDV_{CC}}$  and  $\overline{RST}$  pins and the voltage present on  $DV_{CC}$  voltage supply. If  $\overline{RSTDV_{CC}}$  or  $\overline{RST}$  is held at a logic low or if  $DV_{CC}$  is below the  $SVSH\_+$  minimum threshold, the device remains in its reset condition; that is, these conditions form a logical OR with respect to device reset.

Figure 2. Reset Timing





The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 3. Maximum System Frequency**

## Electrical Characteristics

### Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

| PARAMETER              | EXECUTION MEMORY | V <sub>CC</sub> | PMMCOREVx | FREQUENCY (f <sub>DCO</sub> = f <sub>MCLK</sub> = f <sub>SMCLK</sub> ) |      |       |      |        |     |        |     |        |      | UNIT |
|------------------------|------------------|-----------------|-----------|------------------------------------------------------------------------|------|-------|------|--------|-----|--------|-----|--------|------|------|
|                        |                  |                 |           | 1 MHz                                                                  |      | 8 MHz |      | 12 MHz |     | 20 MHz |     | 25 MHz |      |      |
|                        |                  |                 |           | TYP                                                                    | MAX  | TYP   | MAX  | TYP    | MAX | TYP    | MAX | TYP    | MAX  |      |
| I <sub>AM, Flash</sub> | Flash            | 3.0 V           | 0         | 0.36                                                                   | 0.47 | 2.32  | 2.60 |        |     |        |     |        |      | mA   |
|                        |                  |                 | 1         | 0.40                                                                   |      | 2.65  |      | 4.0    | 4.4 |        |     |        |      |      |
|                        |                  |                 | 2         | 0.44                                                                   |      | 2.90  |      | 4.3    |     | 7.1    | 7.7 |        |      |      |
|                        |                  |                 | 3         | 0.46                                                                   |      | 3.10  |      | 4.6    |     | 7.6    |     | 10.1   | 11.0 |      |
| I <sub>AM, RAM</sub>   | RAM              | 3.0 V           | 0         | 0.20                                                                   | 0.29 | 1.20  | 1.30 |        |     |        |     |        |      | mA   |
|                        |                  |                 | 1         | 0.22                                                                   |      | 1.35  |      | 2.0    | 2.2 |        |     |        |      |      |
|                        |                  |                 | 2         | 0.24                                                                   |      | 1.50  |      | 2.2    |     | 3.7    | 4.2 |        |      |      |
|                        |                  |                 | 3         | 0.26                                                                   |      | 1.60  |      | 2.4    |     | 3.9    |     | 5.3    | 6.2  |      |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.  
 $f_{ACLK} = 32786$  Hz,  $f_{DCO} = f_{MCLK} = f_{SMCLK}$  at specified frequency.  
 $XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$ .

## Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                                                                                                                       | $V_{CC}$ | PMMCOREVx | -40 °C |     | 25 °C |      | 60 °C |     | 85 °C |      | UNIT    |
|-------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----------|--------|-----|-------|------|-------|-----|-------|------|---------|
|                                                                                                                                                 |          |           | TYP    | MAX | TYP   | MAX  | TYP   | MAX | TYP   | MAX  |         |
| $I_{LPM0,1MHz}$ Low-power mode 0 <sup>(3)(4)</sup>                                                                                              | 2.2 V    | 0         | 73     |     | 77    | 91   | 80    |     | 85    | 97   | $\mu A$ |
|                                                                                                                                                 | 3.0 V    | 3         | 79     |     | 83    | 99   | 88    |     | 95    | 107  |         |
| $I_{LPM2}$ Low-power mode 2 <sup>(5)(4)</sup>                                                                                                   | 2.2 V    | 0         | 6.5    |     | 6.5   | 12   | 10    |     | 11    | 17   | $\mu A$ |
|                                                                                                                                                 | 3.0 V    | 3         | 7.0    |     | 7.0   | 13   | 11    |     | 12    | 18   |         |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode <sup>(6)(4)</sup>                                                                               | 2.2 V    | 0         | 1.60   |     | 1.90  |      | 2.8   |     | 6.0   |      | $\mu A$ |
|                                                                                                                                                 |          | 1         | 1.65   |     | 2.00  |      | 3.0   |     | 6.3   |      |         |
|                                                                                                                                                 |          | 2         | 1.75   |     | 2.15  |      | 3.2   |     | 6.6   |      |         |
|                                                                                                                                                 | 3.0 V    | 0         | 1.8    |     | 2.1   | 2.9  | 3.0   |     | 6.2   | 9.4  |         |
|                                                                                                                                                 |          | 1         | 1.9    |     | 2.3   |      | 3.2   |     | 6.5   |      |         |
|                                                                                                                                                 |          | 2         | 2.0    |     | 2.4   |      | 3.3   |     | 6.8   |      |         |
|                                                                                                                                                 |          | 3         | 2.0    |     | 2.5   | 3.9  | 3.4   |     | 6.8   | 10.9 |         |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode <sup>(7)(4)</sup>                                                                                     | 3.0 V    | 0         | 1.1    |     | 1.4   | 2.7  | 2.0   |     | 6.1   | 9.7  | $\mu A$ |
|                                                                                                                                                 |          | 1         | 1.1    |     | 1.4   |      | 2.2   |     | 6.4   |      |         |
|                                                                                                                                                 |          | 2         | 1.2    |     | 1.5   |      | 2.3   |     | 6.8   |      |         |
|                                                                                                                                                 |          | 3         | 1.3    |     | 1.6   | 3.0  | 2.3   |     | 6.8   | 10.9 |         |
| $I_{LPM4}$ Low-power mode 4 <sup>(8)(4)</sup>                                                                                                   | 3.0 V    | 0         | 0.9    |     | 1.1   | 1.5  | 2.0   |     | 5.1   | 8.8  | $\mu A$ |
|                                                                                                                                                 |          | 1         | 1.1    |     | 1.2   |      | 2.1   |     | 5.3   |      |         |
|                                                                                                                                                 |          | 2         | 1.2    |     | 1.2   |      | 2.2   |     | 5.5   |      |         |
|                                                                                                                                                 |          | 3         | 1.3    |     | 1.3   | 1.6  | 2.2   |     | 5.5   | 9.8  |         |
| $I_{LPM4.5}$ Low-power mode 4.5 <sup>(9)</sup>                                                                                                  | 3.0 V    |           | 0.15   |     | 0.18  | 0.35 | 0.26  |     | 0.5   | 1.0  | $\mu A$ |
| $I_{DVIO\_START}$ Current supplied from DVIO while DVCC = AVCC = 0 V, DVIO = 1.62 V to 1.98 V, All DVIO I/O floating including BLEN and RST/NMI | 0 V      |           | 1.8    |     | 1.8   |      | 1.8   |     | 1.8   |      | $\mu A$ |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for the watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE<sub>x</sub> = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0);  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 1 MHz
- (4) Current for brownout and high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM<sub>L</sub>) disabled. High-side monitor (SVM<sub>H</sub>) disabled. RAM retention enabled.
- (5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE<sub>x</sub> = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2);  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  = 0 MHz,  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.)
- (6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVE<sub>x</sub> = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3);  $f_{ACLK}$  = 32768 Hz,  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz
- (7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3);  $f_{ACLK}$  =  $f_{VLO}$ ,  $f_{MCLK}$  =  $f_{SMCLK}$  =  $f_{DCO}$  = 0 MHz
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4);  $f_{DCO}$  =  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz
- (9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5);  $f_{DCO}$  =  $f_{ACLK}$  =  $f_{MCLK}$  =  $f_{SMCLK}$  = 0 MHz

### Schmitt-Trigger Inputs – General-Purpose I/O DVCC Domain<sup>(1)</sup> (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RSTDVCC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                    | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|-----------------|------|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |                                                                                                    | 1.8 V           | 0.80 |     | 1.40 | V    |
|                                                                                  |                                                                                                    | 3 V             | 1.50 |     | 2.10 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage                          |                                                                                                    | 1.8 V           | 0.45 |     | 1.00 | V    |
|                                                                                  |                                                                                                    | 3 V             | 0.75 |     | 1.65 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) |                                                                                                    | 1.8 V           | 0.3  |     | 0.8  | V    |
|                                                                                  |                                                                                                    | 3 V             | 0.4  |     | 1.0  |      |
| R <sub>Pull</sub> Pullup or pulldown resistor                                    | For pullup: V <sub>IN</sub> = V <sub>SS</sub> ,<br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> |                 | 20   | 35  | 50   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                               |                 |      | 5   |      | pF   |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

### Schmitt-Trigger Inputs – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5, $\overline{\text{RST}}$ /NMI, BLEN)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                    | V <sub>IO</sub>  | MIN | TYP | MAX  | UNIT |
|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|------------------|-----|-----|------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          | V <sub>CC</sub> = 3.0 V                                                                            | 1.62 V           | 0.8 |     | 1.25 | V    |
|                                                                                  |                                                                                                    | 1.98 V           | 1.1 |     | 1.40 |      |
| V <sub>IT-</sub> Negative-going input threshold voltage                          | V <sub>CC</sub> = 3.0 V                                                                            | 1.62 V           | 0.3 |     | 0.7  | V    |
|                                                                                  |                                                                                                    | 1.98 V           | 0.5 |     | 1.0  |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) | V <sub>CC</sub> = 3.0 V                                                                            | 1.62 V to 1.98 V | 0.3 |     | 0.8  | V    |
| R <sub>Pull</sub> Pullup or pulldown resistor                                    | For pullup: V <sub>IN</sub> = V <sub>SS</sub> ,<br>For pulldown: V <sub>IN</sub> = V <sub>IO</sub> |                  | 20  | 35  | 50   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>IO</sub>                                               |                  |     | 5   |      | pF   |

### Inputs – Interrupts DVCC Domain Port P1 (P1.0 to P1.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS                                       | V <sub>CC</sub> | MIN | MAX | UNIT |
|-------------------------------------------------------------|-------------------------------------------------------|-----------------|-----|-----|------|
| t <sub>(int)</sub> External interrupt timing <sup>(1)</sup> | External trigger pulse duration to set interrupt flag | 1.8 V, 3 V      | 20  |     | ns   |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

### Inputs – Interrupts DVIO Domain Ports P1 and P2 (P1.4 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                   | TEST CONDITIONS                                                                            | V <sub>IO</sub> <sup>(1)</sup> | MIN | MAX | UNIT |
|-------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------------------|-----|-----|------|
| t <sub>(int)</sub> External interrupt timing <sup>(2)</sup> | External trigger pulse duration to set interrupt flag,<br>V <sub>CC</sub> = 1.8 V or 3.0 V | 1.62 V to 1.98 V               | 20  |     | ns   |

(1) In all test conditions, V<sub>IO</sub> ≤ V<sub>CC</sub>.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

### Leakage Current – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                              | TEST CONDITIONS | V <sub>CC</sub> | MIN | MAX | UNIT |
|--------------------------------------------------------|-----------------|-----------------|-----|-----|------|
| I <sub>lkg</sub> (Px.y) High-impedance leakage current | (1) (2)         | 1.8 V, 3 V      | -50 | 50  | nA   |

- (1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pins, unless otherwise noted.  
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

### Leakage Current – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                              | TEST CONDITIONS | V <sub>IO</sub> <sup>(1)</sup> | MIN | MAX | UNIT |
|--------------------------------------------------------|-----------------|--------------------------------|-----|-----|------|
| I <sub>lkg</sub> (Px.y) High-impedance leakage current | (2) (3)         | 1.62 V to 1.98 V               | -50 | 50  | nA   |

- (1) In all test conditions, V<sub>IO</sub> ≤ V<sub>CC</sub>.  
(2) The leakage current is measured with V<sub>SS</sub> or V<sub>IO</sub> applied to the corresponding pins, unless otherwise noted.  
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

### Outputs – General-Purpose I/O DVCC Domain (Full Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                              | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|----------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = -3 mA <sup>(1)</sup>  | 1.8 V           | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = -10 mA <sup>(2)</sup> |                 | V <sub>CC</sub> - 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = -5 mA <sup>(1)</sup>  | 3 V             | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = -15 mA <sup>(2)</sup> |                 | V <sub>CC</sub> - 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 3 mA <sup>(1)</sup>   | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 10 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 5 mA <sup>(1)</sup>   | 3 V             | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 15 mA <sup>(2)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.  
(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

### Outputs – General-Purpose I/O DVCC Domain (Reduced Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN                    | MAX                    | UNIT |
|-------------------------------------------|---------------------------------------------|-----------------|------------------------|------------------------|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = -1 mA <sup>(2)</sup> | 1.8 V           | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        | V    |
|                                           | I <sub>(OHmax)</sub> = -3 mA <sup>(3)</sup> |                 | V <sub>CC</sub> - 0.60 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = -2 mA <sup>(2)</sup> | 3.0 V           | V <sub>CC</sub> - 0.25 | V <sub>CC</sub>        |      |
|                                           | I <sub>(OHmax)</sub> = -6 mA <sup>(3)</sup> |                 | V <sub>CC</sub> - 0.60 | V <sub>CC</sub>        |      |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 1 mA <sup>(2)</sup>  | 1.8 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 | V    |
|                                           | I <sub>(OLmax)</sub> = 3 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |
|                                           | I <sub>(OLmax)</sub> = 2 mA <sup>(2)</sup>  | 3.0 V           | V <sub>SS</sub>        | V <sub>SS</sub> + 0.25 |      |
|                                           | I <sub>(OLmax)</sub> = 6 mA <sup>(3)</sup>  |                 | V <sub>SS</sub>        | V <sub>SS</sub> + 0.60 |      |

- (1) Selecting reduced drive strength may reduce EMI.  
(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.  
(3) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

## Outputs – General-Purpose I/O DVIO Domain (Full Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER |                           | TEST CONDITIONS                     | $V_{IO}^{(1)}$   | MIN             | MAX             | UNIT |
|-----------|---------------------------|-------------------------------------|------------------|-----------------|-----------------|------|
| $V_{OH}$  | High-level output voltage | $I_{(OHmax)} = -3 \text{ mA}^{(2)}$ | 1.62 V to 1.98 V | $V_{IO} - 0.25$ | $V_{IO}$        | V    |
|           |                           | $I_{(OHmax)} = -6 \text{ mA}^{(2)}$ |                  | $V_{IO} - 0.50$ | $V_{IO}$        |      |
| $V_{OL}$  | Low-level output voltage  | $I_{(OLmax)} = 3 \text{ mA}^{(2)}$  | 1.62 V to 1.98 V | $V_{SS}$        | $V_{SS} + 0.25$ | V    |
|           |                           | $I_{(OLmax)} = 6 \text{ mA}^{(2)}$  |                  | $V_{SS}$        | $V_{SS} + 0.50$ |      |

(1) In all test conditions,  $V_{IO} \leq V_{CC}$ .

(2) The maximum total current,  $I_{(OHmax)}$  and  $I_{(OLmax)}$ , for all outputs combined, should not exceed  $\pm 48 \text{ mA}$  to hold the maximum voltage drop specified.

## Outputs – General-Purpose I/O DVIO Domain (Reduced Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER |                           | TEST CONDITIONS                     | $V_{IO}^{(2)}$   | MIN             | MAX             | UNIT |
|-----------|---------------------------|-------------------------------------|------------------|-----------------|-----------------|------|
| $V_{OH}$  | High-level output voltage | $I_{(OHmax)} = -1 \text{ mA}^{(3)}$ | 1.62 V to 1.98 V | $V_{IO} - 0.25$ | $V_{IO}$        | V    |
|           |                           | $I_{(OHmax)} = -2 \text{ mA}^{(3)}$ |                  | $V_{IO} - 0.50$ | $V_{IO}$        |      |
| $V_{OL}$  | Low-level output voltage  | $I_{(OLmax)} = 1 \text{ mA}^{(3)}$  | 1.62 V to 1.98 V | $V_{SS}$        | $V_{SS} + 0.25$ | V    |
|           |                           | $I_{(OLmax)} = 2 \text{ mA}^{(3)}$  |                  | $V_{SS}$        | $V_{SS} + 0.50$ |      |

(1) Selecting reduced drive strength may reduce EMI.

(2) In all test conditions,  $V_{IO} \leq V_{CC}$ .

(3) The maximum total current,  $I_{(OHmax)}$  and  $I_{(OLmax)}$ , for all outputs combined, should not exceed  $\pm 48 \text{ mA}$  to hold the maximum voltage drop specified.

## Output Frequency – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS                                     |                                            | MIN | MAX | UNIT |
|----------------------------------------------|-----------------------------------------------------|--------------------------------------------|-----|-----|------|
| $f_{Px,y}$ Port output frequency (with load) | (1)(2)                                              | $V_{CC} = 1.8\text{ V}$ ,<br>PMMCOREVx = 0 |     | 16  | MHz  |
|                                              |                                                     | $V_{CC} = 3\text{ V}$ ,<br>PMMCOREVx = 3   |     | 25  |      |
| $f_{Port\_CLK}$ Clock output frequency       | ACLK, SMCLK, or MCLK,<br>$C_L = 20\text{ pF}^{(2)}$ | $V_{CC} = 1.8\text{ V}$ ,<br>PMMCOREVx = 0 |     | 16  | MHz  |
|                                              |                                                     | $V_{CC} = 3\text{ V}$ ,<br>PMMCOREVx = 3   |     | 25  |      |

- (1) A resistive divider with  $2 \times R1$  between  $V_{CC}$  and  $V_{SS}$  is used as load. The output is connected to the center tap of the divider. For full drive strength,  $R1 = 550\ \Omega$ . For reduced drive strength,  $R1 = 1.6\text{ k}\Omega$ .  $C_L = 20\text{ pF}$  is connected to the output to  $V_{SS}$ .
- (2) The output voltage reaches at least 10% and 90%  $V_{CC}$  at the specified toggle frequency.

## Output Frequency – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS                                     |                                                                    | MIN | MAX | UNIT |
|----------------------------------------------|-----------------------------------------------------|--------------------------------------------------------------------|-----|-----|------|
| $f_{Px,y}$ Port output frequency (with load) | (1)(2)                                              | $V_{IO} = 1.62\text{ V to }1.98\text{ V}^{(3)}$ ,<br>PMMCOREVx = 0 |     | 16  | MHz  |
|                                              |                                                     | $V_{IO} = 1.62\text{ V to }1.98\text{ V}^{(3)}$ ,<br>PMMCOREVx = 3 |     | 25  |      |
| $f_{Port\_CLK}$ Clock output frequency       | ACLK, SMCLK, or MCLK,<br>$C_L = 20\text{ pF}^{(2)}$ | $V_{IO} = 1.62\text{ V to }1.98\text{ V}^{(3)}$ ,<br>PMMCOREVx = 0 |     | 16  | MHz  |
|                                              |                                                     | $V_{IO} = 1.62\text{ V to }1.98\text{ V}^{(3)}$ ,<br>PMMCOREVx = 3 |     | 25  |      |

- (1) A resistive divider with  $2 \times R1$  between  $V_{IO}$  and  $V_{SS}$  is used as load. The output is connected to the center tap of the divider. For full drive strength,  $R1 = 550\ \Omega$ . For reduced drive strength,  $R1 = 1.6\text{ k}\Omega$ .  $C_L = 20\text{ pF}$  is connected to the output to  $V_{SS}$ .
- (2) The output voltage reaches at least 10% and 90%  $V_{IO}$  at the specified toggle frequency.
- (3) In all test conditions,  $V_{IO} \leq V_{CC}$ .

## Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

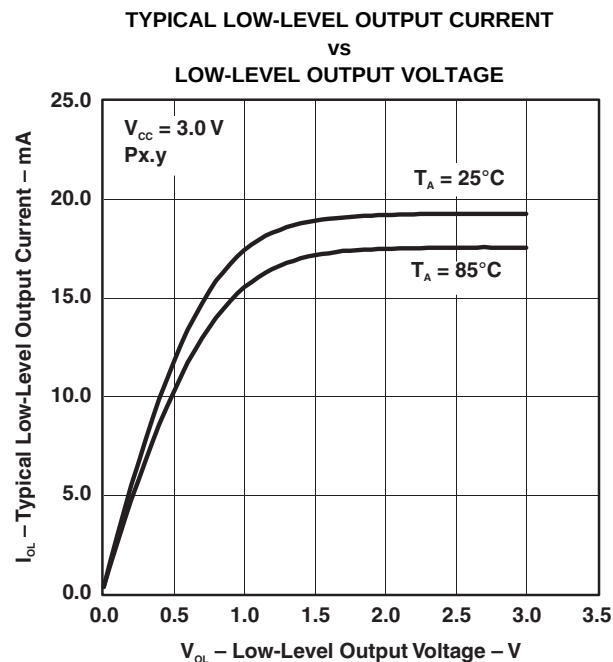


Figure 4.

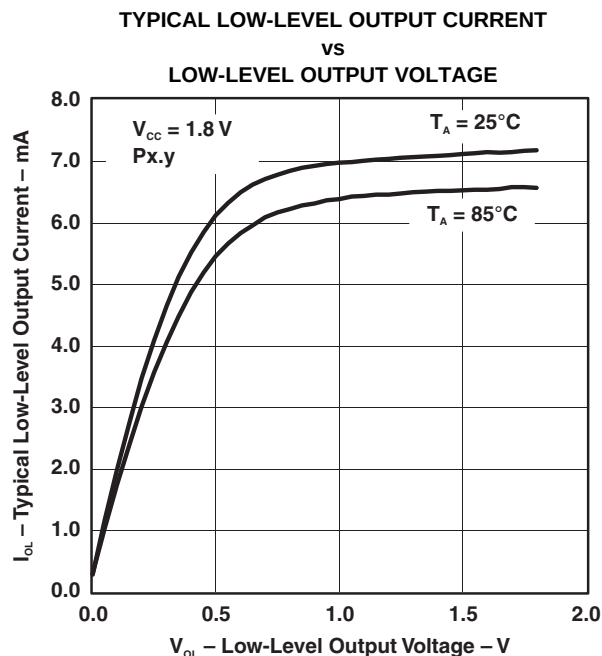


Figure 5.

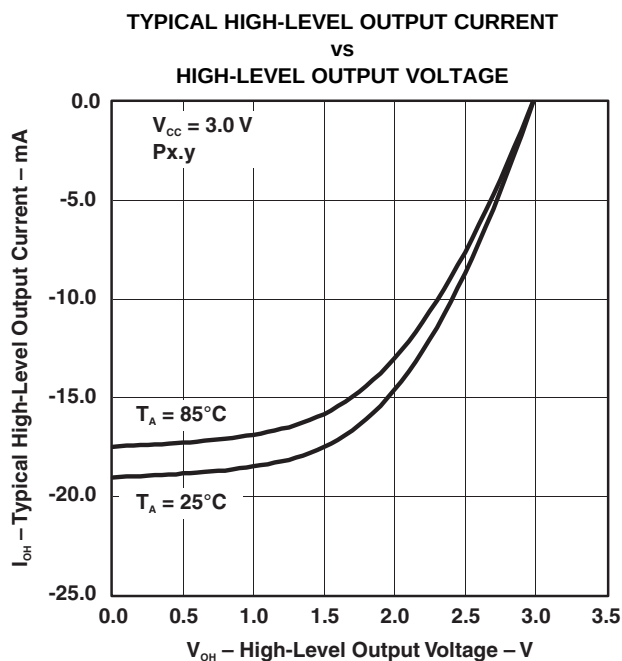


Figure 6.

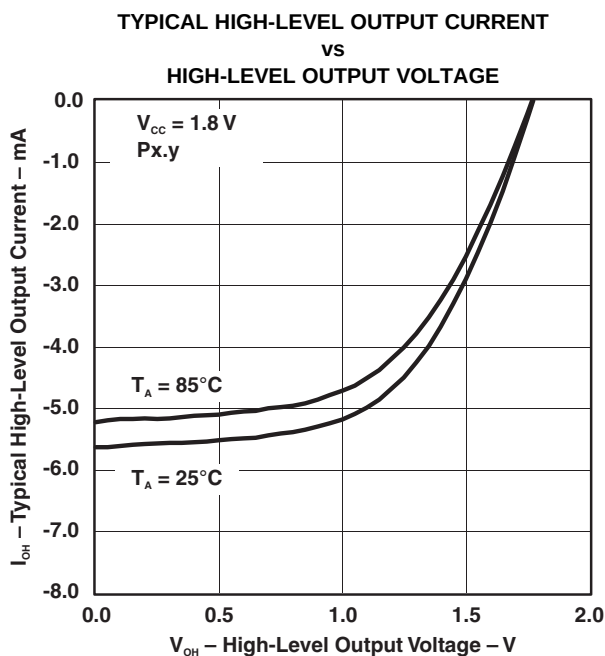


Figure 7.



## Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

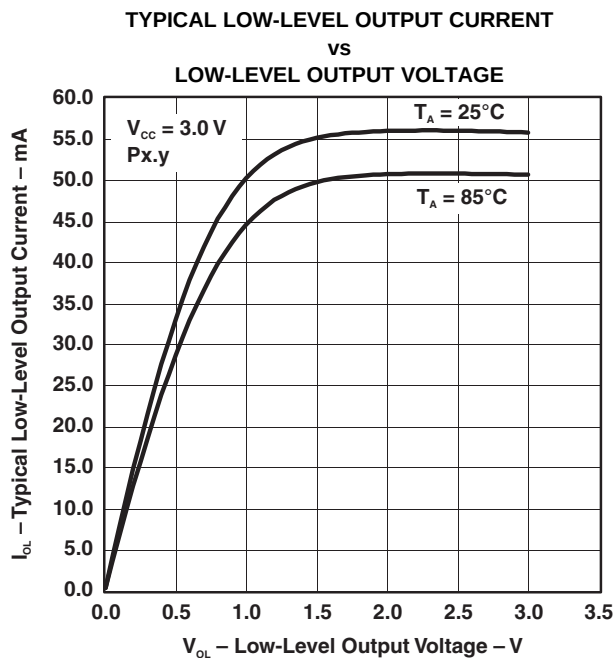


Figure 8.

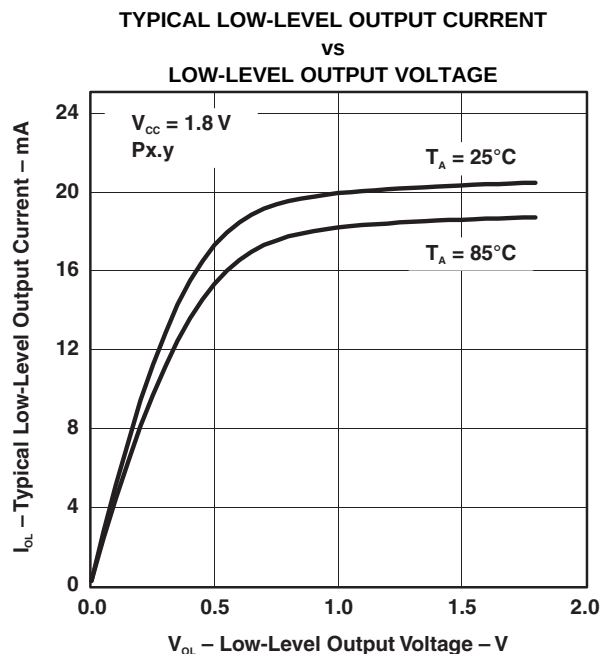


Figure 9.

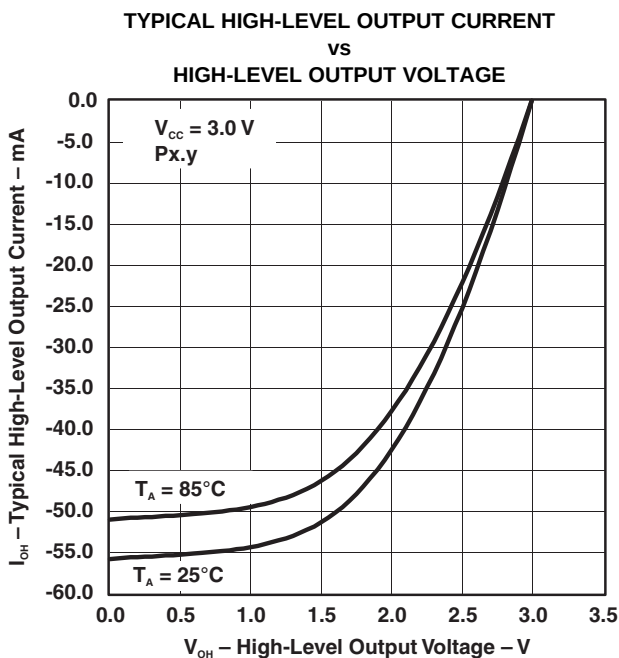


Figure 10.

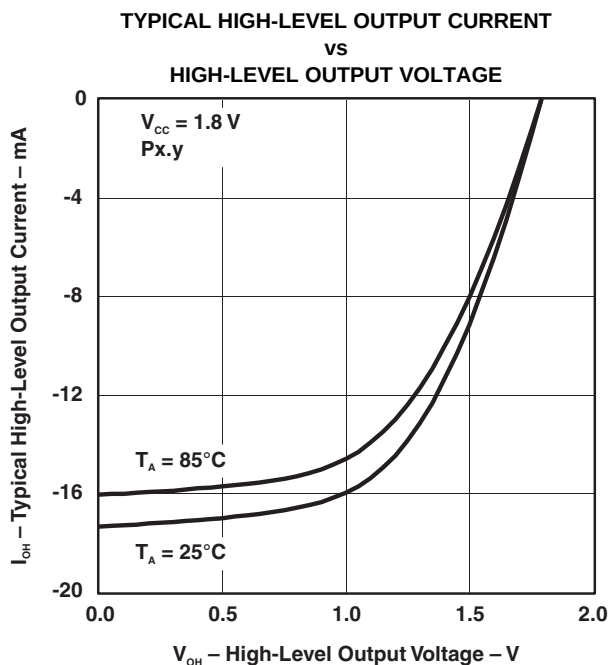


Figure 11.

## Crystal Oscillator, XT1, Low-Frequency Mode<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                            | TEST CONDITIONS                                                                                                                   | V <sub>CC</sub> | MIN   | TYP    | MAX | UNIT |
|------------------------|--------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|--------|-----|------|
| ΔI <sub>DVCC,LF</sub>  | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1, T <sub>A</sub> = 25°C                             | 3.0 V           | 0.075 |        |     | μA   |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 2, T <sub>A</sub> = 25°C                             |                 | 0.170 |        |     |      |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C                             |                 | 0.290 |        |     |      |
| f <sub>XT1,LF0</sub>   | XT1 oscillator crystal frequency, LF mode                                                  | XTS = 0, XT1BYPASS = 0                                                                                                            |                 | 32768 |        |     | Hz   |
| f <sub>XT1,LF,SW</sub> | XT1 oscillator logic-level square-wave input frequency, LF mode                            | XTS = 0, XT1BYPASS = 1 <sup>(2)(3)</sup><br>XT1BYPASSLV = 0 or 1                                                                  |                 | 10    | 32.768 | 50  | kHz  |
| OA <sub>LF</sub>       | Oscillation allowance for LF crystals <sup>(4)</sup>                                       | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, f <sub>XT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF                      |                 | 210   |        |     | kΩ   |
|                        |                                                                                            | XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 1, f <sub>XT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF                     |                 | 300   |        |     |      |
| C <sub>L,eff</sub>     | Integrated effective load capacitance, LF mode <sup>(5)</sup>                              | XTS = 0, XCAP <sub>x</sub> = 0 <sup>(6)</sup>                                                                                     |                 | 2     |        |     | pF   |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 1                                                                                                    |                 | 5.5   |        |     |      |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 2                                                                                                    |                 | 8.5   |        |     |      |
|                        |                                                                                            | XTS = 0, XCAP <sub>x</sub> = 3                                                                                                    |                 | 12.0  |        |     |      |
| Duty cycle, LF mode    |                                                                                            | XTS = 0, Measured at ACLK, f <sub>XT1,LF</sub> = 32768 Hz                                                                         |                 | 30    | 70     |     | %    |
| f <sub>Fault,LF</sub>  | Oscillator fault frequency, LF mode <sup>(7)</sup>                                         | XTS = 0, XT1BYPASS = 1 <sup>(8)</sup> , XT1BYPASSLV = 0 or 1                                                                      |                 | 10    | 10000  |     | Hz   |
| t <sub>START,LF</sub>  | Startup time, LF mode                                                                      | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 0, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 6 pF  | 3.0 V           | 1000  |        |     | ms   |
|                        |                                                                                            | f <sub>OSC</sub> = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 12 pF |                 | 500   |        |     |      |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - (a) Keep the trace between the device and the crystal as short as possible.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parameters defined in the Schmitt-Trigger Inputs section of this datasheet. When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT1BYPASSLV = 0) or DVSS to DVIO (XT1BYPASSLV = 1). In this case, it is required that the pin be configured properly for the intended input swing.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE<sub>x</sub> settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but each application should be evaluated based on the actual crystal selected:
  - (a) For XT1DRIVE<sub>x</sub> = 0, C<sub>L,eff</sub> ≤ 6 pF
  - (b) For XT1DRIVE<sub>x</sub> = 1, 6 pF ≤ C<sub>L,eff</sub> ≤ 9 pF
  - (c) For XT1DRIVE<sub>x</sub> = 2, 6 pF ≤ C<sub>L,eff</sub> ≤ 10 pF
  - (d) For XT1DRIVE<sub>x</sub> = 3, C<sub>L,eff</sub> ≥ 6 pF
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

## Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                                                                  | TEST CONDITIONS                                                                                                        | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| I <sub>DVCC,XT2</sub> XT2 oscillator crystal current consumption                           | f <sub>OSC</sub> = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 0, T <sub>A</sub> = 25°C                  | 3.0 V           |     | 200 |     | μA   |
|                                                                                            | f <sub>OSC</sub> = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 1, T <sub>A</sub> = 25°C                 |                 |     | 260 |     |      |
|                                                                                            | f <sub>OSC</sub> = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 2, T <sub>A</sub> = 25°C                 |                 |     | 325 |     |      |
|                                                                                            | f <sub>OSC</sub> = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 3, T <sub>A</sub> = 25°C                 |                 |     | 450 |     |      |
| f <sub>XT2,HF0</sub> XT2 oscillator crystal frequency, mode 0                              | XT2DRIVE <sub>x</sub> = 0, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 4   |     | 8   | MHz  |
| f <sub>XT2,HF1</sub> XT2 oscillator crystal frequency, mode 1                              | XT2DRIVE <sub>x</sub> = 1, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 8   |     | 16  | MHz  |
| f <sub>XT2,HF2</sub> XT2 oscillator crystal frequency, mode 2                              | XT2DRIVE <sub>x</sub> = 2, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 16  |     | 24  | MHz  |
| f <sub>XT2,HF3</sub> XT2 oscillator crystal frequency, mode 3                              | XT2DRIVE <sub>x</sub> = 3, XT2BYPASS = 0 <sup>(3)</sup>                                                                |                 | 24  |     | 32  | MHz  |
| f <sub>XT2,HF,SW</sub> XT2 oscillator logic-level square-wave input frequency, bypass mode | XT2BYPASS = 1 <sup>(4)(3)</sup><br>XT2BYPASSLV = 0 or 1                                                                |                 | 0.7 |     | 32  | MHz  |
| O <sub>AHF</sub> Oscillation allowance for HF crystals <sup>(5)</sup>                      | XT2DRIVE <sub>x</sub> = 0, XT2BYPASS = 0, f <sub>XT2,HF0</sub> = 6 MHz, C <sub>L,eff</sub> = 15 pF                     |                 |     | 450 |     | Ω    |
|                                                                                            | XT2DRIVE <sub>x</sub> = 1, XT2BYPASS = 0, f <sub>XT2,HF1</sub> = 12 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 320 |     |      |
|                                                                                            | XT2DRIVE <sub>x</sub> = 2, XT2BYPASS = 0, f <sub>XT2,HF2</sub> = 20 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 200 |     |      |
|                                                                                            | XT2DRIVE <sub>x</sub> = 3, XT2BYPASS = 0, f <sub>XT2,HF3</sub> = 32 MHz, C <sub>L,eff</sub> = 15 pF                    |                 |     | 200 |     |      |
| t <sub>START,HF</sub> Startup time                                                         | f <sub>OSC</sub> = 6 MHz, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 0, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF  | 3.0 V           |     | 0.5 |     | ms   |
|                                                                                            | f <sub>OSC</sub> = 20 MHz, XT2BYPASS = 0, XT2DRIVE <sub>x</sub> = 2, T <sub>A</sub> = 25°C, C <sub>L,eff</sub> = 15 pF |                 |     | 0.3 |     |      |
| C <sub>L,eff</sub> Integrated effective load capacitance, HF mode <sup>(6) (1)</sup>       |                                                                                                                        |                 |     | 1   |     | pF   |
| Duty cycle                                                                                 | Measured at ACLK, f <sub>XT2,HF2</sub> = 20 MHz                                                                        |                 | 40  | 50  | 60  | %    |

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

(a) Keep the traces between the device and the crystal as short as possible.

(b) Design a good ground plane around the oscillator pins.

(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.

(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.

(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.

(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT2BYPASSLV = 0) or DVSS to DVIO (XT2BYPASSLV = 1). In this case, it is required that the pin be configured properly for the intended input swing.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

## Crystal Oscillator, XT2 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                                       | TEST CONDITIONS                                        | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------|--------------------------------------------------------|-----------------|-----|-----|-----|------|
| f <sub>Fault,HF</sub> Oscillator fault frequency <sup>(7)</sup> | XT2BYPASS = 1 <sup>(8)</sup> ,<br>XT2BYPASSLV = 0 or 1 |                 | 30  |     | 300 | kHz  |

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals. In general, an effective load capacitance of up to 18 pF can be supported.

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                              | TEST CONDITIONS                 | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub> VLO frequency                                         | Measured at ACLK                | 1.8 V to 3.6 V  | 6   | 9.4 | 14  | kHz  |
| df <sub>VLO</sub> /dT VLO frequency temperature drift                  | Measured at ACLK <sup>(1)</sup> | 1.8 V to 3.6 V  |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> VLO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup> | 1.8 V to 3.6 V  |     | 4   |     | %/V  |
| Duty cycle                                                             | Measured at ACLK                | 1.8 V to 3.6 V  | 40  | 50  | 60  | %    |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

## Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                | TEST CONDITIONS                    | V <sub>CC</sub>        | MIN  | TYP   | MAX | UNIT |
|--------------------------------------------------------------------------|------------------------------------|------------------------|------|-------|-----|------|
| I <sub>REFO</sub> REFO oscillator current consumption                    | T <sub>A</sub> = 25°C              | 1.8 V to 3.6 V         |      | 3     |     | μA   |
| f <sub>REFO</sub>                                                        | REFO frequency calibrated          | 1.8 V to 3.6 V         |      | 32768 |     | Hz   |
|                                                                          | REFO absolute tolerance calibrated | Full temperature range |      |       |     |      |
|                                                                          | T <sub>A</sub> = 25°C              | 1.8 V to 3.6 V         | -3.5 |       | 3.5 | %    |
| df <sub>REFO</sub> /dT REFO frequency temperature drift                  | Measured at ACLK <sup>(1)</sup>    | 1.8 V to 3.6 V         |      | 0.01  |     | %/°C |
| df <sub>REFO</sub> /dV <sub>CC</sub> REFO frequency supply voltage drift | Measured at ACLK <sup>(2)</sup>    | 1.8 V to 3.6 V         |      | 1.0   |     | %/V  |
| Duty cycle                                                               | Measured at ACLK                   | 1.8 V to 3.6 V         | 40   | 50    | 60  | %    |
| t <sub>START</sub> REFO startup time                                     | 40%/60% duty cycle                 | 1.8 V to 3.6 V         |      | 25    |     | μs   |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

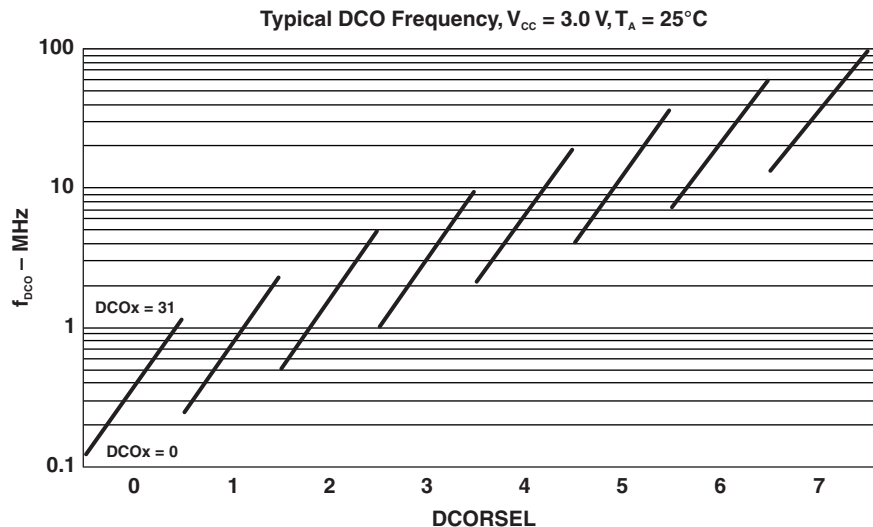
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

## DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                                      | TEST CONDITIONS                                                                    | MIN  | TYP | MAX  | UNIT  |
|-------------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------|------|-----|------|-------|
| f <sub>DCO(0,0)</sub>               | DCO frequency (0, 0) <sup>(1)</sup>                  | DCORSELx = 0, DCOx = 0, MODx = 0                                                   | 0.07 |     | 0.20 | MHz   |
| f <sub>DCO(0,31)</sub>              | DCO frequency (0, 31) <sup>(1)</sup>                 | DCORSELx = 0, DCOx = 31, MODx = 0                                                  | 0.70 |     | 1.70 | MHz   |
| f <sub>DCO(1,0)</sub>               | DCO frequency (1, 0) <sup>(1)</sup>                  | DCORSELx = 1, DCOx = 0, MODx = 0                                                   | 0.15 |     | 0.36 | MHz   |
| f <sub>DCO(1,31)</sub>              | DCO frequency (1, 31) <sup>(1)</sup>                 | DCORSELx = 1, DCOx = 31, MODx = 0                                                  | 1.47 |     | 3.45 | MHz   |
| f <sub>DCO(2,0)</sub>               | DCO frequency (2, 0) <sup>(1)</sup>                  | DCORSELx = 2, DCOx = 0, MODx = 0                                                   | 0.32 |     | 0.75 | MHz   |
| f <sub>DCO(2,31)</sub>              | DCO frequency (2, 31) <sup>(1)</sup>                 | DCORSELx = 2, DCOx = 31, MODx = 0                                                  | 3.17 |     | 7.38 | MHz   |
| f <sub>DCO(3,0)</sub>               | DCO frequency (3, 0) <sup>(1)</sup>                  | DCORSELx = 3, DCOx = 0, MODx = 0                                                   | 0.64 |     | 1.51 | MHz   |
| f <sub>DCO(3,31)</sub>              | DCO frequency (3, 31) <sup>(1)</sup>                 | DCORSELx = 3, DCOx = 31, MODx = 0                                                  | 6.07 |     | 14.0 | MHz   |
| f <sub>DCO(4,0)</sub>               | DCO frequency (4, 0) <sup>(1)</sup>                  | DCORSELx = 4, DCOx = 0, MODx = 0                                                   | 1.3  |     | 3.2  | MHz   |
| f <sub>DCO(4,31)</sub>              | DCO frequency (4, 31) <sup>(1)</sup>                 | DCORSELx = 4, DCOx = 31, MODx = 0                                                  | 12.3 |     | 28.2 | MHz   |
| f <sub>DCO(5,0)</sub>               | DCO frequency (5, 0) <sup>(1)</sup>                  | DCORSELx = 5, DCOx = 0, MODx = 0                                                   | 2.5  |     | 6.0  | MHz   |
| f <sub>DCO(5,31)</sub>              | DCO frequency (5, 31) <sup>(1)</sup>                 | DCORSELx = 5, DCOx = 31, MODx = 0                                                  | 23.7 |     | 54.1 | MHz   |
| f <sub>DCO(6,0)</sub>               | DCO frequency (6, 0) <sup>(1)</sup>                  | DCORSELx = 6, DCOx = 0, MODx = 0                                                   | 4.6  |     | 10.7 | MHz   |
| f <sub>DCO(6,31)</sub>              | DCO frequency (6, 31) <sup>(1)</sup>                 | DCORSELx = 6, DCOx = 31, MODx = 0                                                  | 39.0 |     | 88.0 | MHz   |
| f <sub>DCO(7,0)</sub>               | DCO frequency (7, 0) <sup>(1)</sup>                  | DCORSELx = 7, DCOx = 0, MODx = 0                                                   | 8.5  |     | 19.6 | MHz   |
| f <sub>DCO(7,31)</sub>              | DCO frequency (7, 31) <sup>(1)</sup>                 | DCORSELx = 7, DCOx = 31, MODx = 0                                                  | 60   |     | 135  | MHz   |
| S <sub>DCORSEL</sub>                | Frequency step between range DCORSEL and DCORSEL + 1 | S <sub>RSEL</sub> = f <sub>DCO(DCORSEL+1,DCO)</sub> /f <sub>DCO(DCORSEL,DCO)</sub> | 1.2  |     | 2.3  | ratio |
| S <sub>DCO</sub>                    | Frequency step between tap DCO and DCO + 1           | S <sub>DCO</sub> = f <sub>DCO(DCORSEL,DCO+1)</sub> /f <sub>DCO(DCORSEL,DCO)</sub>  | 1.02 |     | 1.12 | ratio |
|                                     | Duty cycle                                           | Measured at SMCLK                                                                  | 40   | 50  | 60   | %     |
| df <sub>DCO</sub> /dT               | DCO frequency temperature drift <sup>(2)</sup>       | f <sub>DCO</sub> = 1 MHz                                                           |      | 0.1 |      | %/°C  |
| df <sub>DCO</sub> /dV <sub>CC</sub> | DCO frequency voltage drift <sup>(3)</sup>           | f <sub>DCO</sub> = 1 MHz                                                           |      | 1.9 |      | %/V   |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency,  $f_{\text{DCO}}$ , should be set to reside within the range of  $f_{\text{DCO}(n, 0), \text{MAX}} \leq f_{\text{DCO}} \leq f_{\text{DCO}(n, 31), \text{MIN}}$ , where  $f_{\text{DCO}(n, 0), \text{MAX}}$  represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and  $f_{\text{DCO}(n, 31), \text{MIN}}$  represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual  $f_{\text{DCO}}$  frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method:  $(\text{MAX}(-40 \text{ to } 85^\circ\text{C}) - \text{MIN}(-40 \text{ to } 85^\circ\text{C})) / \text{MIN}(-40 \text{ to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$
- (3) Calculated using the box method:  $(\text{MAX}(1.8 \text{ to } 3.6 \text{ V}) - \text{MIN}(1.8 \text{ to } 3.6 \text{ V})) / \text{MIN}(1.8 \text{ to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$



**Figure 12. Typical DCO frequency**

## PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                 |                                                                              | TEST CONDITIONS                 | MIN  | TYP  | MAX  | UNIT |
|---------------------------|------------------------------------------------------------------------------|---------------------------------|------|------|------|------|
| V <sub>DVCC_BOR_IT-</sub> | BOR <sub>H</sub> on voltage, DV <sub>CC</sub> falling level                  | dDV <sub>CC</sub> /dt   < 3 V/s |      |      | 1.45 | V    |
| V <sub>DVCC_BOR_IT+</sub> | BOR <sub>H</sub> off voltage, DV <sub>CC</sub> rising level                  | dDV <sub>CC</sub> /dt   < 3 V/s | 0.80 | 1.30 | 1.50 | V    |
| V <sub>DVCC_BOR_hys</sub> | BOR <sub>H</sub> hysteresis                                                  |                                 | 60   |      | 250  | mV   |
| t <sub>RESET</sub>        | Pulse duration required at $\overline{\text{RST/NMI}}$ pin to accept a reset |                                 | 2    |      |      | μs   |

## PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               |                                              | TEST CONDITIONS                  | MIN | TYP  | MAX | UNIT |
|-------------------------|----------------------------------------------|----------------------------------|-----|------|-----|------|
| V <sub>CORE3(AM)</sub>  | Core voltage, active mode, PMMCOREV = 3      | 2.4 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.90 |     | V    |
| V <sub>CORE2(AM)</sub>  | Core voltage, active mode, PMMCOREV = 2      | 2.2 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.80 |     | V    |
| V <sub>CORE1(AM)</sub>  | Core voltage, active mode, PMMCOREV = 1      | 2.0 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.60 |     | V    |
| V <sub>CORE0(AM)</sub>  | Core voltage, active mode, PMMCOREV = 0      | 1.8 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.40 |     | V    |
| V <sub>CORE3(LPM)</sub> | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.94 |     | V    |
| V <sub>CORE2(LPM)</sub> | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.84 |     | V    |
| V <sub>CORE1(LPM)</sub> | Core voltage, low-current mode, PMMCOREV = 1 | 2.0 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.64 |     | V    |
| V <sub>CORE0(LPM)</sub> | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ DV <sub>CC</sub> ≤ 3.6 V |     | 1.44 |     | V    |

## PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                           | TEST CONDITIONS                                              | MIN  | TYP  | MAX  | UNIT |
|---------------------------------------------------------------------|--------------------------------------------------------------|------|------|------|------|
| $I_{(SVSH)}$ SVS current consumption                                | SVSHE = 0, DV <sub>CC</sub> = 3.6 V                          |      | 0    |      | nA   |
|                                                                     | SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 0              |      | 200  |      | nA   |
|                                                                     | SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 1              |      | 1.5  |      | μA   |
| $V_{(SVSH\_IT-)}$ SVS <sub>H</sub> on voltage level <sup>(1)</sup>  | SVSHE = 1, SVSHRVL = 0                                       | 1.57 | 1.68 | 1.78 | V    |
|                                                                     | SVSHE = 1, SVSHRVL = 1                                       | 1.79 | 1.88 | 1.98 |      |
|                                                                     | SVSHE = 1, SVSHRVL = 2                                       | 1.98 | 2.08 | 2.21 |      |
|                                                                     | SVSHE = 1, SVSHRVL = 3                                       | 2.10 | 2.18 | 2.31 |      |
| $V_{(SVSH\_IT+)}$ SVS <sub>H</sub> off voltage level <sup>(1)</sup> | SVSHE = 1, SVSMHRRRL = 0                                     | 1.62 | 1.74 | 1.85 | V    |
|                                                                     | SVSHE = 1, SVSMHRRRL = 1                                     | 1.88 | 1.94 | 2.07 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 2                                     | 2.07 | 2.14 | 2.28 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 3                                     | 2.20 | 2.30 | 2.42 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 4                                     | 2.32 | 2.40 | 2.55 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 5                                     | 2.52 | 2.70 | 2.88 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 6                                     | 2.90 | 3.10 | 3.23 |      |
|                                                                     | SVSHE = 1, SVSMHRRRL = 7                                     | 2.90 | 3.10 | 3.23 |      |
| $t_{pd(SVSH)}$ SVS <sub>H</sub> propagation delay                   | SVSHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVSHFP = 1     |      | 2.5  |      | μs   |
|                                                                     | SVSHE = 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVSHFP = 0      |      | 20   |      |      |
| $t_{(SVSH)}$ SVS <sub>H</sub> on or off delay time                  | SVSHE = 0 → 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVSHFP = 1 |      | 12.5 |      | μs   |
|                                                                     | SVSHE = 0 → 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVSHFP = 0  |      | 100  |      |      |
| dV <sub>DVCC</sub> /dt DV <sub>CC</sub> rise time                   |                                                              | 0    |      | 1000 | V/s  |

(1) The SVS<sub>H</sub> settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and use.

## PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                            | TEST CONDITIONS                                              | MIN  | TYP  | MAX  | UNIT |
|----------------------------------------------------------------------|--------------------------------------------------------------|------|------|------|------|
| $I_{(SVMH)}$ SVM <sub>H</sub> current consumption                    | SVMHE = 0, DV <sub>CC</sub> = 3.6 V                          |      | 0    |      | nA   |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 0              |      | 200  |      | nA   |
|                                                                      | SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 1              |      | 1.5  |      | μA   |
| $V_{(SVMH)}$ SVM <sub>H</sub> on or off voltage level <sup>(1)</sup> | SVMHE = 1, SVSMHRRRL = 0                                     | 1.62 | 1.74 | 1.85 | V    |
|                                                                      | SVMHE = 1, SVSMHRRRL = 1                                     | 1.88 | 1.94 | 2.07 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 2                                     | 2.07 | 2.14 | 2.28 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 3                                     | 2.20 | 2.30 | 2.42 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 4                                     | 2.32 | 2.40 | 2.55 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 5                                     | 2.52 | 2.70 | 2.88 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 6                                     | 2.90 | 3.10 | 3.23 |      |
|                                                                      | SVMHE = 1, SVSMHRRRL = 7                                     | 2.90 | 3.10 | 3.23 |      |
|                                                                      | SVMHE = 1, SVMHOVPE = 1                                      |      | 3.75 |      |      |
| $t_{pd(SVMH)}$ SVM <sub>H</sub> propagation delay                    | SVMHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVMHFP = 1     |      | 2.5  |      | μs   |
|                                                                      | SVMHE = 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVMHFP = 0      |      | 20   |      |      |
| $t_{(SVMH)}$ SVM <sub>H</sub> on or off delay time                   | SVMHE = 0 → 1, dV <sub>DVCC</sub> /dt = 10 mV/μs, SVMHFP = 1 |      | 12.5 |      | μs   |
|                                                                      | SVMHE = 0 → 1, dV <sub>DVCC</sub> /dt = 1 mV/μs, SVMHFP = 0  |      | 100  |      |      |

(1) The SVM<sub>H</sub> settings available depend on the V<sub>CORE</sub> (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and use.

## PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                          | TEST CONDITIONS                                              | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------|--------------------------------------------------------------|-----|------|-----|------|
| $I_{(SVSL)}$ SVS <sub>L</sub> current consumption  | SVSLE = 0, PMMCOREV = 2                                      |     | 0    |     | nA   |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0                          |     | 200  |     | nA   |
|                                                    | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1                          |     | 1.5  |     | μA   |
| $t_{pd(SVSL)}$ SVS <sub>L</sub> propagation delay  | SVSLE = 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVSLFP = 1     |     | 2.5  |     | μs   |
|                                                    | SVSLE = 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVSLFP = 0      |     | 20   |     |      |
| $t_{(SVSL)}$ SVS <sub>L</sub> on or off delay time | SVSLE = 0 → 1, dV <sub>CORE</sub> /dt = 10 mV/μs, SVSLFP = 1 |     | 12.5 |     | μs   |
|                                                    | SVSLE = 0 → 1, dV <sub>CORE</sub> /dt = 1 mV/μs, SVSLFP = 0  |     | 100  |     |      |



## PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                                       | TEST CONDITIONS                                                        | MIN | TYP  | MAX | UNIT |
|----------------|---------------------------------------|------------------------------------------------------------------------|-----|------|-----|------|
| $I_{(SVML)}$   | SVM <sub>L</sub> current consumption  | SVMLE = 0, PMMCOREV = 2                                                |     | 0    |     | nA   |
|                |                                       | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0                                    |     | 200  |     | nA   |
|                |                                       | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1                                    |     | 1.5  |     | μA   |
| $t_{pd(SVML)}$ | SVM <sub>L</sub> propagation delay    | SVMLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$ , SVMLFP = 1     |     | 2.5  |     | μs   |
|                |                                       | SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$ , SVMLFP = 0      |     | 20   |     |      |
| $t_{(SVML)}$   | SVM <sub>L</sub> on or off delay time | SVMLE = 0 → 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$ , SVMLFP = 1 |     | 12.5 |     | μs   |
|                |                                       | SVMLE = 0 → 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$ , SVMLFP = 0  |     | 100  |     |      |

## Wake-Up From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                  |                                                                                      | TEST CONDITIONS                                                     |                                       | MIN | TYP | MAX | UNIT |
|----------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------|---------------------------------------|-----|-----|-----|------|
| t <sub>WAKE-UP-FAST</sub>  | Wake-up time from LPM2, LPM3, or LPM4 to active mode <sup>(1)</sup>                  | PMMCOREV = SVSMLRRL = n<br>(where n = 0, 1, 2, or 3),<br>SVSLFP = 1 | f <sub>MCLK</sub> ≥ 4.0 MHz           |     | 3.5 | 7.5 | μs   |
|                            |                                                                                      |                                                                     | 1.0 MHz < f <sub>MCLK</sub> < 4.0 MHz |     | 4.5 | 9   |      |
| t <sub>WAKE-UP-SLOW</sub>  | Wake-up time from LPM2, LPM3 or LPM4 to active mode <sup>(2)</sup>                   | PMMCOREV = SVSMLRRL = n<br>(where n = 0, 1, 2, or 3),<br>SVSLFP = 0 |                                       |     | 150 | 175 | μs   |
| t <sub>WAKE-UP-LPM5</sub>  | Wake-up time from LPM4.5 to active mode <sup>(3)</sup>                               |                                                                     |                                       |     | 2   | 3   | ms   |
| t <sub>WAKE-UP-RESET</sub> | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode <sup>(3)</sup> |                                                                     |                                       |     | 2   | 3   | ms   |

- (1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS<sub>L</sub>) and low side monitor (SVM<sub>L</sub>). Fastest wakeup times are possible with SVS<sub>L</sub> and SVM<sub>L</sub> in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS<sub>L</sub> and SVM<sub>L</sub> while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
- (2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS<sub>L</sub>) and low side monitor (SVM<sub>L</sub>). In this case, the SVS<sub>L</sub> and SVM<sub>L</sub> are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS<sub>L</sub> and SVM<sub>L</sub> while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
- (3) This value represents the time from the wakeup event to the reset vector execution.

## Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 | TEST CONDITIONS                                                       | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------|-----------------------------------------------------------------------|-----------------|------------------|-----|-----|-----|------|
| f <sub>TA</sub> Timer_A input clock frequency             | Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ± 10%    | 1.8 V           | 1.62 V to 1.8 V  |     |     | 25  | MHz  |
|                                                           |                                                                       | 3.0 V           | 1.62 V to 1.98 V |     |     | 25  |      |
| t <sub>TA,cap</sub> Timer_A capture timing <sup>(1)</sup> | All capture inputs,<br>Minimum pulse duration<br>required for capture | 1.8 V           | 1.62 V to 1.8 V  | 20  |     |     | ns   |
|                                                           |                                                                       | 3.0 V           | 1.62 V to 1.98 V | 20  |     |     |      |

- (1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than t<sub>TA,cap</sub>.

## Timer\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 | TEST CONDITIONS                                                       | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------|-----------------------------------------------------------------------|-----------------|------------------|-----|-----|-----|------|
| f <sub>TB</sub> Timer_B input clock frequency             | Internal: SMCLK, ACLK<br>External: TBCLK<br>Duty cycle = 50% ± 10%    | 1.8 V           | 1.62 V to 1.8 V  |     |     | 25  | MHz  |
|                                                           |                                                                       | 3.0 V           | 1.62 V to 1.98 V |     |     | 25  |      |
| t <sub>TB,cap</sub> Timer_B capture timing <sup>(1)</sup> | All capture inputs,<br>Minimum pulse duration<br>required for capture | 1.8 V           | 1.62 V to 1.8 V  | 20  |     |     | ns   |
|                                                           |                                                                       | 3.0 V           | 1.62 V to 1.98 V | 20  |     |     |      |

- (1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than t<sub>TB,cap</sub>.

## USCI (UART Mode), Recommended Operating Conditions

| PARAMETER                                                              | CONDITIONS                                                        | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|------------------------------------------------------------------------|-------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                           | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| f <sub>BITCLK</sub> BITCLK clock frequency (equals baud rate in MBaud) |                                                                   |                 |     | 1                   |     | MHz  |

## USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP | MAX | UNIT |
|----------------------------------------------------------|-----------------|-----------------|------------------|-----|-----|-----|------|
| t <sub>r</sub> UART receive deglitch time <sup>(1)</sup> |                 | 1.8 V           | 1.62 V to 1.80 V | 50  |     | 600 | ns   |
|                                                          |                 | 3.0 V           | 1.62 V to 1.98 V | 50  |     | 600 |      |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

## USCI (SPI Master Mode), Recommended Operating Conditions

| PARAMETER                                    | CONDITIONS                                         | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|----------------------------------------------|----------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |

## USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see Note <sup>(1)</sup>, [Figure 13](#) and [Figure 14](#))

| PARAMETER                                                        | TEST CONDITIONS                                                     | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP                 | MAX | UNIT |
|------------------------------------------------------------------|---------------------------------------------------------------------|-----------------|------------------|-----|---------------------|-----|------|
| f <sub>USCI</sub> USCI input clock frequency                     | SMCLK or ACLK,<br>Duty cycle = 50% ± 10%                            |                 |                  |     | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>SU,MI</sub> SOMI input data setup time                    | PMMCOREV = 0                                                        | 1.8 V           | 1.62 V to 1.80 V | 55  |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | 55  |                     |     |      |
|                                                                  | PMMCOREV = 3                                                        | 2.4 V           | 1.62 V to 1.98 V | 35  |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | 35  |                     |     |      |
| t <sub>HD,MI</sub> SOMI input data hold time                     | PMMCOREV = 0                                                        | 1.8 V           | 1.62 V to 1.80 V | 0   |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | 0   |                     |     |      |
|                                                                  | PMMCOREV = 3                                                        | 2.4 V           | 1.62 V to 1.98 V | 0   |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | 0   |                     |     |      |
| t <sub>VALID,MO</sub> SIMO output data valid time <sup>(2)</sup> | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF,<br>PMMCOREV = 0 | 1.8 V           | 1.62 V to 1.80 V |     |                     | 20  | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V |     |                     | 20  |      |
|                                                                  | UCLK edge to SIMO valid,<br>C <sub>L</sub> = 20 pF,<br>PMMCOREV = 3 | 2.4 V           | 1.62 V to 1.98 V |     |                     | 16  | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V |     |                     | 16  |      |
| t <sub>HD,MO</sub> SIMO output data hold time <sup>(3)</sup>     | C <sub>L</sub> = 20 pF,<br>PMMCOREV = 0                             | 1.8 V           | 1.62 V to 1.80 V | -10 |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | -10 |                     |     |      |
|                                                                  | C <sub>L</sub> = 20 pF,<br>PMMCOREV = 3                             | 2.4 V           | 1.62 V to 1.98 V | -10 |                     |     | ns   |
|                                                                  |                                                                     | 3.0 V           | 1.62 V to 1.98 V | -10 |                     |     |      |

- (1) f<sub>UCxCLK</sub> = 1/2t<sub>LO/HI</sub> with t<sub>LO/HI</sub> ≥ max(t<sub>VALID,MO</sub>(USCI) + t<sub>SU,SI</sub>(Slave), t<sub>SU,MI</sub>(USCI) + t<sub>VALID,SO</sub>(Slave)).

For the slave's parameters t<sub>SU,SI</sub>(Slave) and t<sub>VALID,SO</sub>(Slave) see the SPI parameters of the attached slave.

- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 13](#) and [Figure 14](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 13](#) and [Figure 14](#).

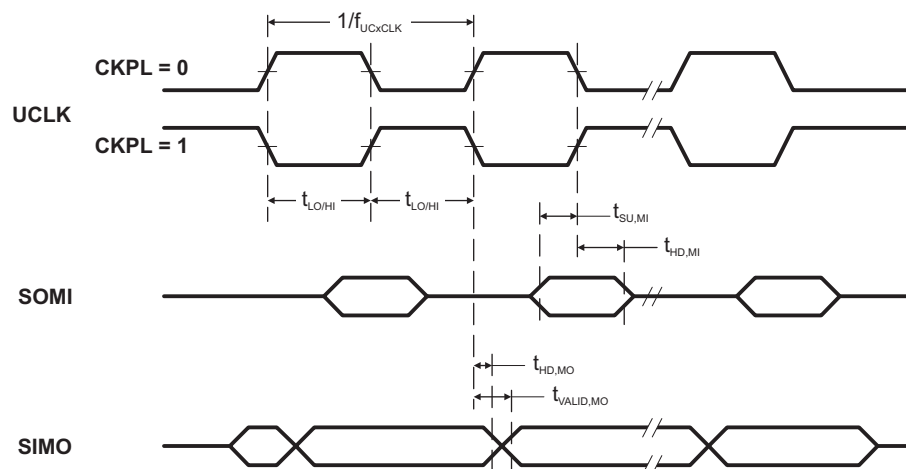


Figure 13. SPI Master Mode, CKPH = 0

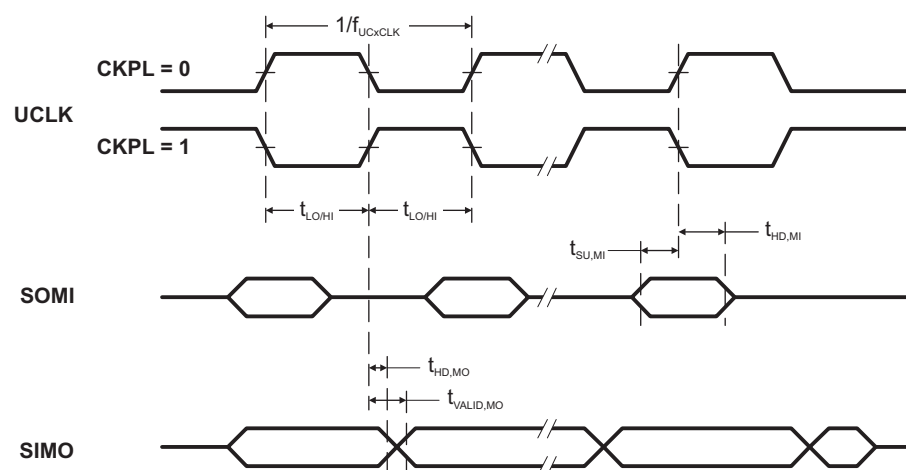


Figure 14. SPI Master Mode, CKPH = 1

## USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)  
(see Note <sup>(1)</sup>, [Figure 15](#) and [Figure 16](#))

| PARAMETER                                                       | TEST CONDITIONS                                               | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------|---------------------------------------------------------------|-----------------|------------------|-----|-----|-----|------|
| $t_{STE,LEAD}$ STE lead time, STE low to clock                  | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V | 12  |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 12  |     |     |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V | 10  |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 10  |     |     |      |
| $t_{STE,LAG}$ STE lag time, Last clock to STE high              | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V | 6   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 6   |     |     |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V | 6   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 6   |     |     |      |
| $t_{STE,ACC}$ STE access time, STE low to SOMI data out         | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V |     |     | 65  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 65  |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V |     |     | 45  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 45  |      |
| $t_{STE,DIS}$ STE disable time, STE high to SOMI high impedance | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V |     |     | 35  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 35  |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V |     |     | 25  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 25  |      |
| $t_{SU,SI}$ SIMO input data setup time                          | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V | 5   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 5   |     |     |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V | 5   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 5   |     |     |      |
| $t_{HD,SI}$ SIMO input data hold time                           | PMMCOREV = 0                                                  | 1.8 V           | 1.62 V to 1.80 V | 5   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 5   |     |     |      |
|                                                                 | PMMCOREV = 3                                                  | 2.4 V           | 1.62 V to 1.98 V | 5   |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 5   |     |     |      |
| $t_{VALID,SO}$ SOMI output data valid time <sup>(2)</sup>       | UCLK edge to SOMI valid, C <sub>L</sub> = 20 pF, PMMCOREV = 0 | 1.8 V           | 1.62 V to 1.80 V |     |     | 75  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 75  |      |
|                                                                 | UCLK edge to SOMI valid, C <sub>L</sub> = 20 pF, PMMCOREV = 3 | 2.4 V           | 1.62 V to 1.98 V |     |     | 50  | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V |     |     | 50  |      |
| $t_{HD,SO}$ SOMI output data hold time <sup>(3)</sup>           | C <sub>L</sub> = 20 pF, PMMCOREV = 0                          | 1.8 V           | 1.62 V to 1.80 V | 18  |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 18  |     |     |      |
|                                                                 | C <sub>L</sub> = 20 pF, PMMCOREV = 3                          | 2.4 V           | 1.62 V to 1.98 V | 10  |     |     | ns   |
|                                                                 |                                                               | 3.0 V           | 1.62 V to 1.98 V | 10  |     |     |      |

- (1)  $f_{UCXCLK} = 1/2t_{LO/HI}$  with  $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$ .  
For the master's parameters  $t_{SU,MI(Master)}$  and  $t_{VALID,MO(Master)}$  see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 13](#) and [Figure 14](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 13](#) and [Figure 14](#).

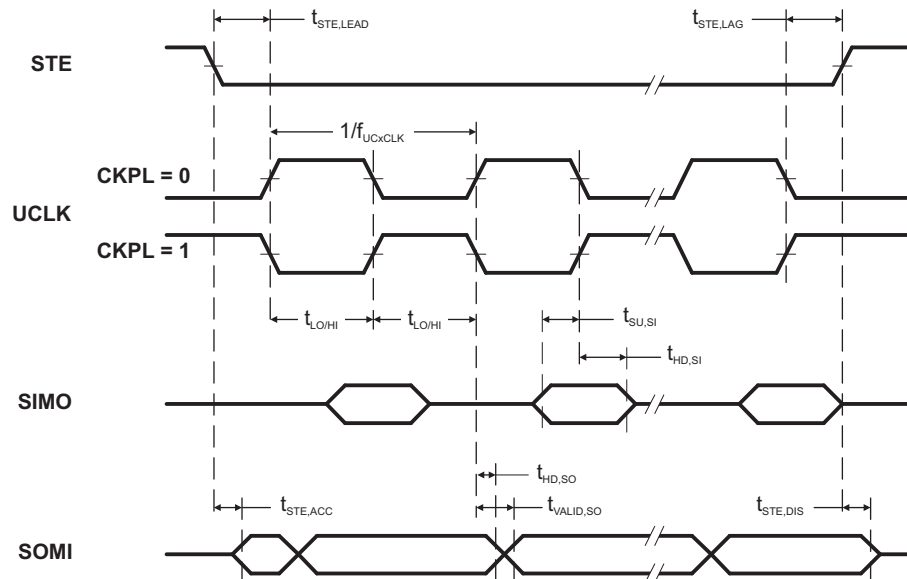


Figure 15. SPI Slave Mode, CKPH = 0

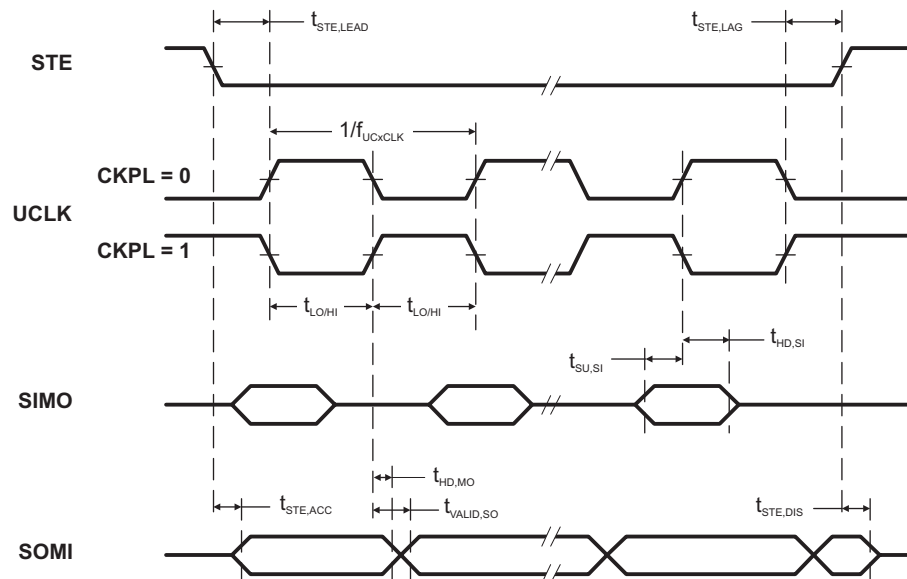


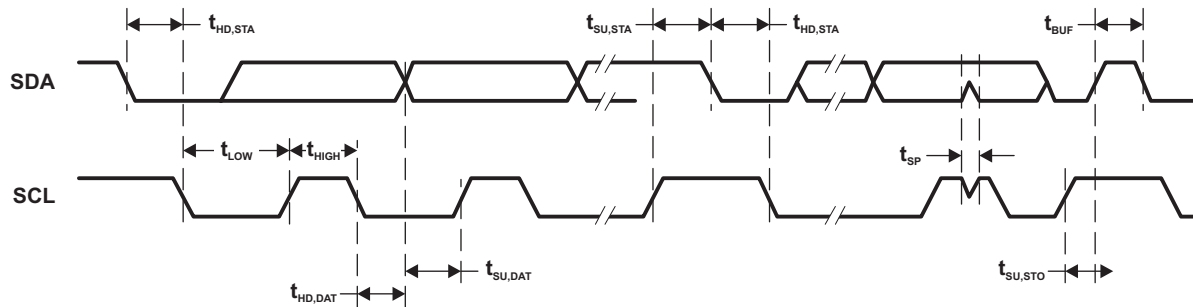
Figure 16. SPI Slave Mode, CKPH = 1

## USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 17](#))

| PARAMETER           | TEST CONDITIONS                                     | V <sub>CC</sub> | V <sub>IO</sub> <sup>(1)</sup> | MIN | TYP | MAX                 | UNIT |
|---------------------|-----------------------------------------------------|-----------------|--------------------------------|-----|-----|---------------------|------|
| f <sub>USCI</sub>   | USCI input clock frequency                          |                 |                                |     |     | f <sub>SYSTEM</sub> | MHz  |
| f <sub>SCL</sub>    | SCL clock frequency                                 | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 0   |     | 400                 | kHz  |
| t <sub>HD,STA</sub> | Hold time (repeated) START                          | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 4.0 |     |                     | μs   |
|                     |                                                     |                 |                                | 0.6 |     |                     |      |
| t <sub>SU,STA</sub> | Setup time for a repeated START                     | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 4.7 |     |                     | μs   |
|                     |                                                     |                 |                                | 0.6 |     |                     |      |
| t <sub>HD,DAT</sub> | Data hold time                                      | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 0   |     |                     | ns   |
| t <sub>SU,DAT</sub> | Data setup time                                     | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 250 |     |                     | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP                                 | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 4.0 |     |                     | μs   |
|                     |                                                     |                 |                                | 0.6 |     |                     |      |
| t <sub>SP</sub>     | Pulse duration of spikes suppressed by input filter | 2.2 V, 3 V      | 1.62 V to 1.98 V               | 50  |     | 600                 | ns   |

(1) In all test conditions, V<sub>IO</sub> ≤ V<sub>CC</sub>



**Figure 17. I2C Mode Timing**

## 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER            |                                                                                   | TEST CONDITIONS                                                                                                                                                             | V <sub>CC</sub> | MIN | TYP | MAX              | UNIT |
|----------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|------------------|------|
| AV <sub>CC</sub>     | Analog supply voltage                                                             | AV <sub>CC</sub> and DV <sub>CC</sub> are connected together, AV <sub>SS</sub> and DV <sub>SS</sub> are connected together, V <sub>(AVSS)</sub> = V <sub>(DVSS)</sub> = 0 V |                 | 1.8 |     | 3.6              | V    |
| V <sub>(Ax)</sub>    | Analog input voltage range <sup>(2)</sup>                                         | All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals                                                                                                                  |                 | 0   |     | AV <sub>CC</sub> | V    |
| I <sub>ADC10_A</sub> | Operating supply current into AVCC terminal, REF module and reference buffer off  | f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00                                                                   | 2.2 V           |     | 60  | 100              | μA   |
|                      |                                                                                   |                                                                                                                                                                             | 3 V             |     | 75  | 110              |      |
|                      | Operating supply current into AVCC terminal, REF module on, reference buffer on   | f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01                                                                   | 3 V             |     | 113 | 150              | μA   |
|                      | Operating supply current into AVCC terminal, REF module off, reference buffer on  | f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V                                                     | 3 V             |     | 105 | 140              | μA   |
|                      | Operating supply current into AVCC terminal, REF module off, reference buffer off | f <sub>ADC10CLK</sub> = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V                                                     | 3 V             |     | 70  | 110              | μA   |
| C <sub>I</sub>       | Input capacitance                                                                 | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad                                                       | 2.2 V           |     | 3.5 |                  | pF   |
| R <sub>I</sub>       | Input MUX ON resistance                                                           | AV <sub>CC</sub> > 2 V, 0 V ≤ V <sub>Ax</sub> ≤ AV <sub>CC</sub>                                                                                                            |                 |     |     | 36               | kΩ   |
|                      |                                                                                   | 1.8 V < AV <sub>CC</sub> < 2 V, 0 V ≤ V <sub>Ax</sub> ≤ AV <sub>CC</sub>                                                                                                    |                 |     |     | 96               |      |

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results. The external reference voltage requires decoupling capacitors. See <sup>0</sup>.

## 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                            | TEST CONDITIONS                                                                                           | V <sub>CC</sub> | MIN  | TYP | MAX | UNIT |
|-----------------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----------------|------|-----|-----|------|
| f <sub>ADC10CLK</sub> | Input clock frequency                      | For specified performance of ADC10_A linearity parameters                                                 | 2.2 V, 3 V      | 0.45 | 5   | 5.5 | MHz  |
| f <sub>ADC10OSC</sub> | Internal ADC10_A oscillator <sup>(1)</sup> | ADC10DIV = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>                                               | 2.2 V, 3 V      | 4.2  | 4.8 | 5.4 | MHz  |
| t <sub>CONVERT</sub>  | Conversion time                            | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode<br>f <sub>ADC10OSC</sub> = 4 MHz to 5 MHz | 2.2 V, 3 V      | 2.4  |     | 3.0 | μs   |
|                       |                                            | External f <sub>ADC10CLK</sub> from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0                                    |                 |      | (2) |     |      |
| t <sub>ADC10ON</sub>  | Turn on settling time of the ADC           | See <sup>(3)</sup>                                                                                        |                 |      |     | 100 | ns   |
| t <sub>Sample</sub>   | Sampling time                              | R <sub>S</sub> = 1000 Ω, R <sub>I</sub> = 96 k Ω, C <sub>I</sub> = 3.5 pF <sup>(4)</sup>                  | 1.8 V           | 3    |     |     | μs   |
|                       |                                            |                                                                                                           | 3.0 V           | 1    |     |     | μs   |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) 12 × ADC10DIV × 1/f<sub>ADC10CLK</sub>

(3) The condition is that the error in a conversion started after t<sub>ADC10ON</sub> is less than ±0.5 LSB. The reference and input signal are already settled.

(4) Approximately eight Tau (τ) are needed to get an error of less than ±0.5 LSB



## 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER      |                              | TEST CONDITIONS                                                                                                                                                                                                      | V <sub>CC</sub> | MIN | TYP  | MAX  | UNIT |
|----------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|------|------|
| E <sub>I</sub> | Integral linearity error     | $1.4\text{ V} \leq (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq 1.6\text{ V}$                                                                                                             | 2.2 V, 3 V      |     |      | ±1.0 | LSB  |
|                |                              | $1.6\text{ V} < (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq V_{\text{AVCC}}$                                                                                                             |                 |     |      | ±1.0 |      |
| E <sub>D</sub> | Differential linearity error | $(V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})$ ,<br>C <sub>VREF+</sub> = 20 pF                                                      | 2.2 V, 3 V      |     |      | ±1.0 | LSB  |
| E <sub>O</sub> | Offset error                 | $(V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})$ ,<br>Internal impedance of source R <sub>S</sub> < 100 Ω, C <sub>VREF+</sub> = 20 pF | 2.2 V, 3 V      |     |      | ±1.0 | LSB  |
| E <sub>G</sub> | Gain error                   | $(V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})$ ,<br>C <sub>VREF+</sub> = 20 pF                                                      | 2.2 V, 3 V      |     |      | ±1.0 | LSB  |
| E <sub>T</sub> | Total unadjusted error       | $(V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})_{\text{min}} \leq (V_{\text{eREF+}} - V_{\text{REF-}}/N_{\text{eREF-}})$ ,<br>C <sub>VREF+</sub> = 20 pF                                                      | 2.2 V, 3 V      |     | ±1.0 | ±2.0 | LSB  |

## REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                    |                                               | TEST CONDITIONS                                                                                                                                                         | V <sub>CC</sub> | MIN | TYP | MAX               | UNIT |
|----------------------------------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----|-----|-------------------|------|
| V <sub>eREF+</sub>                           | Positive external reference voltage input     | $V_{\text{eREF+}} > V_{\text{REF-}}/N_{\text{eREF-}}$ <sup>(2)</sup>                                                                                                    |                 | 1.4 |     | V <sub>AVCC</sub> | V    |
| V <sub>eREF-</sub>                           | Negative external reference voltage input     | $V_{\text{eREF+}} > V_{\text{REF-}}/N_{\text{eREF-}}$ <sup>(3)</sup>                                                                                                    |                 | 0   |     | 1.2               | V    |
| (V <sub>eREF+</sub> – V <sub>eREF-</sub> )   | Differential external reference voltage input | $V_{\text{eREF+}} > V_{\text{REF-}}/N_{\text{eREF-}}$ <sup>(4)</sup>                                                                                                    |                 | 1.4 |     | V <sub>AVCC</sub> | V    |
| I <sub>VeREF+</sub> ,<br>I <sub>VeREF-</sub> | Static input current                          | $1.4\text{ V} \leq V_{\text{eREF+}} \leq V_{\text{AVCC}}$ , V <sub>eREF-</sub> = 0 V,<br>f <sub>ADC10CLK</sub> = 5 MHz, ADC10SHTx = 0x0001,<br>Conversion rate 200 ksps | 2.2 V, 3 V      | -26 |     | 26                | μA   |
|                                              |                                               | $1.4\text{ V} \leq V_{\text{eREF+}} \leq V_{\text{AVCC}}$ , V <sub>eREF-</sub> = 0 V,<br>f <sub>ADC10CLK</sub> = 5 MHz, ADC10SHTx = 0x1000,<br>Conversion rate 20 ksps  | 2.2 V, 3 V      | -1  |     | 1                 | μA   |
| C <sub>VREF+</sub> ,<br>C <sub>VREF-</sub>   | Capacitance at VeREF+ or VeREF- terminal      | (5)                                                                                                                                                                     |                 | 10  |     |                   | μF   |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C<sub>I</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10\_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

## REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                            | TEST CONDITIONS                                                                                                                                                      | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT   |
|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-------|-------|--------|
| V <sub>REF+</sub>                    | REFVSEL = {2} for 2.5 V<br>REFON = 1                                                                                                                                 | 3 V             | 2.472 | 2.51  | 2.548 | V      |
|                                      | REFVSEL = {1} for 2.0 V<br>REFON = 1                                                                                                                                 | 3 V             | 1.96  | 1.99  | 2.02  |        |
|                                      | REFVSEL = {0} for 1.5 V<br>REFON = 1                                                                                                                                 | 2.2 V, 3 V      | 1.472 | 1.495 | 1.518 |        |
| AV <sub>CC(min)</sub>                | REFVSEL = {0} for 1.5 V                                                                                                                                              |                 | 2.2   |       |       | V      |
|                                      | REFVSEL = {1} for 2.0 V                                                                                                                                              |                 | 2.2   |       |       |        |
|                                      | REFVSEL = {2} for 2.5 V                                                                                                                                              |                 | 2.7   |       |       |        |
| I <sub>REF+</sub>                    | f <sub>ADC10CLK</sub> = 5.0 MHz<br>REFON = 1, REFBURST = 0,<br>REFVSEL = {2} for 2.5 V                                                                               | 3 V             |       | 18    | 24    | μA     |
|                                      | f <sub>ADC10CLK</sub> = 5.0 MHz<br>REFON = 1, REFBURST = 0,<br>REFVSEL = {1} for 2.0 V                                                                               | 3 V             |       | 15.5  | 21    | μA     |
|                                      | f <sub>ADC10CLK</sub> = 5.0 MHz<br>REFON = 1, REFBURST = 0,<br>REFVSEL = {0} for 1.5 V                                                                               | 3 V             |       | 13.5  | 21    | μA     |
| TC <sub>REF+</sub>                   | I <sub>VREF+</sub> = 0 A<br>REFVSEL = {0, 1, 2}, REFON = 1                                                                                                           |                 |       | 30    | 50    | ppm/°C |
| I <sub>SENSOR</sub>                  | REFON = 0, INCH = 0Ah,<br>ADC10ON = N A, T <sub>A</sub> = 30°C                                                                                                       | 2.2 V           |       | 20    | 22    | μA     |
|                                      |                                                                                                                                                                      | 3 V             |       | 20    | 22    |        |
| V <sub>SENSOR</sub>                  | See <sup>(5)</sup><br>ADC10ON = 1, INCH = 0Ah,<br>T <sub>A</sub> = 30°C                                                                                              | 2.2 V           |       | 770   |       | mV     |
|                                      |                                                                                                                                                                      | 3 V             |       | 770   |       |        |
| V <sub>MID</sub>                     | AVCC divider at channel 11<br>ADC10ON = 1, INCH = 0Bh,<br>V <sub>MID</sub> ≈ 0.5 × V <sub>AVCC</sub>                                                                 | 2.2 V           | 1.06  | 1.1   | 1.14  | V      |
|                                      |                                                                                                                                                                      | 3 V             | 1.46  | 1.5   | 1.54  |        |
| t <sub>SENSOR(sample)</sub>          | ADC10ON = 1, INCH = 0Ah,<br>Error of conversion result ≤ 1 LSB                                                                                                       |                 | 30    |       |       | μs     |
| t <sub>V<sub>MID</sub>(sample)</sub> | ADC10ON = 1, INCH = 0Bh,<br>Error of conversion result ≤ 1 LSB                                                                                                       |                 | 1     |       |       | μs     |
| PSRR <sub>DC</sub>                   | AV <sub>CC</sub> = AV <sub>CC(min)</sub> - AV <sub>CC(max)</sub><br>T <sub>A</sub> = 25 °C<br>REFVSEL = {0, 1, 2}, REFON = 1                                         |                 |       | 120   |       | μV/V   |
| PSRR <sub>AC</sub>                   | AV <sub>CC</sub> = AV <sub>CC(min)</sub> - AV <sub>CC(max)</sub><br>T <sub>A</sub> = 25 °C<br>f = 1 kHz, ΔV <sub>pp</sub> = 100 mV<br>REFVSEL = {0, 1, 2}, REFON = 1 |                 |       | 6.4   |       | mV/V   |
| t <sub>SETTLE</sub>                  | AV <sub>CC</sub> = AV <sub>CC(min)</sub> - AV <sub>CC(max)</sub><br>REFVSEL = {0, 1, 2}, REFON = 0 → 1                                                               |                 |       | 75    |       | μs     |

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

(3) Calculated using the box method: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C)).

(4) The sensor current I<sub>SENSOR</sub> is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I<sub>SENSOR</sub> is already included in I<sub>REF+</sub>.

(5) The temperature sensor offset can be significant. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.

(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t<sub>SENSOR(on)</sub>.

(7) The on-time t<sub>V<sub>MID</sub>(on)</sub> is included in the sampling time t<sub>V<sub>MID</sub>(sample)</sub>; no additional on time is needed.

(8) The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB.

## Comparator\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                                                                   | TEST CONDITIONS                                                                     | V <sub>CC</sub> | MIN                | TYP              | MAX                | UNIT   |
|------------------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------------|--------------------|------------------|--------------------|--------|
| V <sub>CC</sub>        | Supply voltage                                                                    |                                                                                     |                 | 1.8                |                  | 3.6                | V      |
| I <sub>AVCC_COMP</sub> | Comparator operating supply current into AVCC, Excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBR <sub>Sx</sub> = 00                                      | 1.8 V           |                    |                  | 38                 | μA     |
|                        |                                                                                   |                                                                                     | 2.2 V           |                    | 31               | 38                 |        |
|                        |                                                                                   |                                                                                     | 3 V             |                    | 32               | 39                 |        |
|                        |                                                                                   | CBPWRMD = 01, CBON = 1, CBR <sub>Sx</sub> = 00                                      | 2.2 V, 3 V      |                    | 10               | 17                 |        |
|                        |                                                                                   | CBPWRMD = 10, CBON = 1, CBR <sub>Sx</sub> = 00                                      | 2.2 V, 3 V      |                    | 0.2              | 0.85               |        |
| V <sub>REF</sub>       | Reference voltage level                                                           | CBREFL <sub>x</sub> = 01, CBREFACC = 0                                              | ≥ 1.8V          |                    | 1.44             | ±2.5%              | V      |
|                        |                                                                                   | CBREFL <sub>x</sub> = 10, CBREFACC = 0                                              | ≥ 2.2V          |                    | 1.92             | ±2.5%              |        |
|                        |                                                                                   | CBREFL <sub>x</sub> = 11, CBREFACC = 0                                              | ≥ 3.0V          |                    | 2.39             | ±2.5%              |        |
| I <sub>AVCC_REF</sub>  | Quiescent current of resistor ladder into AVCC, Including REF module current      | CBREFACC = 0, CBREFL <sub>x</sub> = 01, CBR <sub>Sx</sub> = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V      |                    | 17               | 22                 | μA     |
|                        |                                                                                   | CBREFACC = 1, CBREFL <sub>x</sub> = 01, CBR <sub>Sx</sub> = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V      |                    | 33               | 40                 | μA     |
| V <sub>IC</sub>        | Common mode input range                                                           |                                                                                     |                 | 0                  |                  | V <sub>CC</sub> -1 | V      |
| V <sub>OFFSET</sub>    | Input offset voltage                                                              | CBPWRMD = 00                                                                        |                 | -20                |                  | 20                 | mV     |
|                        |                                                                                   | CBPWRMD = 01, 10                                                                    |                 | -10                |                  | 10                 | mV     |
| C <sub>IN</sub>        | Input capacitance                                                                 |                                                                                     |                 |                    | 5                |                    | pF     |
| R <sub>SIN</sub>       | Series input resistance                                                           | ON - switch closed                                                                  |                 |                    | 3                | 4                  | kΩ     |
|                        |                                                                                   | OFF - switch opened                                                                 |                 |                    | 50               |                    | MΩ     |
| t <sub>PD</sub>        | Propagation delay, response time                                                  | CBPWRMD = 00, CBF = 0                                                               |                 |                    |                  | 450                | ns     |
|                        |                                                                                   | CBPWRMD = 01, CBF = 0                                                               |                 |                    |                  | 600                | ns     |
|                        |                                                                                   | CBPWRMD = 10, CBF = 0                                                               |                 |                    |                  | 50                 | μs     |
| t <sub>PD,filter</sub> | Propagation delay with filter active                                              | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 00                            |                 | 0.35               | 0.6              | 1.5                | μs     |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 01                            |                 | 0.6                | 1.0              | 1.8                | μs     |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 10                            |                 | 1.0                | 1.8              | 3.4                | μs     |
|                        |                                                                                   | CBPWRMD = 00, CBON = 1, CBF = 1, CBF <sub>DLY</sub> = 11                            |                 | 1.8                | 3.4              | 6.5                | μs     |
| t <sub>EN_CMP</sub>    | Comparator enable time                                                            | CBON = 0 to CBON = 1, CBPWRMD = 00, 01                                              |                 |                    | 1                | 2                  | μs     |
| t <sub>EN_REF</sub>    | Resistor reference enable time                                                    | CBON = 0 to CBON = 1                                                                |                 |                    | 1.0              | 1.5                | μs     |
| T <sub>CREF</sub>      | Temperature coefficient reference                                                 |                                                                                     |                 |                    |                  | 50                 | ppm/°C |
| V <sub>CB_REF</sub>    | Reference voltage for a given tap                                                 | VIN = reference into resistor ladder, n = 0 to 31                                   |                 | VIN × (n+0.5) / 32 | VIN × (n+1) / 32 | VIN × (n+1.5) / 32 | V      |

## Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                               |                                                                                   | TEST CONDITIONS       | MIN             | TYP             | MAX | UNIT   |
|-----------------------------------------|-----------------------------------------------------------------------------------|-----------------------|-----------------|-----------------|-----|--------|
| DV <sub>CC(PGM/ERASE)</sub>             | Program and erase supply voltage                                                  |                       | 1.8             |                 | 3.6 | V      |
| I <sub>PGM</sub>                        | Average supply current from DVCC during program                                   |                       |                 | 3               | 5   | mA     |
| I <sub>ERASE</sub>                      | Average supply current from DVCC during erase                                     |                       |                 | 6               | 11  | mA     |
| I <sub>MERASE</sub> , I <sub>BANK</sub> | Average supply current from DVCC during mass erase or bank erase                  |                       |                 | 6               | 11  | mA     |
| t <sub>CPT</sub>                        | Cumulative program time                                                           | See <sup>(1)</sup>    |                 |                 | 16  | ms     |
|                                         | Program and erase endurance                                                       |                       | 10 <sup>4</sup> | 10 <sup>5</sup> |     | cycles |
| t <sub>Retention</sub>                  | Data retention duration                                                           | T <sub>J</sub> = 25°C | 100             |                 |     | years  |
| t <sub>Word</sub>                       | Word or byte program time                                                         | See <sup>(2)</sup>    | 64              |                 | 85  | μs     |
| t <sub>Block, 0</sub>                   | Block program time for first byte or word                                         | See <sup>(2)</sup>    | 49              |                 | 65  | μs     |
| t <sub>Block, 1–(N–1)</sub>             | Block program time for each additional byte or word, except for last byte or word | See <sup>(2)</sup>    | 37              |                 | 49  | μs     |
| t <sub>Block, N</sub>                   | Block program time for last byte or word                                          | See <sup>(2)</sup>    | 55              |                 | 73  | μs     |
| t <sub>Erase</sub>                      | Erase time for segment, mass erase, and bank erase when available                 | See <sup>(2)</sup>    | 23              |                 | 32  | ms     |
| f <sub>MCLK,MGR</sub>                   | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)           |                       | 0               |                 | 1   | MHz    |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.

(2) These values are hardwired into the flash controller's state machine.

## JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER             |                                                                                      | V <sub>CC</sub> | V <sub>IO</sub>  | MIN   | TYP | MAX | UNIT |
|-----------------------|--------------------------------------------------------------------------------------|-----------------|------------------|-------|-----|-----|------|
| f <sub>SBW</sub>      | Spy-Bi-Wire input frequency                                                          | 2.2 V, 3 V      | 1.62 V to 1.98 V | 0     |     | 20  | MHz  |
| t <sub>SBW,Low</sub>  | Spy-Bi-Wire low clock pulse length                                                   | 2.2 V, 3 V      | 1.62 V to 1.98 V | 0.025 |     | 15  | μs   |
| t <sub>SBW,En</sub>   | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) <sup>(1)</sup> | 2.2 V, 3 V      | 1.62 V to 1.98 V |       |     | 1   | μs   |
| t <sub>SBW,Rst</sub>  | Spy-Bi-Wire return to normal operation time                                          | 2.2 V, 3 V      | 1.62 V to 1.98 V | 15    |     | 100 | μs   |
| f <sub>TCK</sub>      | TCK input frequency for 4-wire JTAG <sup>(2)</sup>                                   | 2.2 V           | 1.62 V to 1.98 V | 0     |     | 5   | MHz  |
|                       |                                                                                      | 3 V             | 1.62 V to 1.98 V | 0     |     | 10  | MHz  |
| R <sub>Internal</sub> | Internal pulldown resistance on TEST                                                 | 2.2 V, 3 V      | 1.62 V to 1.98 V | 45    | 60  | 80  | kΩ   |

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.

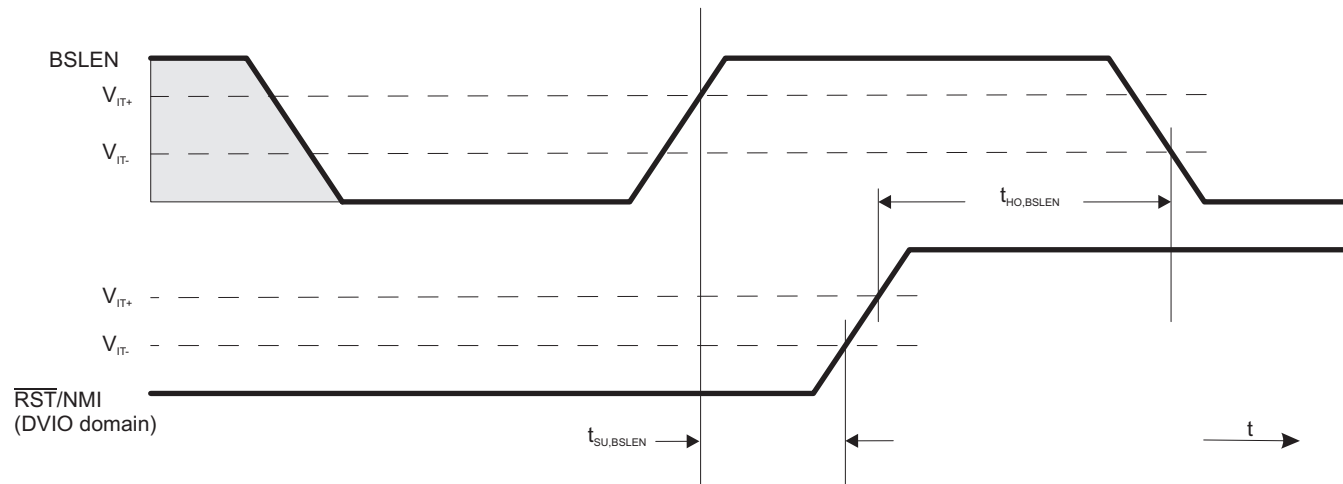
## DVIO BSL Entry

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                              | V <sub>CC</sub> | V <sub>IO</sub>  | MIN | TYP | MAX | UNIT |
|----------------------|--------------------------------------------------------------|-----------------|------------------|-----|-----|-----|------|
| t <sub>SU, BSL</sub> | Setup time BSL to $\overline{\text{RST/NMI}}$ <sup>(1)</sup> | 2.2 V, 3 V      | 1.62 V to 1.98 V | 100 |     |     | ns   |
| t <sub>HO, BSL</sub> | Hold time BSL to $\overline{\text{RST/NMI}}$ <sup>(2)</sup>  | 2.2 V, 3 V      | 1.62 V to 1.98 V | 350 |     |     | μs   |

(1) AVCC, DVCC, DVIO stable and within specification.

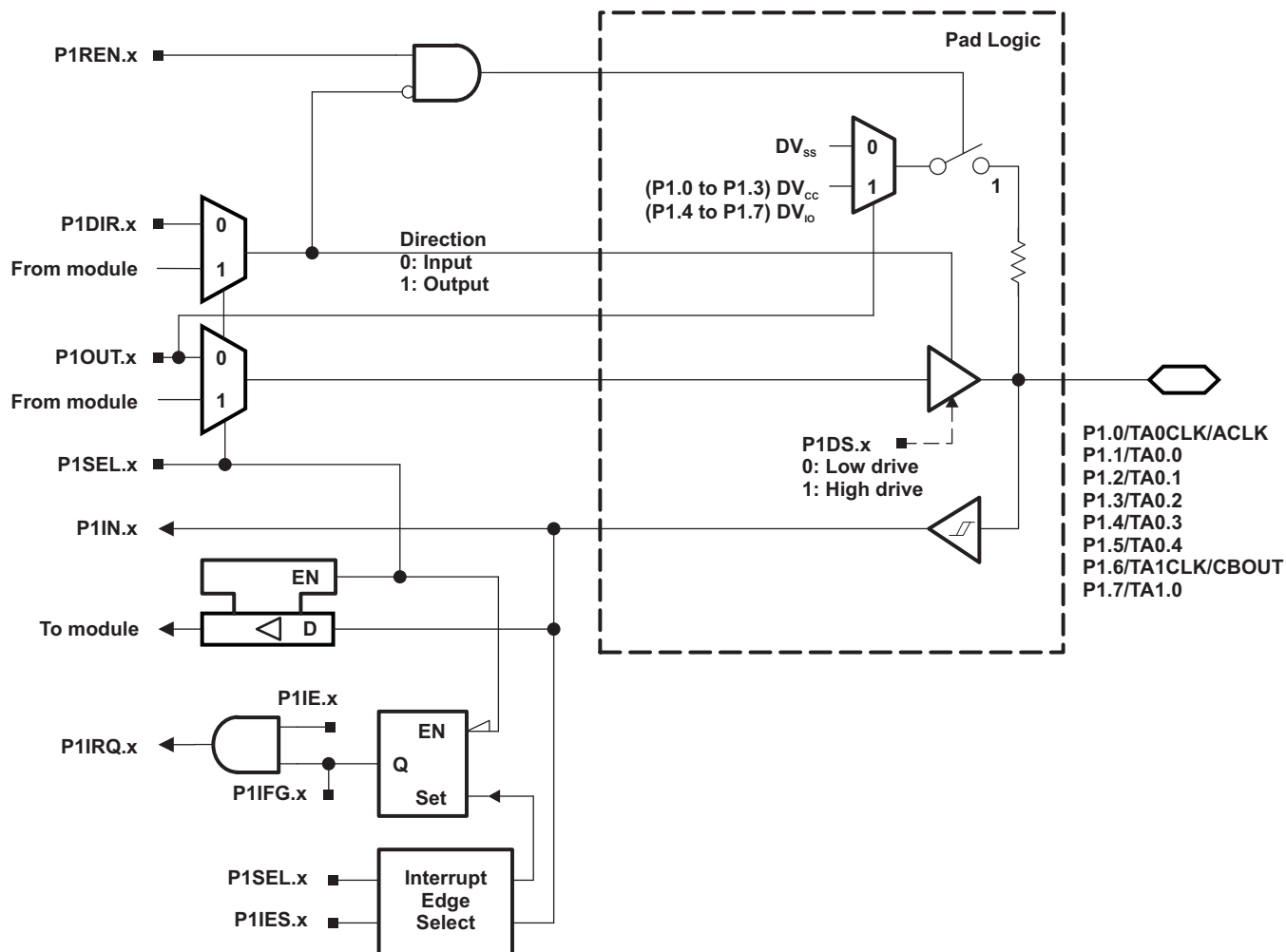
(2) BSL must remain logically high long enough for the boot code to detect its level and enter the BSL sequence. After the minimum hold time is achieved, BSL is a don't care.



**Figure 18. DVIO BSL Entry Timing**

## INPUT/OUTPUT SCHEMATICS

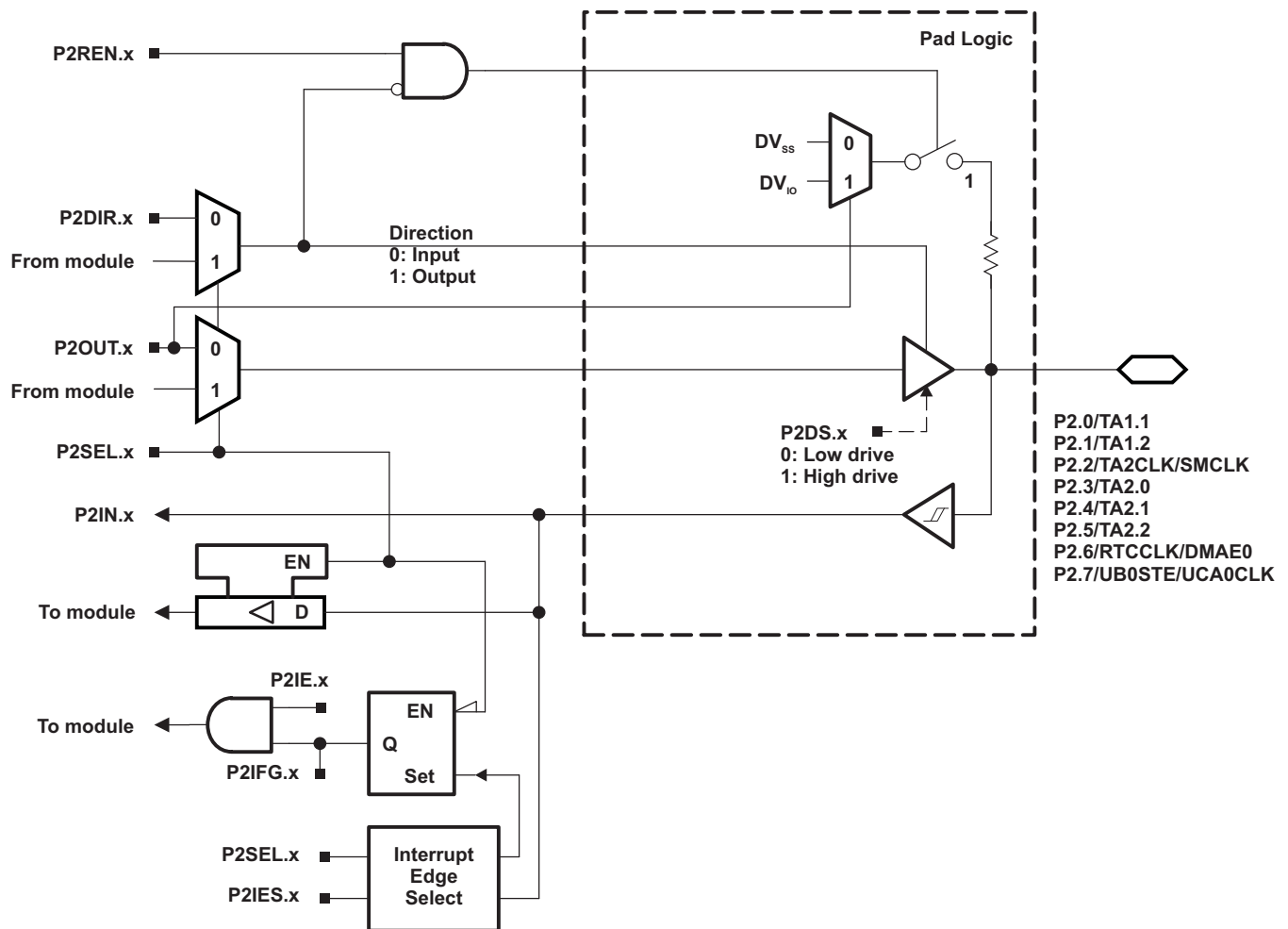
### Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger



**Table 48. Port P1 (P1.0 to P1.7) Pin Functions**

| PIN NAME (P1.x)   | x | FUNCTION           | CONTROL BITS AND SIGNALS |         |
|-------------------|---|--------------------|--------------------------|---------|
|                   |   |                    | P1DIR.x                  | P1SEL.x |
| P1.0/TA0CLK/ACLK  | 0 | P1.0 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0CLK             | 0                        | 1       |
|                   |   | ACLK               | 1                        | 1       |
| P1.1/TA0.0        | 1 | P1.1 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0.CCI0A          | 0                        | 1       |
|                   |   | TA0.0              | 1                        | 1       |
| P1.2/TA0.1        | 2 | P1.2 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0.CCI1A          | 0                        | 1       |
|                   |   | TA0.1              | 1                        | 1       |
| P1.3/TA0.2        | 3 | P1.3 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0.CCI2A          | 0                        | 1       |
|                   |   | TA0.2              | 1                        | 1       |
| P1.4/TA0.3        | 4 | P1.4 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0.CCI3A          | 0                        | 1       |
|                   |   | TA0.3              | 1                        | 1       |
| P1.5/TA0.4        | 5 | P1.5 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA0.CCI4A          | 0                        | 1       |
|                   |   | TA0.4              | 1                        | 1       |
| P1.6/TA1CLK/CBOUT | 6 | P1.6 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA1CLK             | 0                        | 1       |
|                   |   | CBOUT comparator B | 1                        | 1       |
| P1.7/TA1.0        | 7 | P1.7 (I/O)         | I: 0; O: 1               | 0       |
|                   |   | TA1.CCI0A          | 0                        | 1       |
|                   |   | TA1.0              | 1                        | 1       |

## Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger





**Table 49. Port P2 (P2.0 to P2.7) Pin Functions**

| PIN NAME (P2.x)                  | x | FUNCTION                           | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |
|----------------------------------|---|------------------------------------|-----------------------------------------|---------|
|                                  |   |                                    | P2DIR.x                                 | P2SEL.x |
| P2.0/TA1.1 <sup>(2)</sup>        | 0 | P2.0 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA1.CCI1A                          | 0                                       | 1       |
|                                  |   | TA1.1                              | 1                                       | 1       |
| P2.1/TA1.2 <sup>(2)</sup>        | 1 | P2.1 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA1.CCI2A                          | 0                                       | 1       |
|                                  |   | TA1.2                              | 1                                       | 1       |
| P2.2/TA2CLK/SMCLK <sup>(2)</sup> | 2 | P2.2 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA2CLK                             | 0                                       | 1       |
|                                  |   | SMCLK                              | 1                                       | 1       |
| P2.3/TA2.0 <sup>(2)</sup>        | 3 | P2.3 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA2.CCI0A                          | 0                                       | 1       |
|                                  |   | TA2.0                              | 1                                       | 1       |
| P2.4/TA2.1 <sup>(2)</sup>        | 4 | P2.4 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA2.CCI1A                          | 0                                       | 1       |
|                                  |   | TA2.1                              | 1                                       | 1       |
| P2.5/TA2.2 <sup>(2)</sup>        | 5 | P2.5 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | TA2.CCI2A                          | 0                                       | 1       |
|                                  |   | TA2.2                              | 1                                       | 1       |
| P2.6/RTCCLK/DMAE0 <sup>(2)</sup> | 6 | P2.6 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | DMAE0                              | 0                                       | 1       |
|                                  |   | RTCCLK                             | 1                                       | 1       |
| P2.7/UCB0STE/UCA0CLK             | 7 | P2.7 (I/O)                         | I: 0; O: 1                              | 0       |
|                                  |   | UCB0STE/UCA0CLK <sup>(3) (4)</sup> | X                                       | 1       |

(1) X = Don't care

(2) Not available on RGZ package types.

(3) The pin direction is controlled by the USCI module.

(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

## Port P3, P3.0 to P3.4, Input/Output With Schmitt Trigger

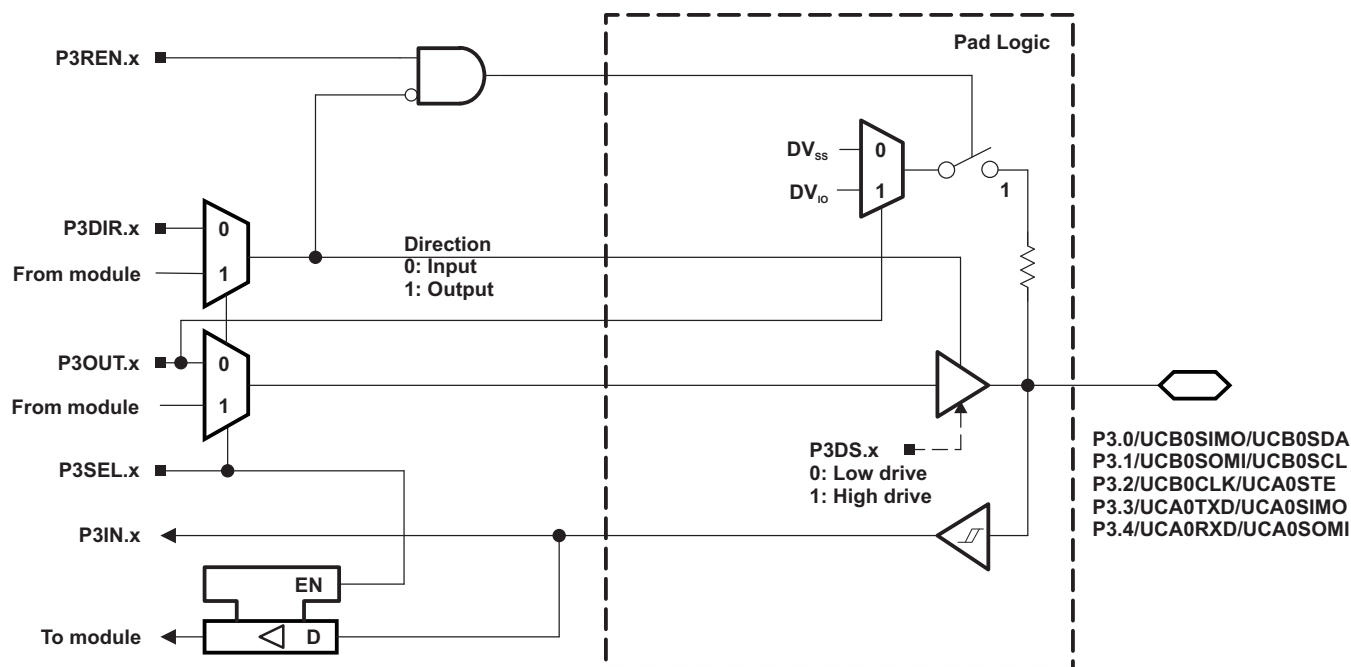


Table 50. Port P3 (P3.0 to P3.4) Pin Functions

| PIN NAME (P3.x)       | x | FUNCTION                            | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |
|-----------------------|---|-------------------------------------|-----------------------------------------|---------|
|                       |   |                                     | P3DIR.x                                 | P3SEL.x |
| P3.0/UCB0SIMO/UCB0SDA | 0 | P3.0 (I/O)                          | I: 0; O: 1                              | 0       |
|                       |   | UCB0SIMO/UCB0SDA <sup>(2) (3)</sup> | X                                       | 1       |
| P3.1/UCB0SOMI/UCB0SCL | 1 | P3.1 (I/O)                          | I: 0; O: 1                              | 0       |
|                       |   | UCB0SOMI/UCB0SCL <sup>(2) (3)</sup> | X                                       | 1       |
| P3.2/UCB0CLK/UCA0STE  | 2 | P3.2 (I/O)                          | I: 0; O: 1                              | 0       |
|                       |   | UCB0CLK/UCA0STE <sup>(2) (4)</sup>  | X                                       | 1       |
| P3.3/UCA0TXD/UCA0SIMO | 3 | P3.3 (I/O)                          | I: 0; O: 1                              | 0       |
|                       |   | UCA0TXD/UCA0SIMO <sup>(2)</sup>     | X                                       | 1       |
| P3.4/UCA0RXD/UCA0SOMI | 4 | P3.4 (I/O)                          | I: 0; O: 1                              | 0       |
|                       |   | UCA0RXD/UCA0SOMI <sup>(2)</sup>     | X                                       | 1       |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I2C functionality is selected, the output drives only the logical 0 to V<sub>SS</sub> level.

(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

## Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

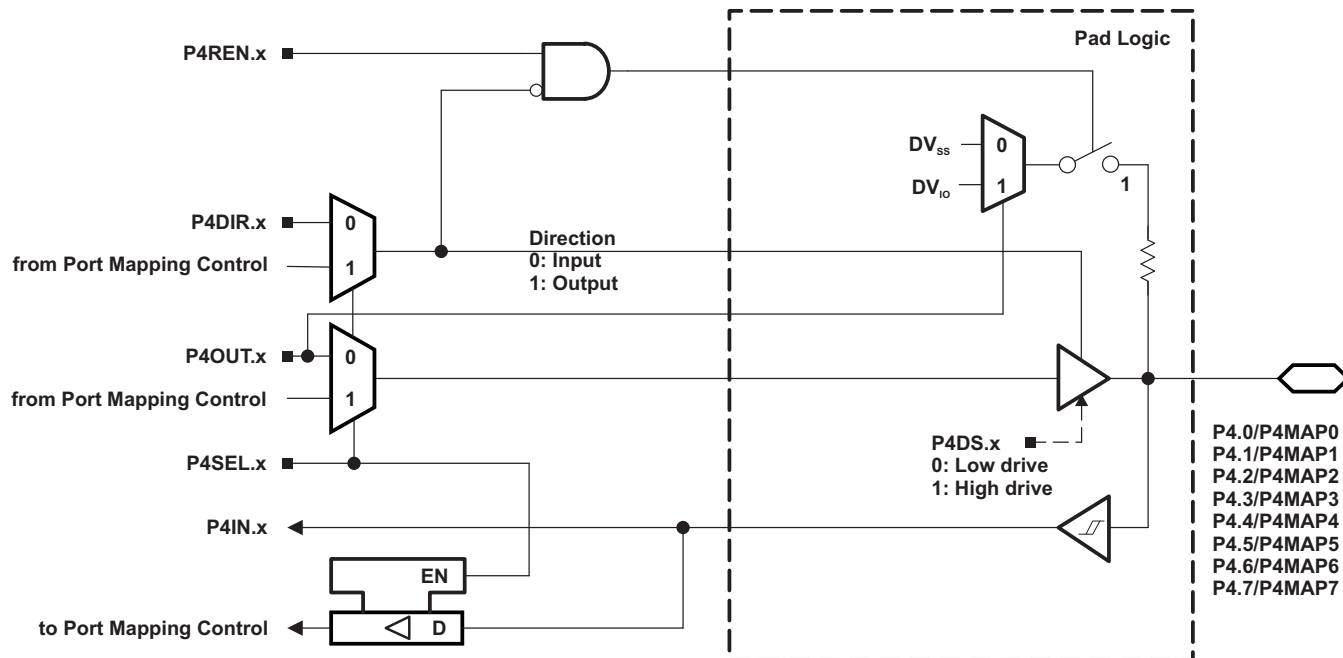


Table 51. Port P4 (P4.0 to P4.7) Pin Functions

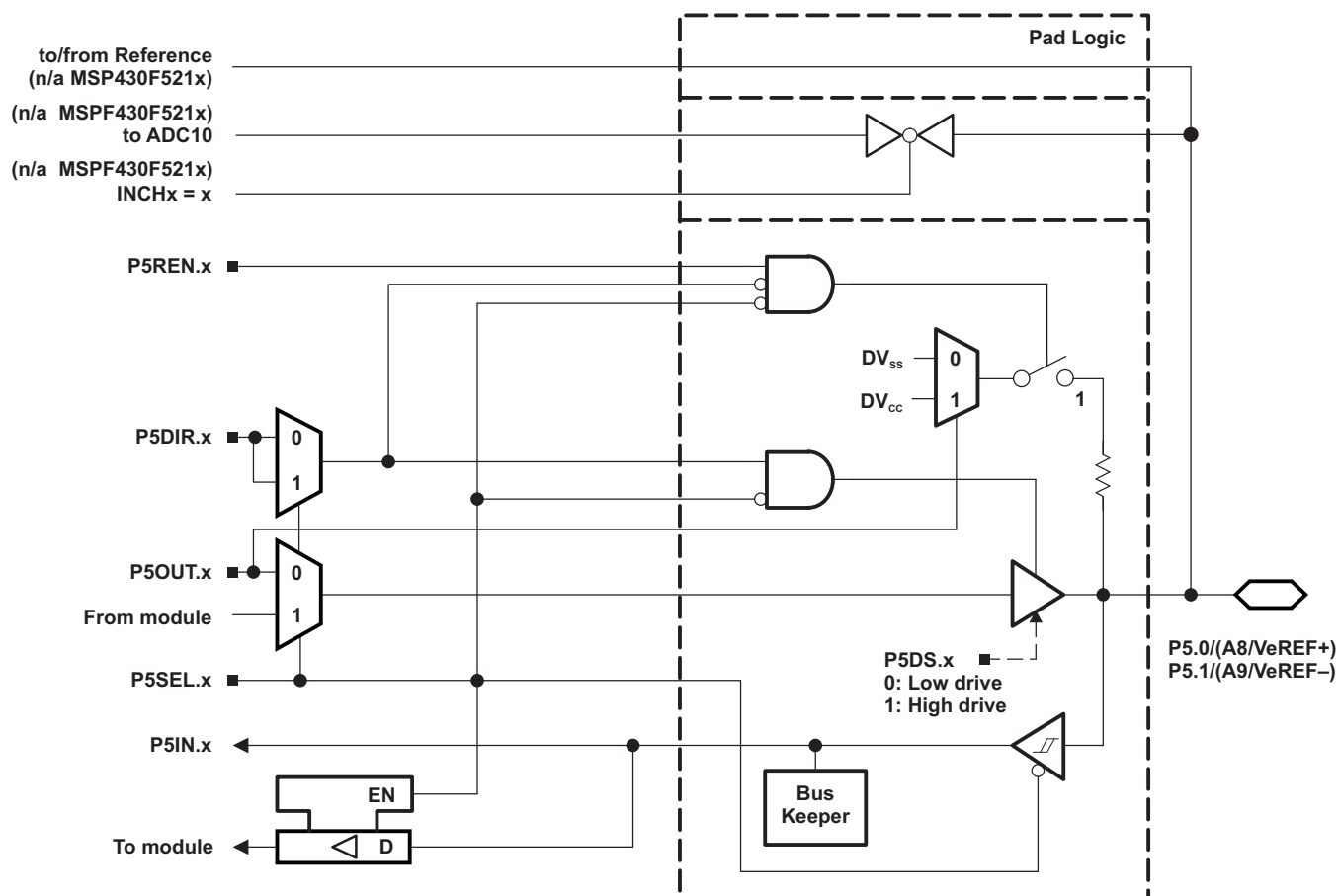
| PIN NAME (P4.x)            | x | FUNCTION                          | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |        |
|----------------------------|---|-----------------------------------|-----------------------------------------|---------|--------|
|                            |   |                                   | P4DIR.x <sup>(2)</sup>                  | P4SEL.x | P4MAPx |
| P4.0/P4MAP0                | 0 | P4.0 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.1/P4MAP1                | 1 | P4.1 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.2/P4MAP2                | 2 | P4.2 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.3/P4MAP3                | 3 | P4.3 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.4/P4MAP4                | 4 | P4.4 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.5/P4MAP5                | 5 | P4.5 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.6/P4MAP6                | 6 | P4.6 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |
| P4.7/P4MAP7 <sup>(3)</sup> | 7 | P4.7 (I/O)                        | I: 0; O: 1                              | 0       | X      |
|                            |   | Mapped secondary digital function | X                                       | 1       | ≤ 30   |

(1) X = Don't care

(2) The direction of some mapped secondary functions are controlled directly by the module. See Table 11 for specific direction control information of mapped secondary functions.

(3) Not available on RGZ package types.

## Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

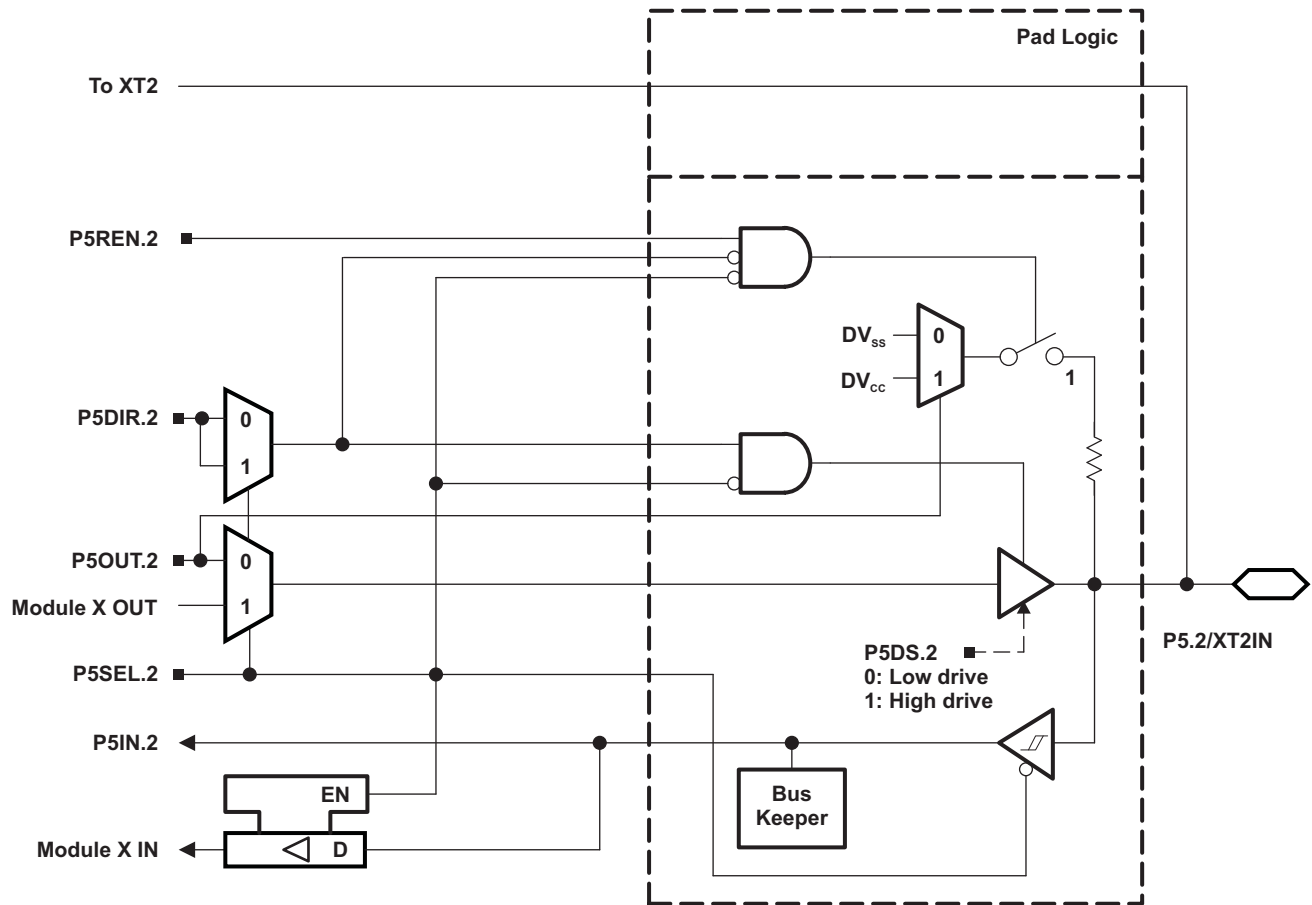


### Table 52. Port P5 (P5.0 and P5.1) Pin Functions

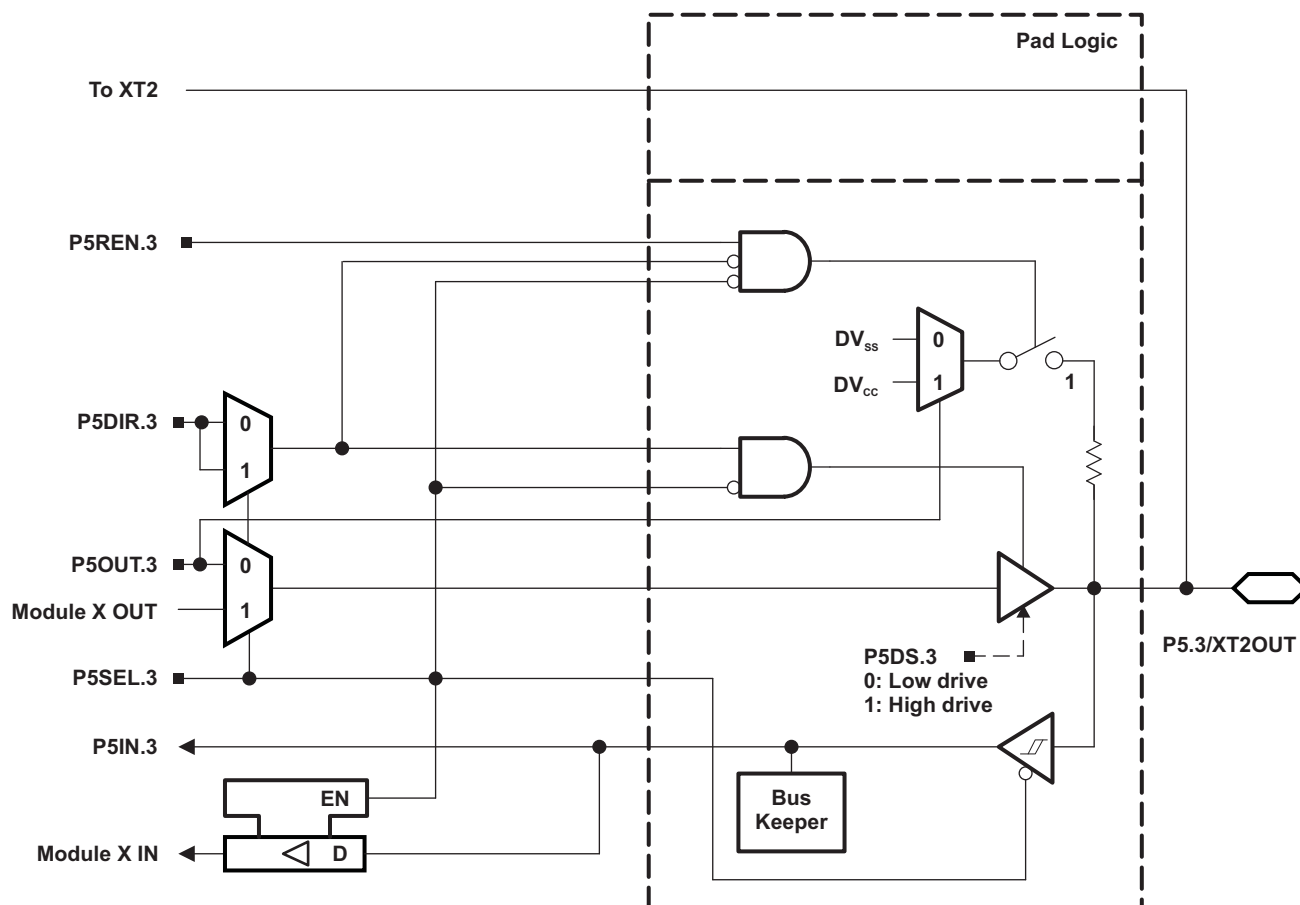
| PIN NAME (P5.x) | x | FUNCTION                  | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |                       |
|-----------------|---|---------------------------|-----------------------------------------|---------|-----------------------|
|                 |   |                           | P5DIR.x                                 | P5SEL.x | REFOUT <sup>(2)</sup> |
| P5.0/A8/VeREF+  | 0 | P5.0 (I/O) <sup>(3)</sup> | I: 0; O: 1                              | 0       | X                     |
|                 |   | A8/VeREF+ <sup>(4)</sup>  | X                                       | 1       | 0                     |
| P5.1/A9/VeREF−  | 1 | P5.1 (I/O) <sup>(3)</sup> | I: 0; O: 1                              | 0       | X                     |
|                 |   | A9/VeREF− <sup>(5)</sup>  | X                                       | 1       | 0                     |

- (1) X = Don't care
- (2) REFOUT resides in the REF module.
- (3) Default condition
- (4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10\_A. Channel A8, when selected with the INCHx bits, is connected to the VeREF+ pin.
- (5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10\_A. Channel A9, when selected with the INCHx bits, is connected to the VeREF- pin.

## Port P5, P5.2, Input/Output With Schmitt Trigger



## Port P5, P5.3, Input/Output With Schmitt Trigger



**Table 53. Port P5 (P5.2, P5.3) Pin Functions**

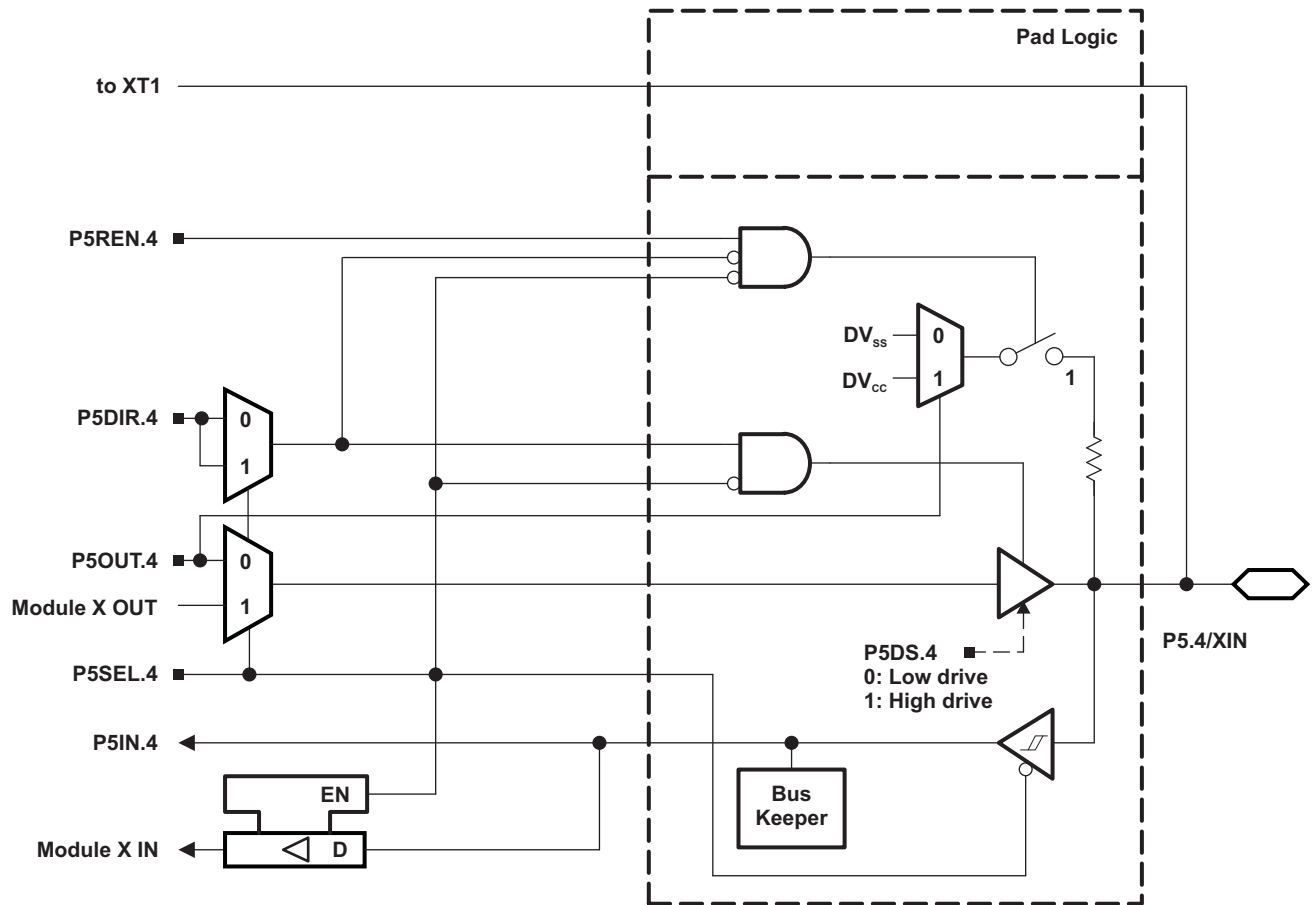
| PIN NAME (P5.x) | x | FUNCTION                           | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |         |           |
|-----------------|---|------------------------------------|-----------------------------------------|---------|---------|-----------|
|                 |   |                                    | P5DIR.x                                 | P5SEL.2 | P5SEL.3 | XT2BYPASS |
| P5.2/XT2IN      | 2 | P5.2 (I/O)                         | I: 0; O: 1                              | 0       | X       | X         |
|                 |   | XT2IN crystal mode <sup>(2)</sup>  | X                                       | 1       | X       | 0         |
|                 |   | XT2IN bypass mode <sup>(2)</sup>   | X                                       | 1       | X       | 1         |
| P5.3/XT2OUT     | 3 | P5.3 (I/O)                         | I: 0; O: 1                              | 0       | X       | X         |
|                 |   | XT2OUT crystal mode <sup>(3)</sup> | X                                       | 1       | X       | 0         |
|                 |   | P5.3 (I/O) <sup>(3)</sup>          | X                                       | 1       | X       | 1         |

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

## Port P5, P5.4 and P5.5 Input/Output With Schmitt Trigger



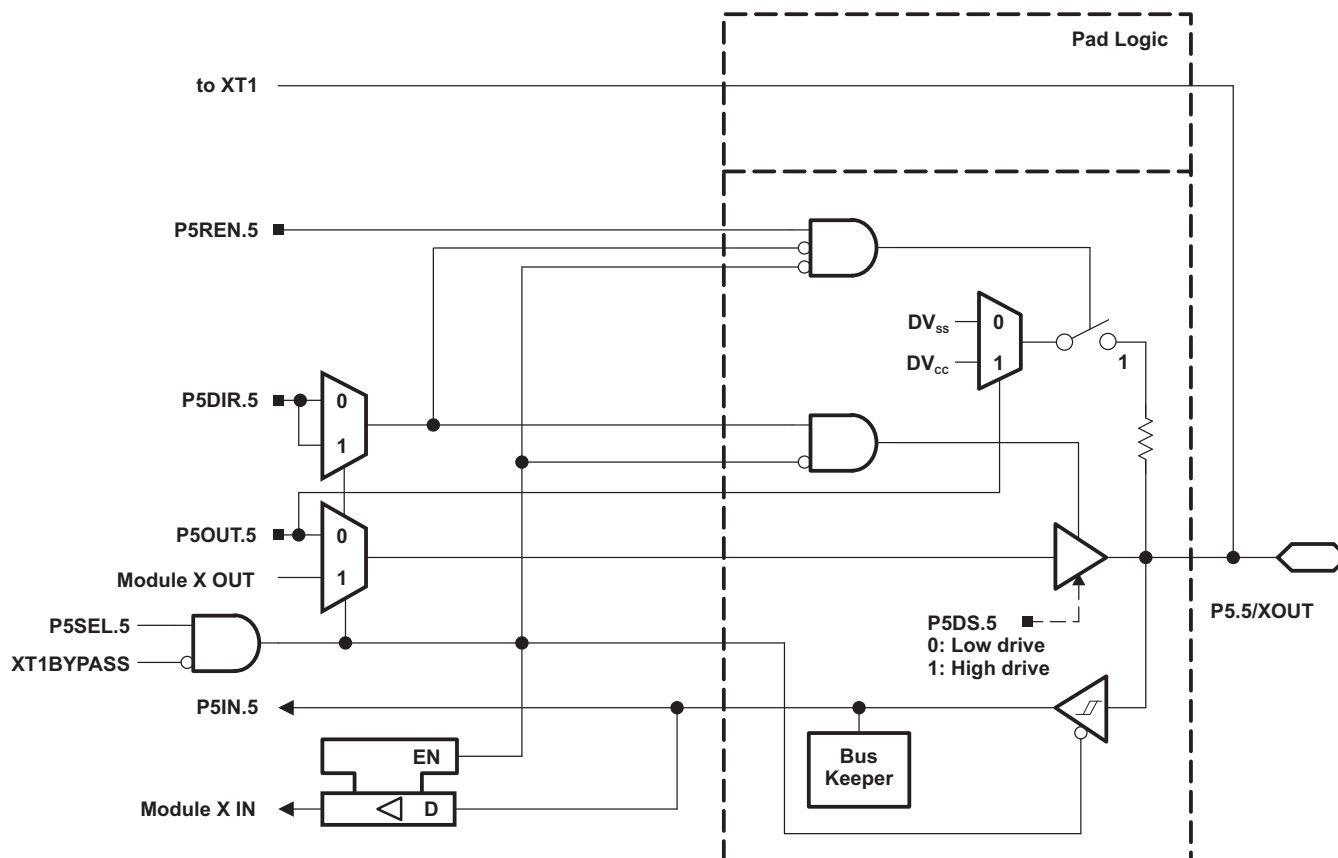


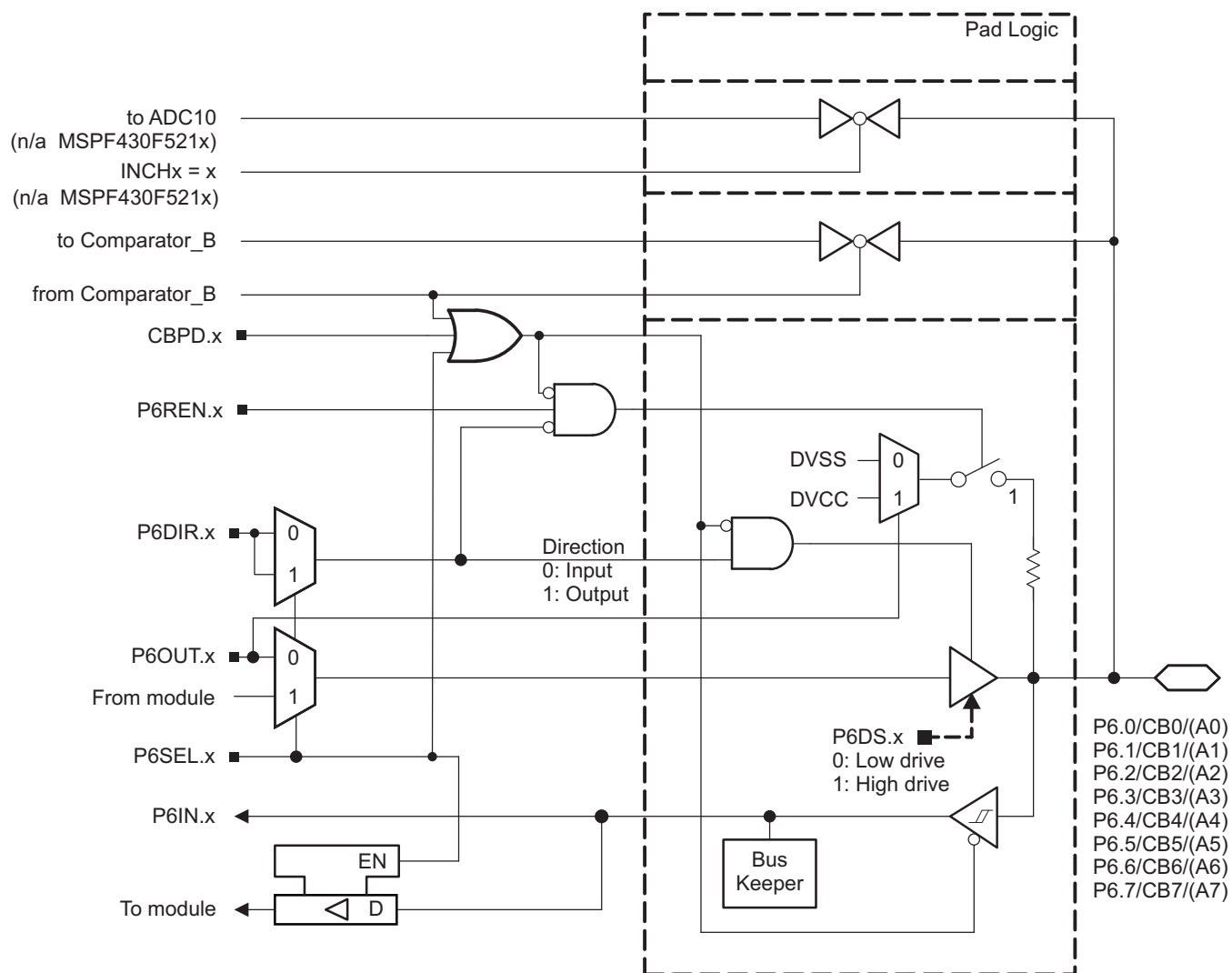
Table 54. Port P5 (P5.4 and P5.5) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION                         | CONTROL BITS AND SIGNALS <sup>(1)</sup> |         |         |           |
|-----------------|---|----------------------------------|-----------------------------------------|---------|---------|-----------|
|                 |   |                                  | P5DIR.x                                 | P5SEL.4 | P5SEL.5 | XT1BYPASS |
| P5.4/XIN        | 4 | P5.4 (I/O)                       | I: 0; O: 1                              | 0       | X       | X         |
|                 |   | XIN crystal mode <sup>(2)</sup>  | X                                       | 1       | X       | 0         |
|                 |   | XIN bypass mode <sup>(2)</sup>   | X                                       | 1       | X       | 1         |
| P5.5/XOUT       | 5 | P5.5 (I/O)                       | I: 0; O: 1                              | 0       | X       | X         |
|                 |   | XOUT crystal mode <sup>(3)</sup> | X                                       | 1       | X       | 0         |
|                 |   | P5.5 (I/O) <sup>(3)</sup>        | X                                       | 1       | X       | 1         |

- (1) X = Don't care  
 (2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.  
 (3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.



## Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger



**Table 55. Port P6 (P6.0 to P6.7) Pin Functions**

| PIN NAME (P6.x)              | x | FUNCTION           | CONTROL BITS AND SIGNALS |         |      |
|------------------------------|---|--------------------|--------------------------|---------|------|
|                              |   |                    | P6DIR.x                  | P6SEL.x | CBPD |
| P6.0/CB0/(A0)                | 0 | P6.0 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A0                 | X                        | 1       | X    |
|                              |   | CB0 <sup>(1)</sup> | X                        | X       | 1    |
| P6.1/CB1/(A1)                | 1 | P6.1 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A1                 | X                        | 1       | X    |
|                              |   | CB1 <sup>(1)</sup> | X                        | X       | 1    |
| P6.2/CB2/(A2)                | 2 | P6.2 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A2                 | X                        | 1       | X    |
|                              |   | CB2 <sup>(1)</sup> | X                        | X       | 1    |
| P6.3/CB3/(A3)                | 3 | P6.3 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A3                 | X                        | 1       | X    |
|                              |   | CB3 <sup>(1)</sup> | X                        | X       | 1    |
| P6.4/CB4/(A4)                | 4 | P6.4 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A4                 | X                        | 1       | X    |
|                              |   | CB4 <sup>(1)</sup> | X                        | X       | 1    |
| P6.5/CB5/(A5)                | 5 | P6.5 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A5                 | X                        | 1       | X    |
|                              |   | CB5 <sup>(1)</sup> | X                        | X       | 1    |
| P6.6/CB6/(A6) <sup>(2)</sup> | 6 | P6.6 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A6                 | X                        | 1       | X    |
|                              |   | CB6 <sup>(1)</sup> | X                        | X       | 1    |
| P6.7/CB7/(A7) <sup>(2)</sup> | 7 | P6.7 (I/O)         | I: 0; O: 1               | 0       | 0    |
|                              |   | A7                 | X                        | 1       | X    |
|                              |   | CB7 <sup>(1)</sup> | X                        | X       | 1    |

(1) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

(2) Not available on RGZ package types.

## Port P7, P7.0 to P7.5, Input/Output With Schmitt Trigger

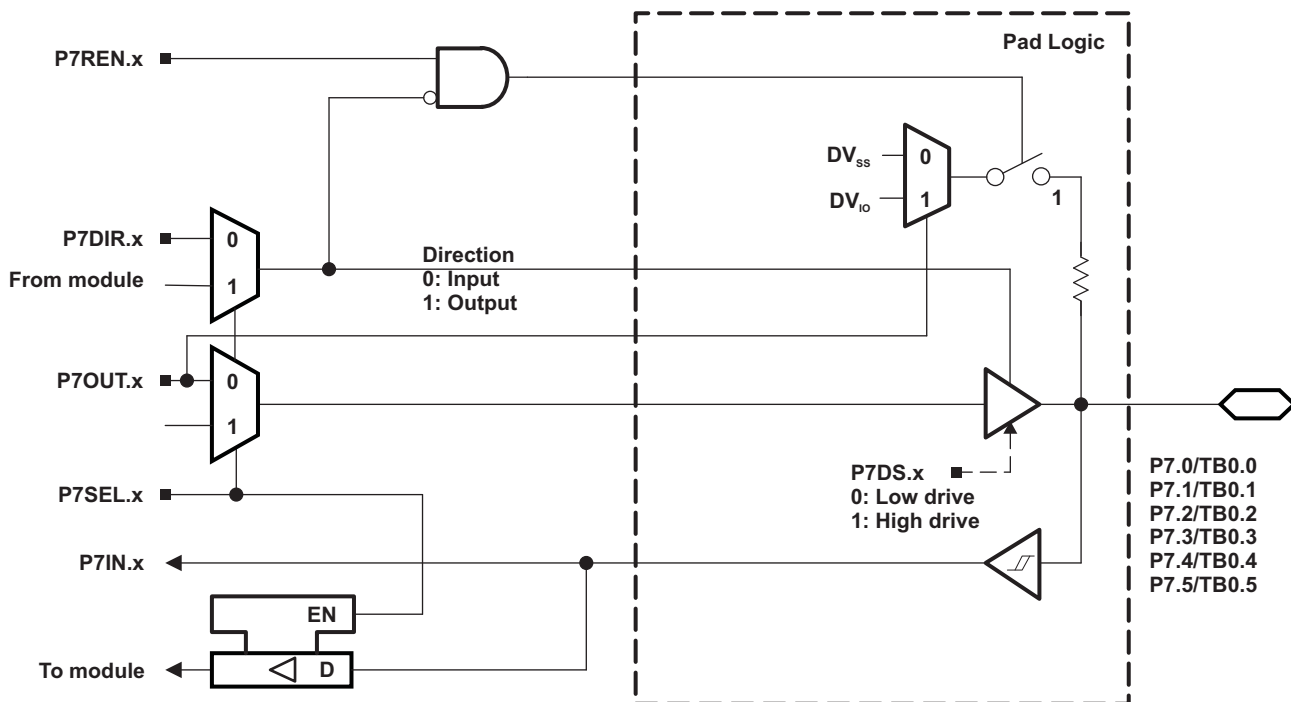


Table 56. Port P7 (P7.0 to P7.5) Pin Functions

| PIN NAME (P7.x)           | x | FUNCTION   | CONTROL BITS AND SIGNALS |         |
|---------------------------|---|------------|--------------------------|---------|
|                           |   |            | P7DIR.x                  | P7SEL.x |
| P7.0/TB0.0 <sup>(1)</sup> | 0 | P7.0 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI0A  | 0                        | 1       |
|                           |   | TB0.0      | 1                        | 1       |
| P7.1/TB0.1 <sup>(1)</sup> | 1 | P7.1 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI1A  | 0                        | 1       |
|                           |   | TB0.1      | 1                        | 1       |
| P7.2/TB0.2 <sup>(1)</sup> | 2 | P7.2 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI2A  | 0                        | 1       |
|                           |   | TB0.2      | 1                        | 1       |
| P7.3/TB0.3 <sup>(1)</sup> | 3 | P7.3 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI3A  | 0                        | 1       |
|                           |   | TB0.3      | 1                        | 1       |
| P7.4/TB0.4 <sup>(1)</sup> | 4 | P7.4 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI4A  | 0                        | 1       |
|                           |   | TB0.4      | 1                        | 1       |
| P7.5/TB0.5 <sup>(1)</sup> | 5 | P7.5 (I/O) | I: 0; O: 1               | 0       |
|                           |   | TB0.CCI5A  | 0                        | 1       |
|                           |   | TB0.5      | 1                        | 1       |

(1) Not available on RGZ package types.

The diagram illustrates the internal circuitry of the Pad Logic for the PJ.0/TDO pin. The circuit is enclosed in a dashed box labeled "Pad Logic".

- Inputs:**
  - PJREN.0:** A control signal that is ANDed with the output of the first multiplexer.
  - PJDIR.0:** A control signal that selects between DVCC and the output of the second multiplexer for the first multiplexer's input 1.
  - DVCC:** A power supply input that can be selected for the first multiplexer's input 1.
  - PJOUT.0:** A data input that is selected for the second multiplexer's input 0.
  - From JTAG:** A signal that is selected for the second multiplexer's input 1.
  - PJIN.0:** A data input that is selected for the output of the inverter.
- Internal Logic:**
  - An AND gate takes PJREN.0 and the output of the first multiplexer as inputs.
  - A 2-to-1 multiplexer has two inputs: DV<sub>SS</sub> (input 0) and DV<sub>CC</sub> (input 1). Its output is selected by PJDIR.0.
  - A buffer takes the output of the AND gate and the output of the 2-to-1 multiplexer as inputs.
  - An inverter takes PJIN.0 as input.
- Output:** The output of the buffer is connected to the PJ.0/TDO pin. A pull-up resistor is connected to DV<sub>CC</sub> and a pull-down resistor is connected to DV<sub>SS</sub>.
- Legend:**
  - PJDS.0:** 0: Low drive, 1: High drive.

**Table 57. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION                    | CONTROL BITS<br>AND SIGNALS <sup>(1)</sup> |
|-----------------|---|-----------------------------|--------------------------------------------|
|                 |   |                             | PJDIR.x                                    |
| PJ.0/TDO        | 0 | PJ.0 (I/O) <sup>(2)</sup>   | I: 0; O: 1                                 |
|                 |   | TDO <sup>(3)</sup>          | X                                          |
| PJ.1/TDI/TCLK   | 1 | PJ.1 (I/O) <sup>(2)</sup>   | I: 0; O: 1                                 |
|                 |   | TDI/TCLK <sup>(3) (4)</sup> | X                                          |
| PJ.2/TMS        | 2 | PJ.2 (I/O) <sup>(2)</sup>   | I: 0; O: 1                                 |
|                 |   | TMS <sup>(3) (4)</sup>      | X                                          |
| PJ.3/TCK        | 3 | PJ.3 (I/O) <sup>(2)</sup>   | I: 0; O: 1                                 |
|                 |   | TCK <sup>(3) (4)</sup>      | X                                          |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

## DEVICE DESCRIPTORS

Table 58 and Table 59 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 58. MSP430F522x Device Descriptor Table<sup>(1)</sup>**

|                              | Description                           | Address | Size<br>(bytes) | F5229      | F5227      | F5224      | F5222      |
|------------------------------|---------------------------------------|---------|-----------------|------------|------------|------------|------------|
|                              |                                       |         |                 | Value      | Value      | Value      | Value      |
| <b>Info Block</b>            | Info length                           | 01A00h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | CRC length                            | 01A01h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | CRC value                             | 01A02h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Device ID                             | 01A04h  | 1               | 51h        | 4Fh        | 4Ch        | 4Ah        |
|                              | Device ID                             | 01A05h  | 1               | 81h        | 81h        | 81h        | 81h        |
|                              | Hardware revision                     | 01A06h  | 1               | per unit   | per unit   | per unit   | per unit   |
| <b>Die Record</b>            | Firmware revision                     | 01A07h  | 1               | per unit   | per unit   | per unit   | per unit   |
|                              | Die Record Tag                        | 01A08h  | 1               | 08h        | 08h        | 08h        | 08h        |
|                              | Die Record length                     | 01A09h  | 1               | 0Ah        | 0Ah        | 0Ah        | 0Ah        |
|                              | Lot/Wafer ID                          | 01A0Ah  | 4               | per unit   | per unit   | per unit   | per unit   |
|                              | Die X position                        | 01A0Eh  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Die Y position                        | 01A10h  | 2               | per unit   | per unit   | per unit   | per unit   |
| <b>ADC10 Calibration</b>     | Test results                          | 01A12h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC10 Calibration Tag                 | 01A14h  | 1               | 13h        | 13h        | 13h        | 13h        |
|                              | ADC10 Calibration length              | 01A15h  | 1               | 10h        | 10h        | 10h        | 10h        |
|                              | ADC Gain Factor                       | 01A16h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC Offset                            | 01A18h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | REF Calibration Tag                   | 01A26h  | 1               | 12h        | 12h        | 12h        | 12h        |
| <b>REF Calibration</b>       | REF Calibration length                | 01A27h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | REF 1.5-V Reference Factor            | 01A28h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | REF 2.0-V Reference Factor            | 01A2Ah  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | REF 2.5-V Reference Factor            | 01A2Ch  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Peripheral Descriptor Tag             | 01A2Eh  | 1               | 02h        | 02h        | 02h        | 02h        |
| <b>Peripheral Descriptor</b> | Peripheral Descriptor Length          | 01A2Fh  | 1               | 5Fh        | 5Fh        | 5Dh        | 5Dh        |
|                              | Memory 1                              |         | 2               | 08h<br>8Ah | 08h<br>8Ah | 08h<br>8Ah | 08h<br>8Ah |
|                              | Memory 2                              |         | 2               | 0Ch<br>86h | 0Ch<br>86h | 0Ch<br>86h | 0Ch<br>86h |
|                              | Memory 3                              |         | 2               | 12h<br>2Eh | 12h<br>2Eh | 12h<br>2Eh | 12h<br>2Eh |

(1) NA = Not applicable, blank = unused and reads FFh.

**Table 58. MSP430F522x Device Descriptor Table<sup>(1)</sup> (continued)**

|  | Description      | Address | Size<br>(bytes) | F5229      | F5227      | F5224      | F5222      |
|--|------------------|---------|-----------------|------------|------------|------------|------------|
|  |                  |         |                 | Value      | Value      | Value      | Value      |
|  | Memory 4         |         | 2               | 22h<br>96h | 22h<br>94h | 22h<br>96h | 22h<br>94h |
|  | Memory 5         |         | 2               | N/A        | N/A        | N/A        | N/A        |
|  | Memory 6         |         | 1/2             | N/A        | N/A        | N/A        | N/A        |
|  | delimiter        |         | 1               | 00h        | 00h        | 00h        | 00h        |
|  | Peripheral count |         | 1               | 20h        | 20h        | 1Fh        | 1Fh        |
|  | MSP430CPUXV2     |         | 2               | 00h<br>23h | 00h<br>23h | 00h<br>23h | 00h<br>23h |
|  | JTAG             |         | 2               | 00h<br>09h | 00h<br>09h | 00h<br>09h | 00h<br>09h |
|  | SBW              |         | 2               | 00h<br>0Fh | 00h<br>0Fh | 00h<br>0Fh | 00h<br>0Fh |
|  | EEM-S            |         | 2               | 00h<br>03h | 00h<br>03h | 00h<br>03h | 00h<br>05h |
|  | TI BSL           |         | 2               | 00h<br>FCh | 00h<br>FCh | 00h<br>FCh | 00h<br>FCh |
|  | SFR              |         | 2               | 10h<br>41h | 10h<br>41h | 10h<br>41h | 10h<br>41h |
|  | PMM              |         | 2               | 02h<br>30h | 02h<br>30h | 02h<br>30h | 02h<br>30h |
|  | FCTL             |         | 2               | 02h<br>38h | 02h<br>38h | 02h<br>38h | 02h<br>38h |
|  | CRC16            |         | 2               | 01h<br>3Ch | 01h<br>3Ch | 01h<br>3Ch | 01h<br>3Ch |
|  | CRC16_RB         |         | 2               | 00h<br>3Dh | 00h<br>3Dh | 00h<br>3Dh | 00h<br>3Dh |
|  | RAMCTL           |         | 2               | 00h<br>44h | 00h<br>44h | 00h<br>44h | 00h<br>44h |
|  | WDT_A            |         | 2               | 00h<br>40h | 00h<br>40h | 00h<br>40h | 00h<br>40h |
|  | UCS              |         | 2               | 01h<br>48h | 01h<br>48h | 01h<br>48h | 01h<br>48h |
|  | SYS              |         | 2               | 02h<br>42h | 02h<br>42h | 02h<br>42h | 02h<br>42h |
|  | REF              |         | 2               | 03h<br>A0h | 03h<br>A0h | 03h<br>A0h | 03h<br>A0h |
|  | Port Mapping     |         | 2               | 01h<br>10h | 01h<br>10h | 01h<br>10h | 01h<br>10h |
|  | Port 1/2         |         | 2               | 04h<br>51h | 04h<br>51h | 04h<br>51h | 04h<br>51h |
|  | Port 3/4         |         | 2               | 02h<br>52h | 02h<br>52h | 02h<br>52h | 02h<br>52h |
|  | Port 5/6         |         | 2               | 02h<br>53h | 02h<br>53h | 02h<br>53h | 02h<br>53h |
|  | Port 7/8         |         | 2               | 02h<br>54h | 02h<br>54h | N/A        | N/A        |
|  | JTAG             |         | 2               | 0Ch<br>5Fh | 0Ch<br>5Fh | 0Eh<br>5Fh | 0Eh<br>5Fh |
|  | TA0              |         | 2               | 02h<br>62h | 02h<br>62h | 02h<br>62h | 02h<br>62h |
|  | TA1              |         | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|  | TB0              |         | 2               | 04h<br>67h | 04h<br>67h | 04h<br>67h | 04h<br>67h |

**Table 58. MSP430F522x Device Descriptor Table<sup>(1)</sup> (continued)**

|                   | Description   | Address | Size<br>(bytes) | F5229      | F5227      | F5224      | F5222      |
|-------------------|---------------|---------|-----------------|------------|------------|------------|------------|
|                   |               |         |                 | Value      | Value      | Value      | Value      |
|                   | TA2           |         | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|                   | RTC           |         | 2               | 0Ah<br>68h | 0Ah<br>68h | 0Ah<br>68h | 0Ah<br>68h |
|                   | MPY32         |         | 2               | 02h<br>85h | 02h<br>85h | 02h<br>85h | 02h<br>85h |
|                   | DMA-3         |         | 2               | 04h<br>47h | 04h<br>47h | 04h<br>47h | 04h<br>47h |
|                   | USCI_A/B      |         | 2               | 0Ch<br>90h | 0Ch<br>90h | 0Ch<br>90h | 0Ch<br>90h |
|                   | USCI_A/B      |         | 2               | 04h<br>90h | 04h<br>90h | 04h<br>90h | 04h<br>90h |
|                   | ADC10_A       |         | 2               | 14h<br>D3h | 14h<br>D3h | 14h<br>D3h | 14h<br>D3h |
|                   | COMP_B        |         | 2               | 18h<br>A8h | 18h<br>A8h | 18h<br>A8h | 18h<br>A8h |
| <b>Interrupts</b> | COMP_B        |         | 1               | A8h        | A8h        | A8h        | A8h        |
|                   | TB0.CCIFG0    |         | 1               | 64h        | 64h        | 64h        | 64h        |
|                   | TB0.CCIFG1..6 |         | 1               | 65h        | 65h        | 65h        | 65h        |
|                   | WDTIFG        |         | 1               | 40h        | 40h        | 40h        | 40h        |
|                   | USCI_A0       |         | 1               | 90h        | 90h        | 90h        | 90h        |
|                   | USCI_B0       |         | 1               | 91h        | 91h        | 91h        | 91h        |
|                   | ADC10_A       |         | 1               | D0h        | D0h        | D0h        | D0h        |
|                   | TA0.CCIFG0    |         | 1               | 60h        | 60h        | 60h        | 60h        |
|                   | TA0.CCIFG1..4 |         | 1               | 61h        | 61h        | 61h        | 61h        |
|                   | Reserved      |         | 1               | 01h        | 01h        | 01h        | 01h        |
|                   | DMA           |         | 1               | 46h        | 46h        | 46h        | 46h        |
|                   | TA1.CCIFG0    |         | 1               | 62h        | 62h        | 62h        | 62h        |
|                   | TA1.CCIFG1..2 |         | 1               | 63h        | 63h        | 63h        | 63h        |
|                   | P1            |         | 1               | 50h        | 50h        | 50h        | 50h        |
|                   | USCI_A1       |         | 1               | 92h        | 92h        | 92h        | 92h        |
|                   | USCI_B1       |         | 1               | 93h        | 93h        | 93h        | 93h        |
|                   | TA1.CCIFG0    |         | 1               | 66h        | 66h        | 66h        | 66h        |
|                   | TA1.CCIFG1..2 |         | 1               | 67h        | 67h        | 67h        | 67h        |
|                   | P2            |         | 1               | 51h        | 51h        | 51h        | 51h        |
|                   | RTC_A         |         | 1               | 68h        | 68h        | 68h        | 68h        |
|                   | delimiter     |         | 1               | 00h        | 00h        | 00h        | 00h        |



**Table 59. MSP430F521x Device Descriptor Table<sup>(1)</sup>**

|                              | Description                           | Address | Size<br>(bytes) | F5219      | F5217      | F5214      | F5212      |
|------------------------------|---------------------------------------|---------|-----------------|------------|------------|------------|------------|
|                              |                                       |         |                 | Value      | Value      | Value      | Value      |
| <b>Info Block</b>            | Info length                           | 01A00h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | CRC length                            | 01A01h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | CRC value                             | 01A02h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Device ID                             | 01A04h  | 1               | 47h        | 45h        | 42h        | 40h        |
|                              | Device ID                             | 01A05h  | 1               | 81h        | 81h        | 81h        | 81h        |
|                              | Hardware revision                     | 01A06h  | 1               | per unit   | per unit   | per unit   | per unit   |
|                              | Firmware revision                     | 01A07h  | 1               | per unit   | per unit   | per unit   | per unit   |
| <b>Die Record</b>            | Die Record Tag                        | 01A08h  | 1               | 08h        | 08h        | 08h        | 08h        |
|                              | Die Record length                     | 01A09h  | 1               | 0Ah        | 0Ah        | 0Ah        | 0Ah        |
|                              | Lot/Wafer ID                          | 01A0Ah  | 4               | per unit   | per unit   | per unit   | per unit   |
|                              | Die X position                        | 01A0Eh  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Die Y position                        | 01A10h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | Test results                          | 01A12h  | 2               | per unit   | per unit   | per unit   | per unit   |
| <b>ADC10 Calibration</b>     | ADC10 Calibration Tag                 | 01A14h  | 1               | 13h        | 13h        | 13h        | 13h        |
|                              | ADC10 Calibration length              | 01A15h  | 1               | 10h        | 10h        | 10h        | 10h        |
|                              | ADC Gain Factor                       | 01A16h  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC Offset                            | 01A18h  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h  | 2               | blank      | blank      | blank      | blank      |
|                              | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h  | 2               | blank      | blank      | blank      | blank      |
| <b>REF Calibration</b>       | REF Calibration Tag                   | 01A26h  | 1               | 12h        | 12h        | 12h        | 12h        |
|                              | REF Calibration length                | 01A27h  | 1               | 06h        | 06h        | 06h        | 06h        |
|                              | REF 1.5-V Reference Factor            | 01A28h  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | REF 2.0-V Reference Factor            | 01A2Ah  | 2               | per unit   | per unit   | per unit   | per unit   |
|                              | REF 2.5-V Reference Factor            | 01A2Ch  | 2               | per unit   | per unit   | per unit   | per unit   |
| <b>Peripheral Descriptor</b> | Peripheral Descriptor Tag             | 01A2Eh  | 1               | 02h        | 02h        | 02h        | 02h        |
|                              | Peripheral Descriptor Length          | 01A2Fh  | 1               | 5Dh        | 5Dh        | 5Bh        | 5Bh        |
|                              | Memory 1                              |         | 2               | 08h<br>8Ah | 08h<br>8Ah | 08h<br>8Ah | 08h<br>8Ah |
|                              | Memory 2                              |         | 2               | 0Ch<br>86h | 0Ch<br>86h | 0Ch<br>86h | 0Ch<br>86h |
|                              | Memory 3                              |         | 2               | 12h<br>2Eh | 12h<br>2Eh | 12h<br>2Eh | 12h<br>2Eh |
|                              | Memory 4                              |         | 2               | 22h<br>96h | 22h<br>94h | 22h<br>96h | 22h<br>94h |
|                              | Memory 5                              |         | 2               | N/A        | N/A        | N/A        | N/A        |
|                              | Memory 6                              |         | 1/2             | N/A        | N/A        | N/A        | N/A        |
|                              | delimiter                             |         | 1               | 00h        | 00h        | 00h        | 00h        |

(1) NA = Not applicable, blank = unused and reads FFh.

**Table 59. MSP430F521x Device Descriptor Table<sup>(1)</sup> (continued)**

|  | Description      | Address | Size<br>(bytes) | F5219      | F5217      | F5214      | F5212      |
|--|------------------|---------|-----------------|------------|------------|------------|------------|
|  |                  |         |                 | Value      | Value      | Value      | Value      |
|  | Peripheral count |         | 1               | 1Fh        | 1Fh        | 1Eh        | 1Eh        |
|  | MSP430CPUXV2     |         | 2               | 00h<br>23h | 00h<br>23h | 00h<br>23h | 00h<br>23h |
|  | JTAG             |         | 2               | 00h<br>09h | 00h<br>09h | 00h<br>09h | 00h<br>09h |
|  | SBW              |         | 2               | 00h<br>0Fh | 00h<br>0Fh | 00h<br>0Fh | 00h<br>0Fh |
|  | EEM-S            |         | 2               | 00h<br>03h | 00h<br>03h | 00h<br>03h | 00h<br>05h |
|  | TI BSL           |         | 2               | 00h<br>FCh | 00h<br>FCh | 00h<br>FCh | 00h<br>FCh |
|  | SFR              |         | 2               | 10h<br>41h | 10h<br>41h | 10h<br>41h | 10h<br>41h |
|  | PMM              |         | 2               | 02h<br>30h | 02h<br>30h | 02h<br>30h | 02h<br>30h |
|  | FCTL             |         | 2               | 02h<br>38h | 02h<br>38h | 02h<br>38h | 02h<br>38h |
|  | CRC16            |         | 2               | 01h<br>3Ch | 01h<br>3Ch | 01h<br>3Ch | 01h<br>3Ch |
|  | CRC16_RB         |         | 2               | 00h<br>3Dh | 00h<br>3Dh | 00h<br>3Dh | 00h<br>3Dh |
|  | RAMCTL           |         | 2               | 00h<br>44h | 00h<br>44h | 00h<br>44h | 00h<br>44h |
|  | WDT_A            |         | 2               | 00h<br>40h | 00h<br>40h | 00h<br>40h | 00h<br>40h |
|  | UCS              |         | 2               | 01h<br>48h | 01h<br>48h | 01h<br>48h | 01h<br>48h |
|  | SYS              |         | 2               | 02h<br>42h | 02h<br>42h | 02h<br>42h | 02h<br>42h |
|  | REF              |         | 2               | 03h<br>A0h | 03h<br>A0h | 03h<br>A0h | 03h<br>A0h |
|  | Port Mapping     |         | 2               | 01h<br>10h | 01h<br>10h | 01h<br>10h | 01h<br>10h |
|  | Port 1/2         |         | 2               | 04h<br>51h | 04h<br>51h | 04h<br>51h | 04h<br>51h |
|  | Port 3/4         |         | 2               | 02h<br>52h | 02h<br>52h | 02h<br>52h | 02h<br>52h |
|  | Port 5/6         |         | 2               | 02h<br>53h | 02h<br>53h | 02h<br>53h | 02h<br>53h |
|  | Port 7/8         |         | 2               | 02h<br>54h | 02h<br>54h | N/A        | N/A        |
|  | JTAG             |         | 2               | 0Ch<br>5Fh | 0Ch<br>5Fh | 0Eh<br>5Fh | 0Eh<br>5Fh |
|  | TA0              |         | 2               | 02h<br>62h | 02h<br>62h | 02h<br>62h | 02h<br>62h |
|  | TA1              |         | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|  | TB0              |         | 2               | 04h<br>67h | 04h<br>67h | 04h<br>67h | 04h<br>67h |
|  | TA2              |         | 2               | 04h<br>61h | 04h<br>61h | 04h<br>61h | 04h<br>61h |
|  | RTC              |         | 2               | 0Ah<br>68h | 0Ah<br>68h | 0Ah<br>68h | 0Ah<br>68h |
|  | MPY32            |         | 2               | 02h<br>85h | 02h<br>85h | 02h<br>85h | 02h<br>85h |

**Table 59. MSP430F521x Device Descriptor Table<sup>(1)</sup> (continued)**

|                   | Description   | Address | Size<br>(bytes) | F5219      | F5217      | F5214      | F5212      |
|-------------------|---------------|---------|-----------------|------------|------------|------------|------------|
|                   |               |         |                 | Value      | Value      | Value      | Value      |
|                   | DMA-3         |         | 2               | 04h<br>47h | 04h<br>47h | 04h<br>47h | 04h<br>47h |
|                   | USCI_A/B      |         | 2               | 0Ch<br>90h | 0Ch<br>90h | 0Ch<br>90h | 0Ch<br>90h |
|                   | USCI_A/B      |         | 2               | 04h<br>90h | 04h<br>90h | 04h<br>90h | 04h<br>90h |
|                   | ADC10_A       |         | 2               | N/A        | N/A        | N/A        | N/A        |
|                   | COMP_B        |         | 2               | 2Ch<br>A8h | 2Ch<br>A8h | 2Ch<br>A8h | 2Ch<br>A8h |
| <b>Interrupts</b> | COMP_B        |         | 1               | A8h        | A8h        | A8h        | A8h        |
|                   | TB0.CCIFG0    |         | 1               | 64h        | 64h        | 64h        | 64h        |
|                   | TB0.CCIFG1..6 |         | 1               | 65h        | 65h        | 65h        | 65h        |
|                   | WDTIFG        |         | 1               | 40h        | 40h        | 40h        | 40h        |
|                   | USCI_A0       |         | 1               | 90h        | 90h        | 90h        | 90h        |
|                   | USCI_B0       |         | 1               | 91h        | 91h        | 91h        | 91h        |
|                   | Reserved      |         | 1               | 01h        | 01h        | 01h        | 01h        |
|                   | TA0.CCIFG0    |         | 1               | 60h        | 60h        | 60h        | 60h        |
|                   | TA0.CCIFG1..4 |         | 1               | 61h        | 61h        | 61h        | 61h        |
|                   | Reserved      |         | 1               | 01h        | 01h        | 01h        | 01h        |
|                   | DMA           |         | 1               | 46h        | 46h        | 46h        | 46h        |
|                   | TA1.CCIFG0    |         | 1               | 62h        | 62h        | 62h        | 62h        |
|                   | TA1.CCIFG1..2 |         | 1               | 63h        | 63h        | 63h        | 63h        |
|                   | P1            |         | 1               | 50h        | 50h        | 50h        | 50h        |
|                   | USCI_A1       |         | 1               | 92h        | 92h        | 92h        | 92h        |
|                   | USCI_B1       |         | 1               | 93h        | 93h        | 93h        | 93h        |
|                   | TA2.CCIFG0    |         | 1               | 66h        | 66h        | 66h        | 66h        |
|                   | TA2.CCIFG1..2 |         | 1               | 67h        | 67h        | 67h        | 67h        |
|                   | P2            |         | 1               | 51h        | 51h        | 51h        | 51h        |
|                   | RTC_A         |         | 1               | 68h        | 68h        | 68h        | 68h        |
|                   | delimiter     |         | 1               | 00h        | 00h        | 00h        | 00h        |

## REVISION HISTORY

| REVISION | DESCRIPTION                                     |
|----------|-------------------------------------------------|
| SLAS718  | Initial release                                 |
| SLAS718A | <a href="#">DCO Frequency</a> , Added note (1). |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type               | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|----------------------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F5212IRGZR | ACTIVE        | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5212                    | <a href="#">Samples</a> |
| MSP430F5212IRGZT | ACTIVE        | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5212                    | <a href="#">Samples</a> |
| MSP430F5213IRGZR | PREVIEW       | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5213                    |                         |
| MSP430F5213IRGZT | PREVIEW       | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5213                    |                         |
| MSP430F5214IRGZR | ACTIVE        | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5214                    | <a href="#">Samples</a> |
| MSP430F5214IRGZT | ACTIVE        | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5214                    | <a href="#">Samples</a> |
| MSP430F5217IRGCR | ACTIVE        | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5217                    | <a href="#">Samples</a> |
| MSP430F5217IRGCT | ACTIVE        | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5217                    | <a href="#">Samples</a> |
| MSP430F5217IYFFR | PREVIEW       | DSBGA                      | YFF                | 64   | 2500        | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5217IYFFT | PREVIEW       | DSBGA                      | YFF                | 64   | 250         | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5217IZQE  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 250         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5217                    | <a href="#">Samples</a> |
| MSP430F5217IZQER | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 2000        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5217                    | <a href="#">Samples</a> |
| MSP430F5218IRGCR | PREVIEW       | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5218                    |                         |
| MSP430F5218IRGCT | PREVIEW       | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5218                    |                         |
| MSP430F5218IYFFR | PREVIEW       | DSBGA                      | YFF                | 64   | 2500        | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5218IZQE  | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 360         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5218                    |                         |
| MSP430F5219IRGCR | ACTIVE        | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5219                    | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type               | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|----------------------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F5219IRGCT | ACTIVE        | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5219                    | <a href="#">Samples</a> |
| MSP430F5219IYFFR | PREVIEW       | DSBGA                      | YFF                | 64   | 2500        | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5219IYFFT | PREVIEW       | DSBGA                      | YFF                | 64   | 250         | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5219IZQE  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 360         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5219                    | <a href="#">Samples</a> |
| MSP430F5219IZQER | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 2500        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5219                    | <a href="#">Samples</a> |
| MSP430F5222IRGZR | ACTIVE        | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5222                    | <a href="#">Samples</a> |
| MSP430F5222IRGZT | ACTIVE        | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5222                    | <a href="#">Samples</a> |
| MSP430F5223IRGZR | PREVIEW       | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5223                    |                         |
| MSP430F5223IRGZT | PREVIEW       | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5223                    |                         |
| MSP430F5224IRGZR | ACTIVE        | VQFN                       | RGZ                | 48   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5224                    | <a href="#">Samples</a> |
| MSP430F5224IRGZT | ACTIVE        | VQFN                       | RGZ                | 48   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5224                    | <a href="#">Samples</a> |
| MSP430F5227IRGCR | ACTIVE        | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5227                    | <a href="#">Samples</a> |
| MSP430F5227IRGCT | ACTIVE        | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5227                    | <a href="#">Samples</a> |
| MSP430F5227IYFFR | PREVIEW       | DSBGA                      | YFF                | 64   | 2500        | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5227IYFFT | PREVIEW       | DSBGA                      | YFF                | 64   | 250         | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5227IZQE  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 360         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5227                    | <a href="#">Samples</a> |
| MSP430F5227IZQER | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 2500        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5227                    | <a href="#">Samples</a> |
| MSP430F5228IRGCR | PREVIEW       | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5228                    |                         |

| Orderable Device | Status<br>(1) | Package Type               | Package<br>Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|----------------------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| MSP430F5228IRGCT | PREVIEW       | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5228                    |                         |
| MSP430F5228IZQE  | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 360         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5228                    |                         |
| MSP430F5228IZQER | PREVIEW       | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 2500        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5228                    |                         |
| MSP430F5229IRGCR | ACTIVE        | VQFN                       | RGC                | 64   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5229                    | <a href="#">Samples</a> |
| MSP430F5229IRGCT | ACTIVE        | VQFN                       | RGC                | 64   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR  |              | F5229                    | <a href="#">Samples</a> |
| MSP430F5229IYFFR | PREVIEW       | DSBGA                      | YFF                | 64   | 2500        | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5229IYFFT | PREVIEW       | DSBGA                      | YFF                | 64   | 250         | TBD                        | Call TI          | Call TI              |              |                          |                         |
| MSP430F5229IZQE  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 360         | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5229                    | <a href="#">Samples</a> |
| MSP430F5229IZQER | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQE                | 80   | 2500        | Green (RoHS<br>& no Sb/Br) | SNAGCU           | Level-3-260C-168 HR  |              | F5229                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

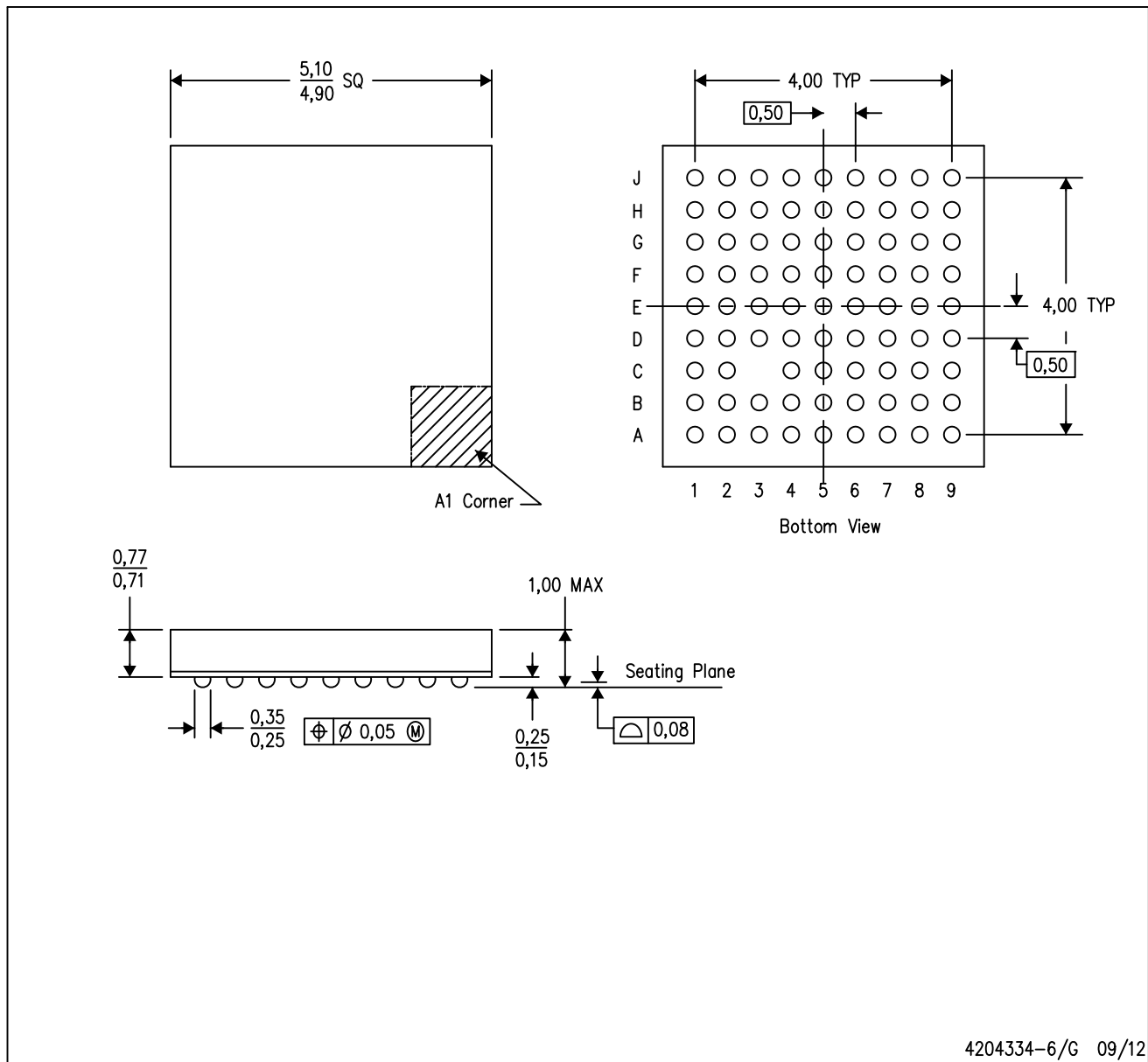
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ZQE (S-PBGA-N80)

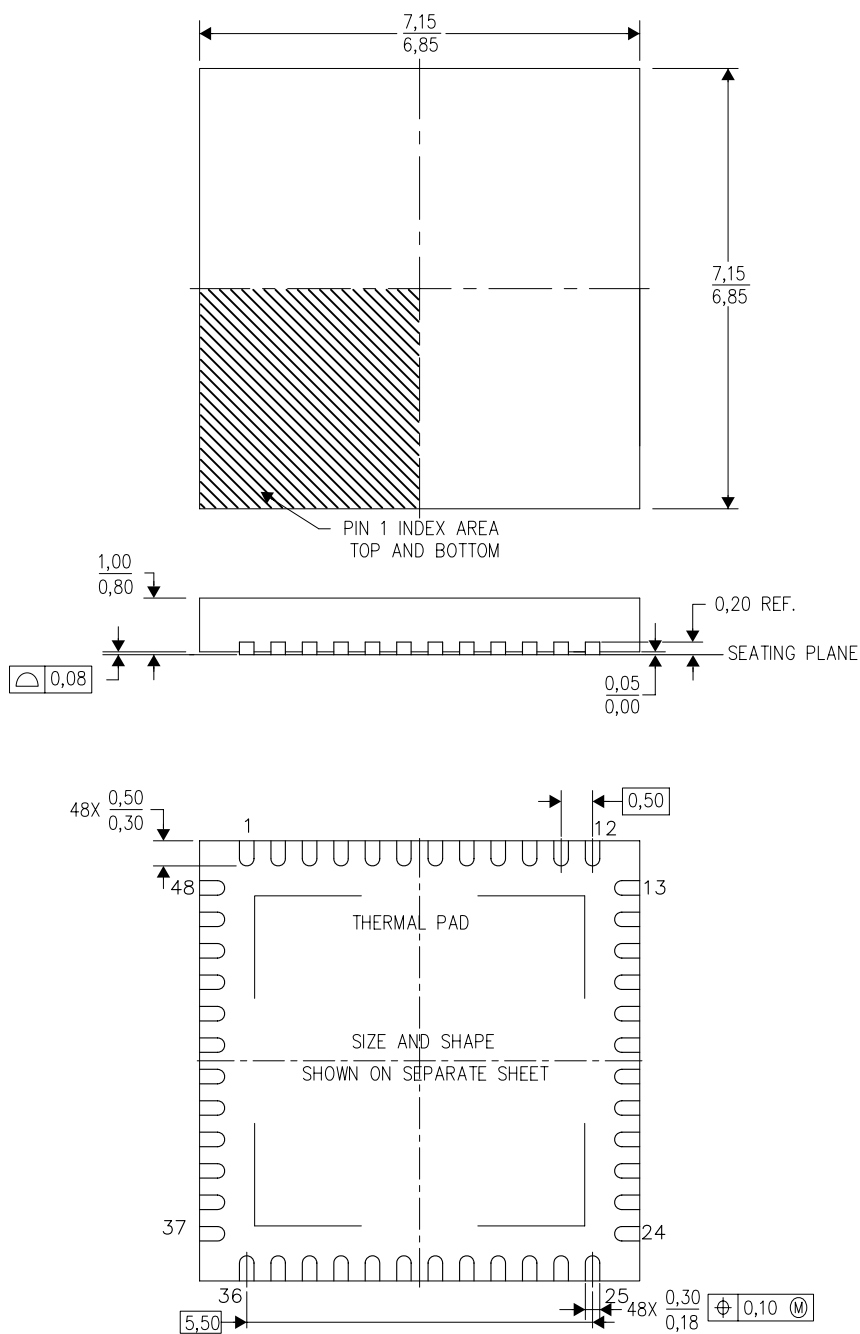
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225
  - D. This is a Pb-free solder ball design.

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

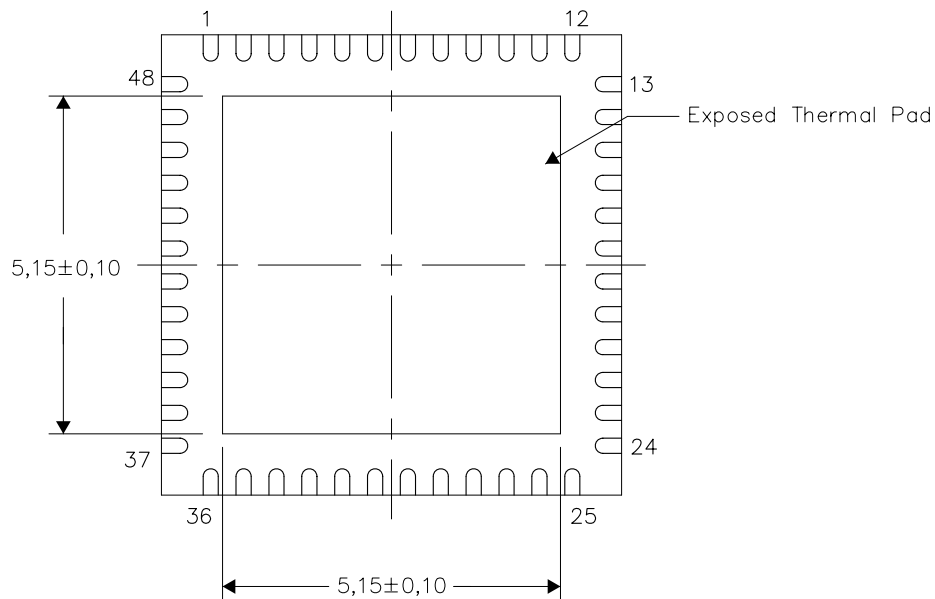
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

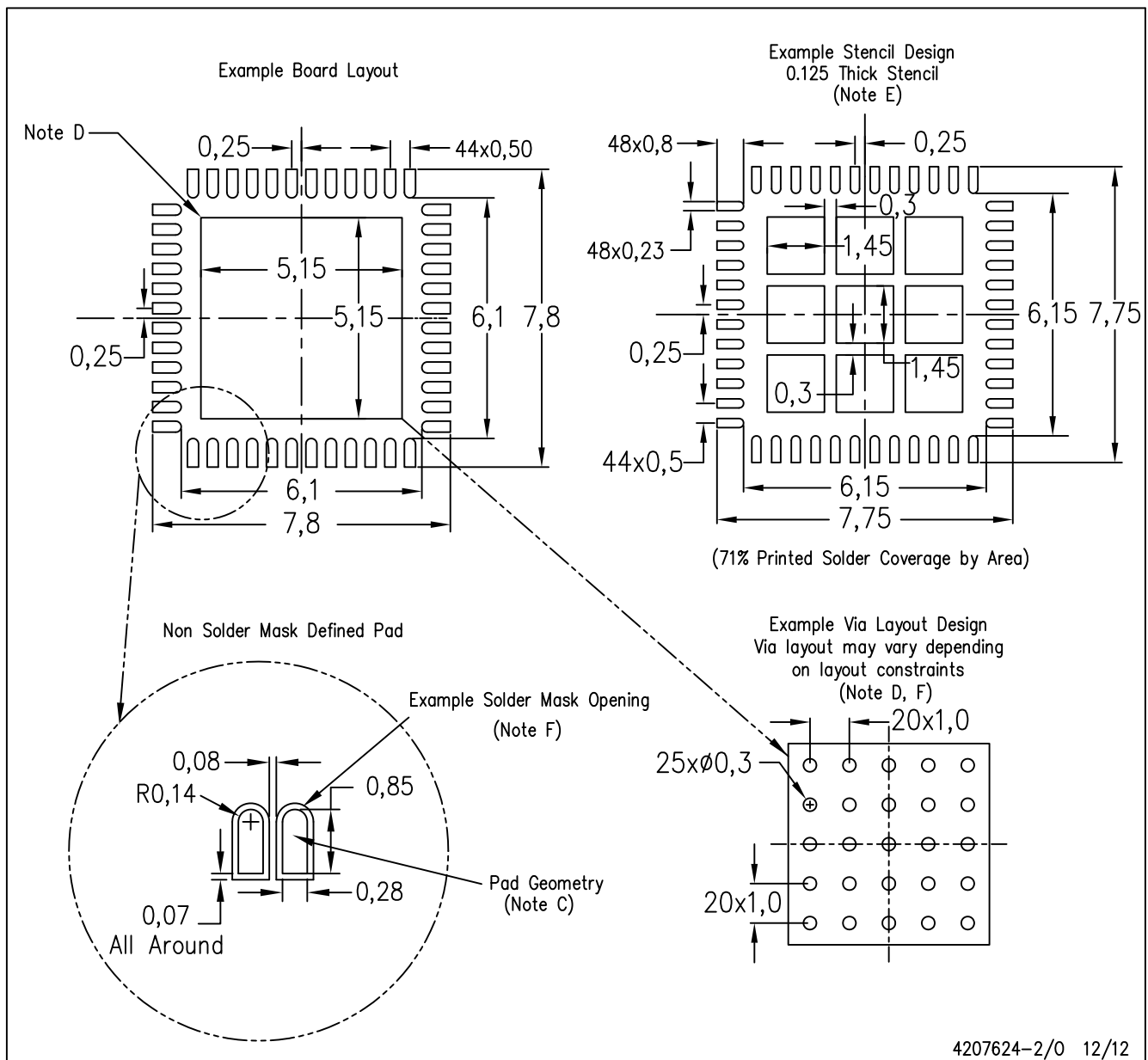
Exposed Thermal Pad Dimensions

4206354-2/R 08/11

NOTE: All linear dimensions are in millimeters

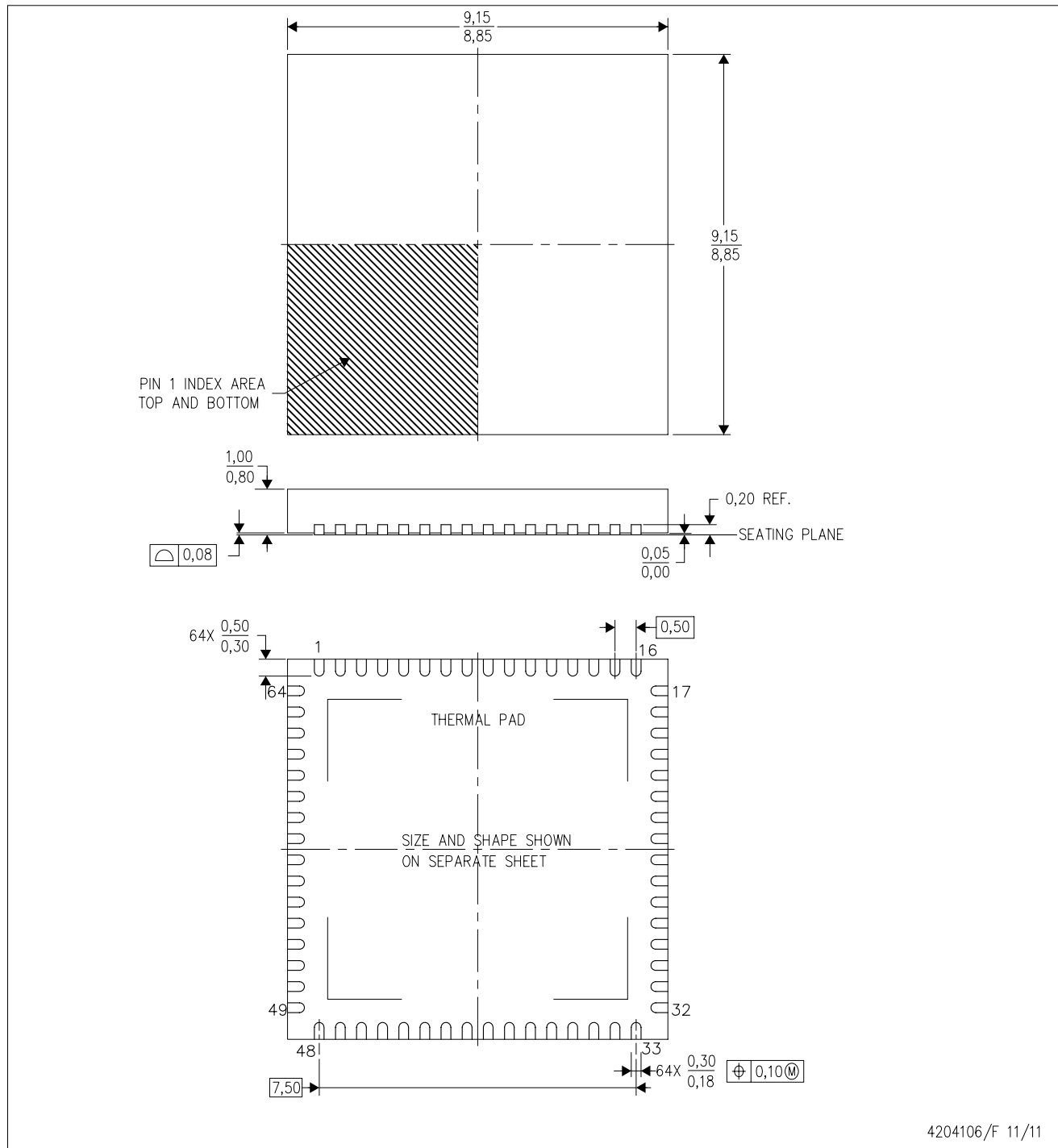
RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

## THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

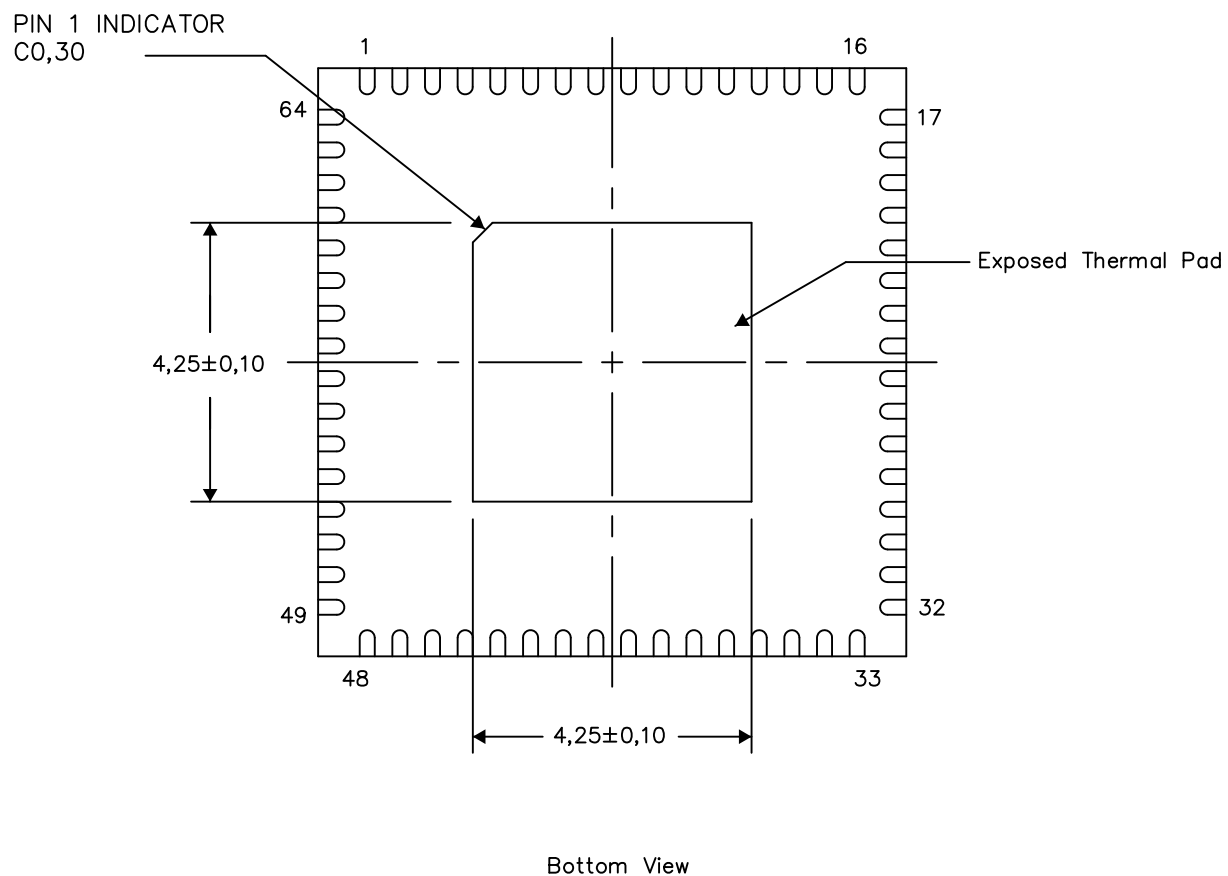
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



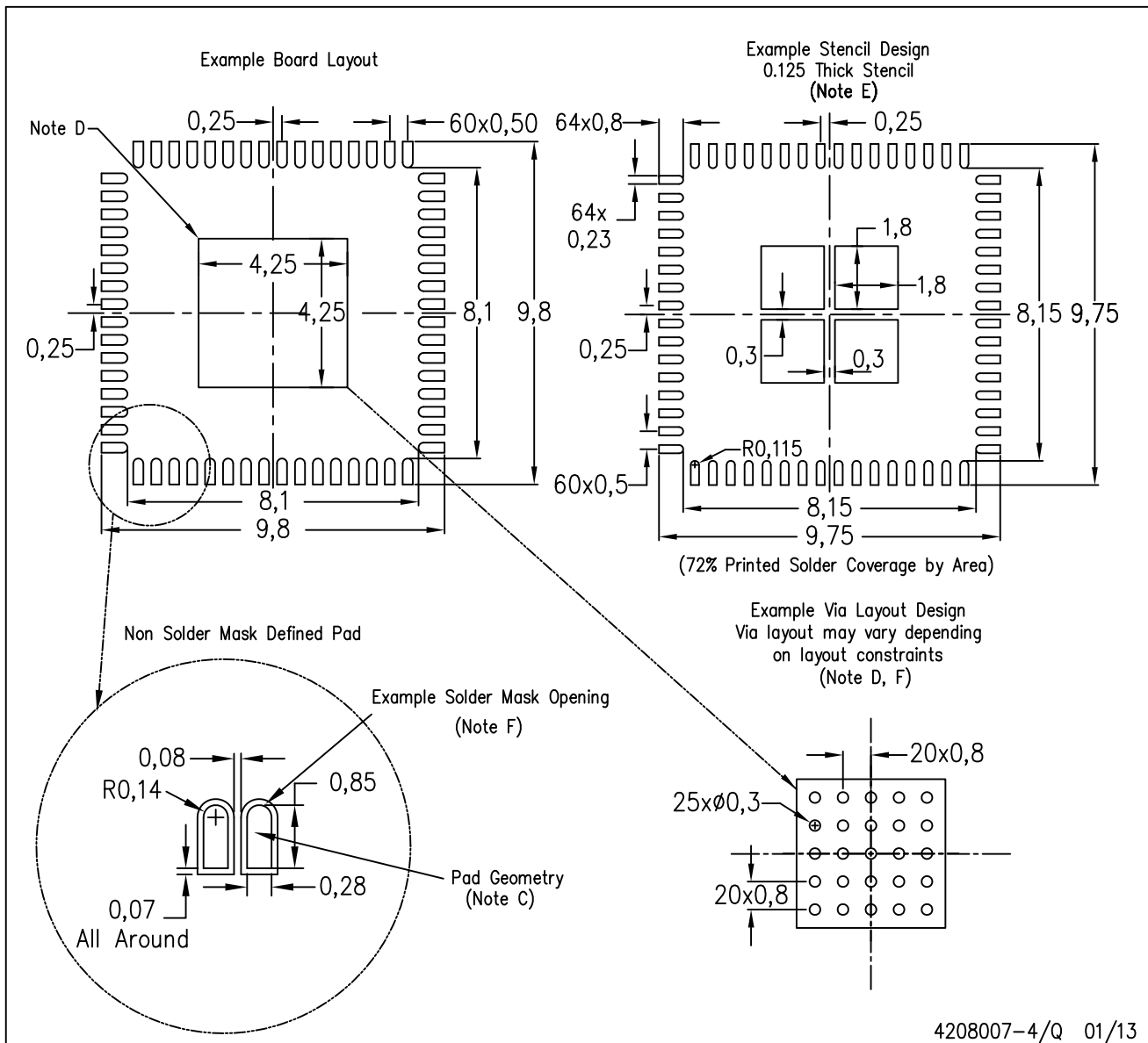
Exposed Thermal Pad Dimensions

4206192-3/W 01/13

NOTE: A. All linear dimensions are in millimeters

## RGC (S-PVQFN-N64)

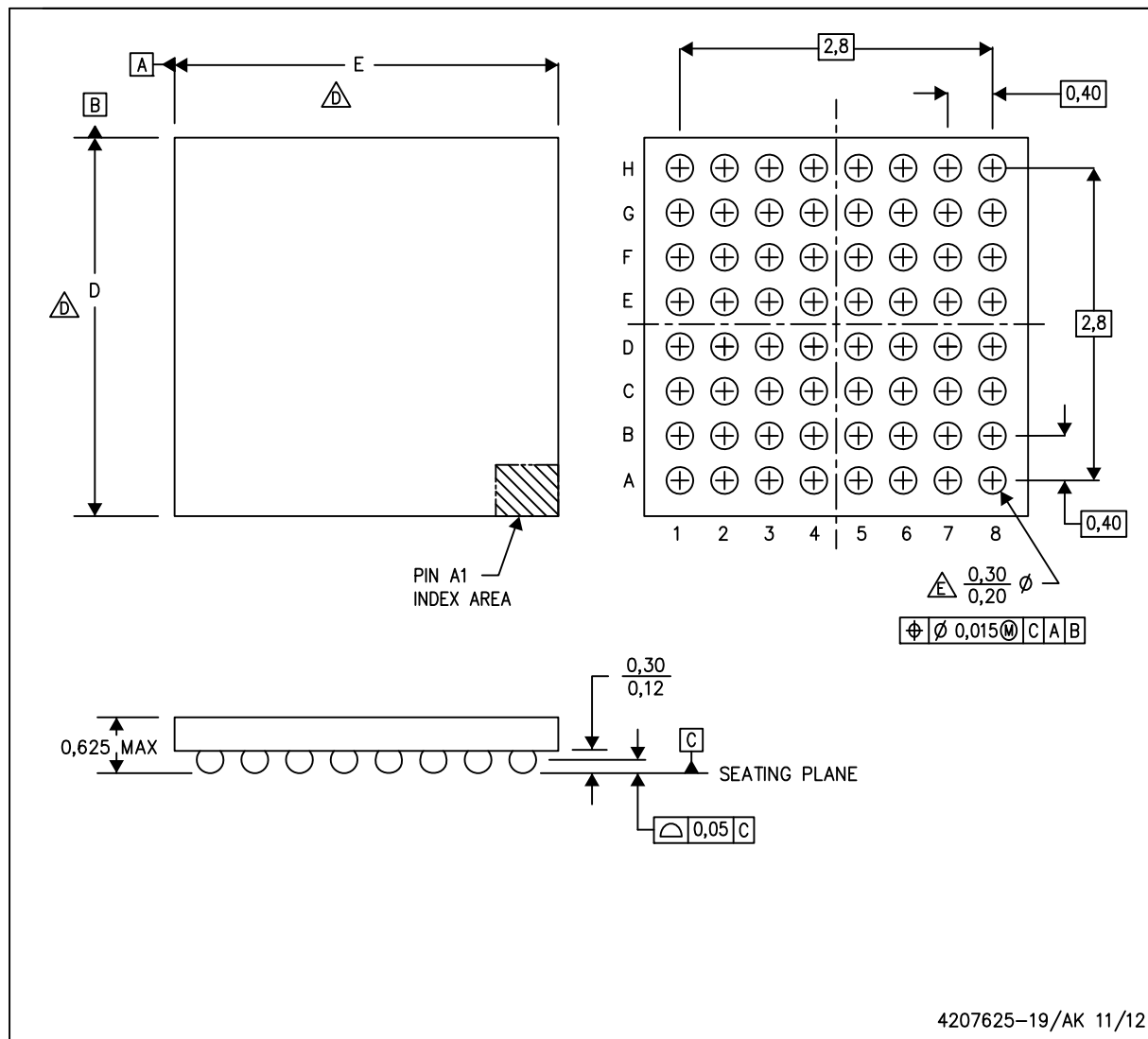
## PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

YFF (R-XBGA-N64)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. Reference Product Data Sheet for array population.
  - F. This package contains Pb-free balls.



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| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
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|                               |                                                                                          |
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