MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply Voltage Range: 2.2 V to 3.6 V
- Ultralow Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    312 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    140 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    Real-Time Clock With Crystal , Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
    2.6 µA at 3.0 V (Typical)
    Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up:
    1.8 µA at 3.0 V (Typical)
  - Off Mode (LPM4):
    Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up:
    1.69 µA at 3.0 V (Typical)
- Wake-Up From Standby Mode in Less Than 5 µs
- 16-Bit RISC Architecture
  - Extended Memory
  - Up to 18-MHz System Clock
- Flexible Power Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power/Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals
  - High-Frequency Crystals up to 32 MHz
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Up to Four Universal Serial Communication Interfaces
  - USCI_A0, USCI_A1, USCI_A2, and USCI_A3 Each Supporting
    - Enhanced UART supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0, USCI_B1, USCI_B2, and USCI_B3 Each Supporting
    - I^2C^{TM}
    - Synchronous SPI
- 12-Bit Analog-to-Digital (A/D) Converter
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - 14 External Channels, 2 Internal Channels
- Hardware Multiplier Supporting 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three Channel Internal DMA
- Basic Timer With Real-Time Clock Feature
- Family Members are Summarized in Table 1
- For Complete Module Descriptions, See the *MSP430x5xx Family User's Guide* (SLAU208)

DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 5 µs.

The MSP430F543x and MSP430F541x series are microcontroller configurations with three 16-bit timers, a high performance 12-bit analog-to-digital (A/D) converter, up to four universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and up to 87 I/O pins.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

Family members available are summarized in Table 1.

Table 1. Family Members

Device	Flash (KB)	SRAM (KB)	Timer_A(1)	Timer_B(2)	USCI		ADC12_A (Ch)	I/O	Package Type
					Channel A: UART/IrDA/ SPI	Channel B: SPI/I²C			
MSP430F5438	256	16	5, 3	7	4	4	14 ext / 2 int	87	100 PZ
MSP430F5437	256	16	5, 3	7	2	2	14 ext / 2 int	67	80 PN
MSP430F5436	192	16	5, 3	7	4	4	14 ext / 2 int	87	100 PZ
MSP430F5435	192	16	5, 3	7	2	2	14 ext / 2 int	67	80 PN
MSP430F5419	128	16	5, 3	7	4	4	14 ext / 2 int	87	100 PZ
MSP430F5418	128	16	5, 3	7	2	2	14 ext / 2 int	67	80 PN

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

(2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

Ordering Information(1)

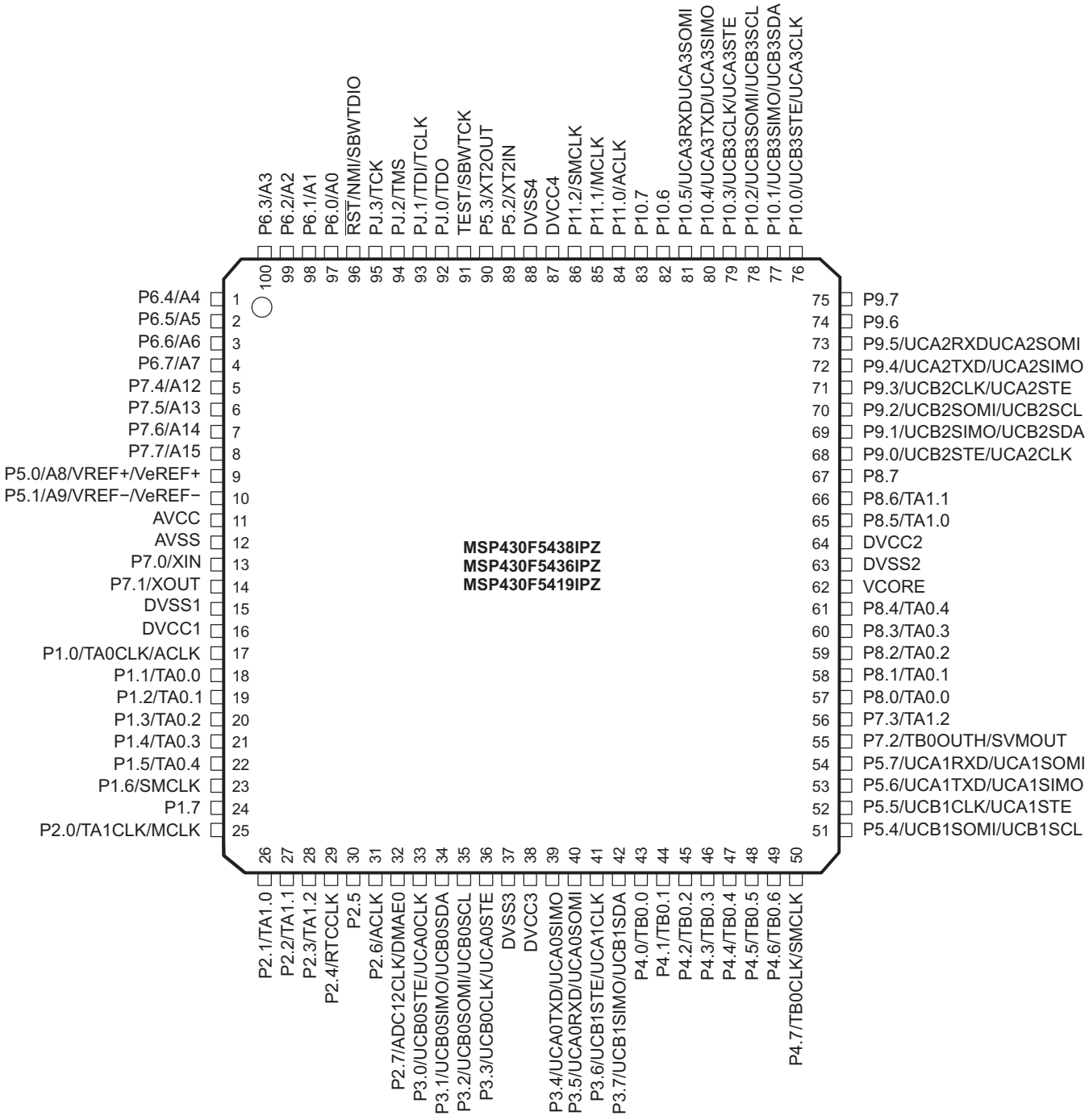
T_A	PACKAGED DEVICES(2)	
	PLASTIC 100-PIN LQFP (PZ)	PLASTIC 80-PIN LQFP (PN)
–40°C to 85°C	MSP430F5438IPZ	MSP430F5437IPN
	MSP430F5436IPZ	MSP430F5435IPN
	MSP430F5419IPZ	MSP430F5418IPN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

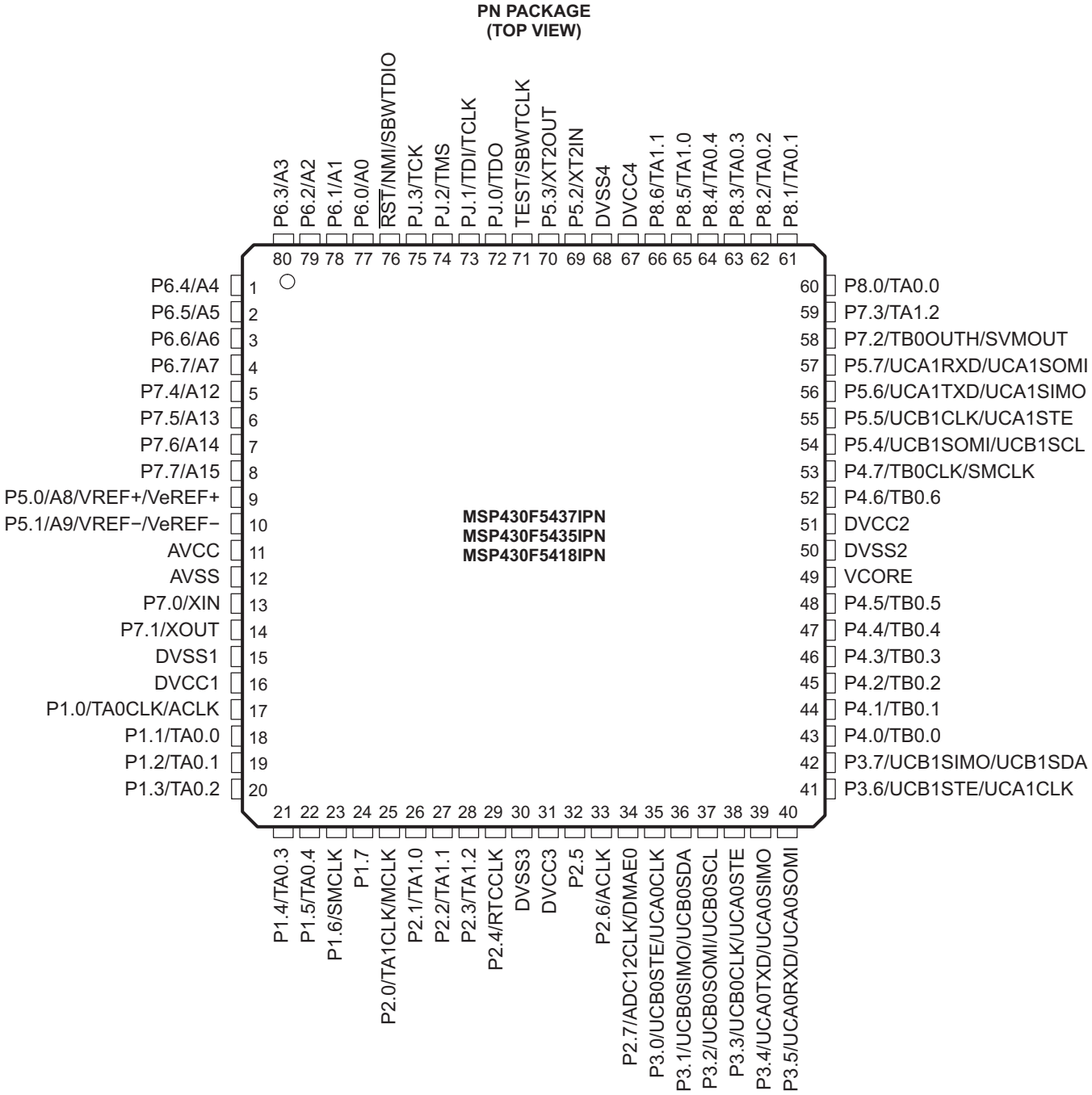
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Pin Designation, MSP430F5438IPZ, MSP430F5436IPZ, MSP430F5419IPZ

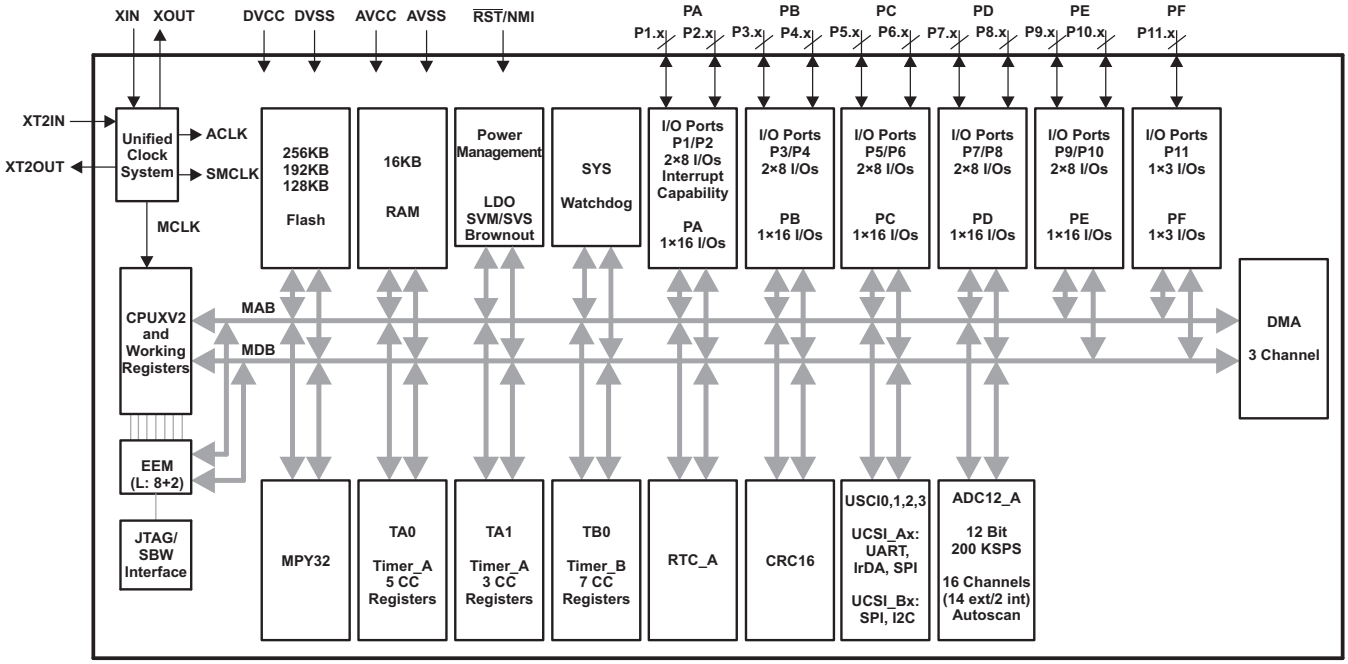
PZ PACKAGE
(TOP VIEW)



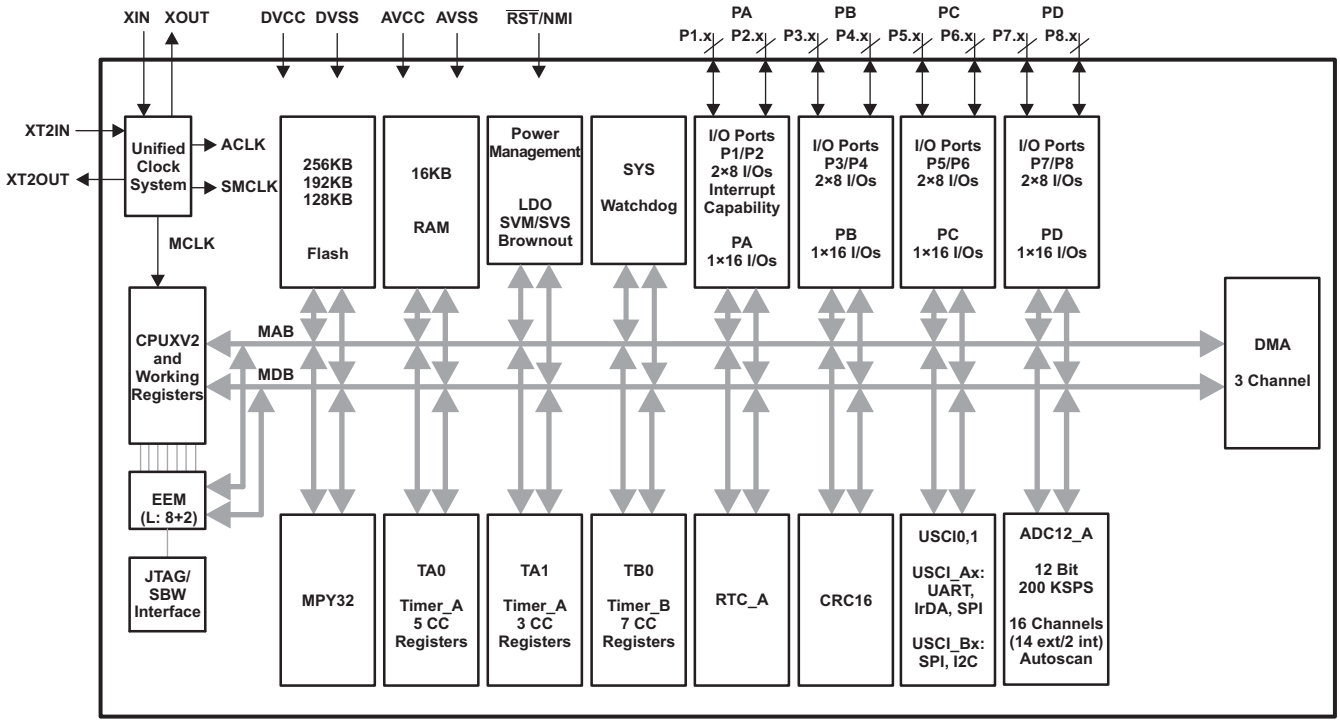
Pin Designation, MSP430F5437IPN, MSP430F5435IPN, MSP430F5418IPN



Functional Block Diagram, MSP430F5438IPZ, MSP430F5436IPZ, MSP430F5419IPZ,



Functional Block Diagram, MSP430F5437IPN, MSP430F5435IPN, MSP430F5418IPN



TERMINAL FUNCTIONS

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	PN		
P6.4/A4	1	1	I/O	General-purpose digital I/O Analog input A4 – ADC
P6.5/A5	2	2	I/O	General-purpose digital I/O Analog input A5 – ADC
P6.6/A6	3	3	I/O	General-purpose digital I/O Analog input A6 – ADC
P6.7/A7	4	4	I/O	General-purpose digital I/O Analog input A7 – ADC
P7.4/A12	5	5	I/O	General-purpose digital I/O Analog input A12 –ADC
P7.5/A13	6	6	I/O	General-purpose digital I/O Analog input A13 – ADC
P7.6/A14	7	7	I/O	General-purpose digital I/O Analog input A14 – ADC
P7.7/A15	8	8	I/O	General-purpose digital I/O Analog input A15 – ADC
P5.0/A8/VREF+/VeREF+	9	9	I/O	General-purpose digital I/O Analog input A8 – ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P5.1/A9/VREF-/VeREF-	10	10	I/O	General-purpose digital I/O Analog input A9 – ADC Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
AVCC	11	11		Analog power supply
AVSS	12	12		Analog ground supply
P7.0/XIN	13	13	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P7.1/XOUT	14	14	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
DVSS1	15	15		Digital ground supply
DVCC1	16	16		Digital power supply
P1.0/TA0CLK/ACLK	17	17	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8)
P1.1/TA0.0	18	18	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	19	19	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	20	20	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	21	21	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	22	22	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/SMCLK	23	23	I/O	General-purpose digital I/O with port interrupt SMCLK output
P1.7	24	24	I/O	General-purpose digital I/O with port interrupt
P2.0/TA1CLK/MCLK	25	25	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input MCLK output

(1) I = input, O = output, N/A = not available on this package offering

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.			
	PZ	PN		
P2.1/TA1.0	26	26	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.2/TA1.1	27	27	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.3/TA1.2	28	28	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.4/RTCCLK	29	29	I/O	General-purpose digital I/O with port interrupt RTCCLK output
P2.5	30	32	I/O	General-purpose digital I/O with port interrupt
P2.6/ACLK	31	33	I/O	General-purpose digital I/O with port interrupt ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P2.7/ADC12CLK/DMAE0	32	34	I/O	General-purpose digital I/O with port interrupt Conversion clock output ADC DMA external trigger input
P3.0/UCB0STE/UCA0CLK	33	35	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.1/UCB0SIMO/UCB0SDA	34	36	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.2/UCB0SOMI/UCB0SCL	35	37	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.3/UCB0CLK/UCA0STE	36	38	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
DVSS3	37	30		Digital ground supply
DVCC3	38	31		Digital power supply
P3.4/UCA0TXD/UCA0SIMO	39	39	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.5/UCA0RXD/UCA0SOMI	40	40	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P3.6/UCB1STE/UCA1CLK	41	41	I/O	General-purpose digital I/O Slave transmit enable – USCI_B1 SPI mode Clock signal input – USCI_A1 SPI slave mode Clock signal output – USCI_A1 SPI master mode
P3.7/UCB1SIMO/UCB1SDA	42	42	I/O	General-purpose digital I/O Slave in, master out – USCI_B1 SPI mode I2C data – USCI_B1 I2C mode
P4.0/TB0.0	43	43	I/O	General-purpose digital I/O TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P4.1/TB0.1	44	44	I/O	General-purpose digital I/O TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P4.2/TB0.2	45	45	I/O	General-purpose digital I/O TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P4.3/TB0.3	46	46	I/O	General-purpose digital I/O TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output
P4.4/TB0.4	47	47	I/O	General-purpose digital I/O TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output
P4.5/TB0.5	48	48	I/O	General-purpose digital I/O TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	PN		
P4.6/TB0.6	49	52	I/O	General-purpose digital I/O TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output
P4.7/TB0CLK/SMCLK	50	53	I/O	General-purpose digital I/O TB0 clock input SMCLK output
P5.4/UCB1SOMI/UCB1SCL	51	54	I/O	General-purpose digital I/O Slave out, master in – USCI_B1 SPI mode I2C clock – USCI_B1 I2C mode
P5.5/UCB1CLK/UCA1STE	52	55	I/O	General-purpose digital I/O Clock signal input – USCI_B1 SPI slave mode Clock signal output – USCI_B1 SPI master mode Slave transmit enable – USCI_A1 SPI mode
P5.6/UCA1TXD/UCA1SIMO	53	56	I/O	General-purpose digital I/O Transmit data – USCI_A1 UART mode Slave in, master out – USCI_A1 SPI mode
P5.7/UCA1RXD/UCA1SOMI	54	57	I/O	General-purpose digital I/O Receive data – USCI_A1 UART mode Slave out, master in – USCI_A1 SPI mode
P7.2/TB0OUTH/SVMOUT	55	58	I/O	General-purpose digital I/O Switch all PWM outputs high impedance – Timer TB0 SVM output
P7.3/TA1.2	56	59	I/O	General-purpose digital I/O TA1 CCR2 capture: CCI2B input, compare: Out2 output
P8.0/TA0.0	57	60	I/O	General-purpose digital I/O TA0 CCR0 capture: CCI0B input, compare: Out0 output
P8.1/TA0.1	58	61	I/O	General-purpose digital I/O TA0 CCR1 capture: CCI1B input, compare: Out1 output
P8.2/TA0.2	59	62	I/O	General-purpose digital I/O TA0 CCR2 capture: CCI2B input, compare: Out2 output
P8.3/TA0.3	60	63	I/O	General-purpose digital I/O TA0 CCR3 capture: CCI3B input, compare: Out3 output
P8.4/TA0.4	61	64	I/O	General-purpose digital I/O TA0 CCR4 capture: CCI4B input, compare: Out4 output
VCORE(2)	62	49		Regulated core power supply output (internal use only, no external current loading)
DVSS2	63	50		Digital ground supply
DVCC2	64	51		Digital power supply
P8.5/TA1.0	65	65	I/O	General-purpose digital I/O TA1 CCR0 capture: CCI0B input, compare: Out0 output
P8.6/TA1.1	66	66	I/O	General-purpose digital I/O TA1 CCR1 capture: CCI1B input, compare: Out1 output
P8.7	67	N/A	I/O	General-purpose digital I/O
P9.0/UCB2STE/UCA2CLK	68	N/A	I/O	General-purpose digital I/O Slave transmit enable – USCI_B2 SPI mode Clock signal input – USCI_A2 SPI slave mode Clock signal output – USCI_A2 SPI master mode
P9.1/UCB2SIMO/UCB2SDA	69	N/A	I/O	General-purpose digital I/O Slave in, master out – USCI_B2 SPI mode I2C data – USCI_B2 I2C mode
P9.2/UCB2SOMI/UCB2SCL	70	N/A	I/O	General-purpose digital I/O Slave out, master in – USCI_B2 SPI mode I2C clock – USCI_B2 I2C mode

(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.			
	PZ	PN		
P9.3/UCB2CLK/UCA2STE	71	N/A	I/O	General-purpose digital I/O Clock signal input – USCI_B2 SPI slave mode Clock signal output – USCI_B2 SPI master mode Slave transmit enable – USCI_A2 SPI mode
P9.4/UCA2TXD/UCA2SIMO	72	N/A	I/O	General-purpose digital I/O Transmit data – USCI_A2 UART mode Slave in, master out – USCI_A2 SPI mode
P9.5/UCA2RXD/UCA2SOMI	73	N/A	I/O	General-purpose digital I/O Receive data – USCI_A2 UART mode Slave out, master in – USCI_A2 SPI mode
P9.6	74	N/A	I/O	General-purpose digital I/O
P9.7	75	N/A	I/O	General-purpose digital I/O
P10.0/UCB3STE/UCA3CLK	76	N/A	I/O	General-purpose digital I/O Slave transmit enable – USCI_B3 SPI mode Clock signal input – USCI_A3 SPI slave mode Clock signal output – USCI_A3 SPI master mode
P10.1/UCB3SIMO/UCB3SDA	77	N/A	I/O	General-purpose digital I/O Slave in, master out – USCI_B3 SPI mode I2C data – USCI_B3 I2C mode
P10.2/UCB3SOMI/UCB3SCL	78	N/A	I/O	General-purpose digital I/O Slave out, master in – USCI_B3 SPI mode I2C clock – USCI_B3 I2C mode
P10.3/UCB3CLK/UCA3STE	79	N/A	I/O	General-purpose digital I/O Clock signal input – USCI_B3 SPI slave mode Clock signal output – USCI_B3 SPI master mode Slave transmit enable – USCI_A3 SPI mode
P10.4/UCA3TXD/UCA3SIMO	80	N/A	I/O	General-purpose digital I/O Transmit data – USCI_A3 UART mode Slave in, master out – USCI_A3 SPI mode
P10.5/UCA3RXD/UCA3SOMI	81	N/A	I/O	General-purpose digital I/O Receive data – USCI_A3 UART mode Slave out, master in – USCI_A3 SPI mode
P10.6	82	N/A	I/O	General-purpose digital I/O
P10.7	83	N/A	I/O	General-purpose digital I/O
P11.0/ACLK	84	N/A	I/O	General-purpose digital I/O ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P11.1/MCLK	85	N/A	I/O	General-purpose digital I/O MCLK output
P11.2/SMCLK	86	N/A	I/O	General-purpose digital I/O SMCLK output
DVCC4	87	67		Digital power supply
DVSS4	88	68		Digital ground supply
P5.2/XT2IN	89	69	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	90	70	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK[3]	91	71	I	Test mode pin – select digital I/O on JTAG pins Spy-bi-wire input clock
PJ.0/TDO[4]	92	72	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK[4]	93	73	I/O	General-purpose digital I/O Test data input or test clock input

(3) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions
(4) See JTAG Operation for use with JTAG function.

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	PN		
PJ.2/TMS(4)	94	74	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK(4)	95	75	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO(3)	96	76	I/O	Reset input active low Non-maskable interrupt input Spy-bi-wire data input/output
P6.0/A0	97	77	I/O	General-purpose digital I/O Analog input A0 – ADC
P6.1/A1	98	78	I/O	General-purpose digital I/O Analog input A1 – ADC
P6.2/A2	99	79	I/O	General-purpose digital I/O Analog input A2 – ADC
P6.3/A3	100	80	I/O	General-purpose digital I/O Analog input A3 – ADC
Reserved	N/A	N/A		

SHORT-FORM DESCRIPTION

CPU

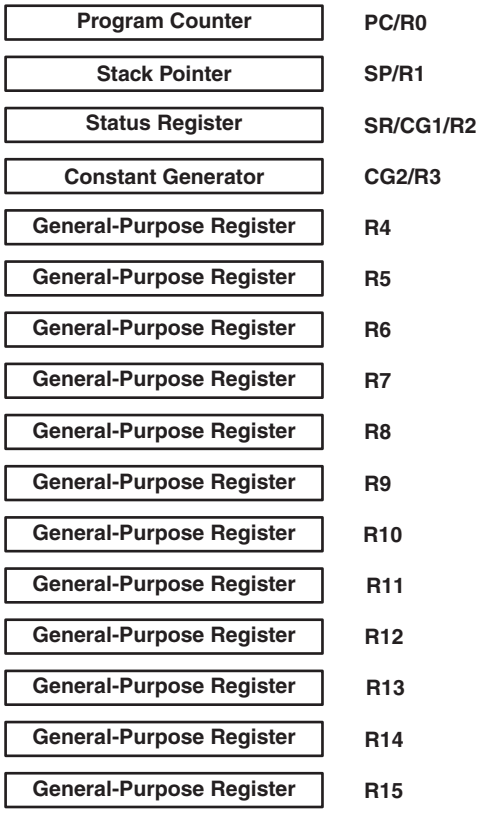
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation PMM Password Violation	WDTIFG, KEYV (SYSRSTIV)(1) (2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV)(1) (2)	(Non)maskable	0FFFAh	61
TB0	TBCCR0 CCIFG0 (3)	Maskable	0FFF8h	60
TB0	TBCCR1 CCIFG1 ... TBCCR6 CCIFG6, TBIFG (TBIV)(1) (3)	Maskable	0FFF6h	59
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF4h	58
USCI_A0 Receive/Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (3)	Maskable	0FFF2h	57
USCI_B0 Receive/Transmit	UCB0RXIFG, UCB0TXIFG (UCAB0IV)(1) (3)	Maskable	0FFF0h	56
ADC12_A	ADC12IFG0 ... ADC12IFG15 (ADC12IV)(1) (3)	Maskable	0FFEEh	55
TA0	TA0CCR0 CCIFG0(3)	Maskable	0FFECh	54
TA0	TA0CCR1 CCIFG1 ... TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (3)	Maskable	0FFEAh	53
USCI_A2 Receive/Transmit	UCA2RXIFG, UCA2TXIFG (UCA2IV)(1) (3)	Maskable	0FFE8h	52
USCI_B2 Receive/Transmit	UCB2RXIFG, UCB2TXIFG (UCB2IV)(1) (3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1) (3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 ... TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1) (3)	Maskable	0FFDEh	47
USCI_A1 Receive/Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (3)	Maskable	0FFDCh	46
USCI_B1 Receive/Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (3)	Maskable	0FFDAh	45
USCI_A3 Receive/Transmit	UCA3RXIFG, UCA3TXIFG (UCA3IV)(1) (3)	Maskable	0FFD8h	44
USCI_B3 Receive/Transmit	UCB3RXIFG, UCB3TXIFG (UCB3IV)(1) (3)	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1) (3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1) (3)	Maskable	0FFD2h	41
Reserved	Reserved(4)		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

		MSP430F5419 MSP430F5418	MSP430F5436 MSP430F5435	MSP430F5438 MSP430F5437
Memory (flash) Main: interrupt vector Main: code memory	Total Size Flash Flash	128 KB 00FFFFh–00FF80h 025BFFh–005C00h	192 KB 00FFFFh–00FF80h 035BFFh–005C00h	256 KB 00FFFFh–00FF80h 045BFFh–005C00h
Main: code memory	Bank 3	N/A	23 KB 035BFFh–030000h	64 KB 03FFFFh–030000h
	Bank 2	23 KB 025BFFh–020000h	64 KB 02FFFFh–020000h	64 KB 02FFFFh–020000h
	Bank 1	64 KB 01FFFFh–010000h	64 KB 01FFFFh–010000h	64 KB 01FFFFh–010000h
	Bank 0	41 KB 00FFFFh–005C00h	41 KB 00FFFFh–005C00h	64 KB 045BFFh–040000h 00FFFFh–005C00h
RAM	Size	16 KB	16 KB	16 KB
	Sector 3	4 KB 005BFFh–004C00h	4 KB 005BFFh–004C00h	4 KB 005BFFh–004C00h
	Sector 2	4 KB 004BFFh–003C00h	4 KB 004BFFh–003C00h	4 KB 004BFFh–003C00h
	Sector 1	4 KB 003BFFh–002C00h	4 KB 003BFFh–002C00h	4 KB 003BFFh–002C00h
	Sector 0	4 KB 002BFFh–001C00h	4 KB 002BFFh–001C00h	4 KB 002BFFh–001C00h
Information memory (flash)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL)[(1)] memory (flash)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–000000h	4KB 000FFFh–000000h	4KB 000FFFh–000000h

(1) The BSL area contains a Texas Instruments provided BSL and cannot be modified.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory via the BSL is protected by an user-defined password. Usage of the BSL requires four pins as shown in Table 3. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

Table 3. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
RST/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 4. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*, literature number SLAU278.

Table 4. JTAG Pin Requirements and Functions

DEVICE SIGNAL	Direction	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input/TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 5. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*, literature number SLAU278.

Table 5. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	Direction	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in Memory Organization.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.
- For Devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx Family User's Guide*, literature number SLAU208.

Digital I/O

There are up to ten 8-bit I/O ports implemented: For 100-pin options, P1 through P10 are complete. P11 contains three individual I/O ports. For 80-pin options, P1 through P7 are complete. P8 contains seven individual I/O ports. P9 through P11 do not exist. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM5 wakeup input capability is available for all bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P11) or word-wise in pairs (PA through PF).

Oscillator and System Clock

The clock system in the MSP430x5xx family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT1 HF mode or XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 6. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV , System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Reserved	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		FLL unlock (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV , System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 7. DMA Trigger Assignments (1)

Trigger	Channel		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
6	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
7	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx	ADC12IFGx	ADC12IFGx
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.

Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430F5438, MSP430F5436, and MSP430F5419 include four complete USCI modules (n = 0 to 3). The MSP430F5437, MSP430F5435, and MSP430F5418 include two complete USCI modules (n = 0 to 1).

TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 8. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
17-P1.0	17-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
17-P1.0	17-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
18-P1.1	18-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	18-P1.1	18-P1.1
57-P8.0	60-P8.0	TA0.0	CCI0B				57-P8.0	60-P8.0
		DV_{SS}	GND				ADC12 (internal) ADC12SHSx = {1}	ADC12 (internal) ADC12SHSx = {1}
		DV_{CC}	V_{CC}					
19-P1.2	19-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	19-P1.2	19-P1.2
58-P8.1	61-P8.1	TA0.1	CCI1B				58-P8.1	61-P8.1
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
20-P1.3	20-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	20-P1.3	20-P1.3
59-P8.2	62-P8.2	TA0.2	CCI2B				59-P8.2	62-P8.2
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
21-P1.4	21-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	21-P1.4	21-P1.4
60-P8.3	63-P8.3	TA0.3	CCI3B				60-P8.3	63-P8.3
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
22-P1.5	22-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	22-P1.5	22-P1.5
61-P8.4	64-P8.4	TA0.4	CCI4B				61-P8.4	64-P8.4
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 9. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
25-P2.0	25-P2.0	TA1CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
25-P2.0	25-P2.0	TA1CLK	$\overline{\text{TACLK}}$					
26-P2.1	26-P2.1	TA1.0	CCI0A	CCR0	TA0	TA1.0	26-P2.1	26-P2.1
65-P8.5	65-P8.5	TA1.0	CCI0B				65-P8.5	65-P8.5
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
27-P2.2	27-P2.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	27-P2.2	27-P2.2
66-P8.6	66-P8.6	TA1.1	CCI1B				66-P8.6	66-P8.6
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
28-P2.3	28-P2.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	28-P2.3	28-P2.3
56-P7.3	59-P7.3	TA1.2	CCI2B				56-P7.3	59-P7.3
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 10. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
50-P4.7	53-P4.7	TB0CLK	TBCLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
50-P4.7	53-P4.7	TB0CLK	$\overline{\text{TBCLK}}$					
43-P4.0	43-P4.0	TB0.0	CCI0A	CCR0	TB0	TB0.0	43-P4.0	43-P4.0
43-P4.0	43-P4.0	TB0.0	CCI0B				ADC12 (internal) ADC12SHSx = {2}	ADC12 (internal) ADC12SHSx = {2}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
44-P4.1	44-P4.1	TB0.1	CCI1A	CCR1	TB1	TB0.1	44-P4.1	44-P4.1
44-P4.1	44-P4.1	TB0.1	CCI1B				ADC12 (internal) ADC12SHSx = {3}	ADC12 (internal) ADC12SHSx = {3}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
45-P4.2	45-P4.2	TB0.2	CCI2A	CCR2	TB2	TB0.2	45-P4.2	45-P4.2
45-P4.2	45-P4.2	TB0.2	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
46-P4.3	46-P4.3	TB0.3	CCI3A	CCR3	TB3	TB0.3	46-P4.3	46-P4.3
46-P4.3	46-P4.3	TB0.3	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
47-P4.4	47-P4.4	TB0.4	CCI4A	CCR4	TB4	TB0.4	47-P4.4	47-P4.4
47-P4.4	47-P4.4	TB0.4	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
48-P4.5	48-P4.5	TB0.5	CCI5A	CCR5	TB5	TB0.5	48-P4.5	48-P4.5
48-P4.5	48-P4.5	TB0.5	CCI5B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
49-P4.6	52-P4.6	TB0.6	CCI6A	CCR6	TB6	TB0.6	49-P4.6	52-P4.6
		ACLK (internal)	CCI6B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

ADC12_A

The ADC12_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Embedded Emulation Module (EEM, L Version)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The L version of the EEM implemented on all devices has the following features:

- Eight hardware triggers/breakpoints on memory access
- Two hardware trigger/breakpoint on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers/breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

Peripheral File Map

Table 11. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (refer to Table 12)	0100h	000h - 01Fh
PMM (refer to Table 13)	0120h	000h - 00Fh
Flash Control (refer to Table 14)	0140h	000h - 00Fh
CRC16 (refer to Table 15)	0150h	000h - 007h
RAM Control (refer to Table 16)	0158h	000h - 001h
Watchdog (refer to Table 17)	015Ch	000h - 001h
UCS (refer to Table 18)	0160h	000h - 01Fh
SYS (refer to Table 19)	0180h	000h - 01Fh
Port P1/P2 (refer to Table 20)	0200h	000h - 01Fh
Port P3/P4 (refer to Table 21)	0220h	000h - 00Bh
Port P5/P6 (refer to Table 22)	0240h	000h - 00Bh
Port P7/P8 (refer to Table 23)	0260h	000h - 00Bh
Port P9/P10 (refer to Table 24)(1)	0280h	000h - 00Bh
Port P11 (refer to Table 25)(1)	02A0h	000h - 00Ah
Port PJ (refer to Table 26)	0320h	000h - 01Fh
TA0 (refer to Table 27)	0340h	000h - 02Eh
TA1 (refer to Table 28)	0380h	000h - 02Eh
TB0 (refer to Table 29)	03C0h	000h - 02Eh
Real Timer Clock (RTC_A) (refer to Table 30)	04A0h	000h - 01Bh
32-bit Hardware Multiplier (refer to Table 31)	04C0h	000h - 02Fh
DMA General Control (refer to Table 32)	0500h	000h - 00Fh
DMA Channel 0 (refer to Table 32)	0510h	000h - 00Ah
DMA Channel 1 (refer to Table 32)	0520h	000h - 00Ah
DMA Channel 2 (refer to Table 32)	0530h	000h - 00Ah
USCI_A0 (refer to Table 33)	05C0h	000h - 01Fh
USCI_B0 (refer to Table 34)	05E0h	000h - 01Fh
USCI_A1 (refer to Table 35)	0600h	000h - 01Fh
USCI_B1 (refer to Table 36)	0620h	000h - 01Fh
USCI_A2 (refer to Table 37)(1)	0640h	000h - 01Fh
USCI_B2 (refer to Table 38)(1)	0660h	000h - 01Fh
USCI_A3 (refer to Table 39)(1)	0680h	000h - 01Fh
USCI_B3 (refer to Table 40)(1)	06A0h	000h - 01Fh
ADC12_A (refer to Table 41)	0700h	000h - 03Eh

(1) Not available on 'F5437, 'F5435, 'F5418 devices

Table 12. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 13. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh

Table 14. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 15. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC result	CRC16INIRES	04h

Table 16. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 17. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 18. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 19. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 20. Port P1/P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 21. Port P3/P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 22. Port P5/P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 23. Port P7/P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pullup/pulldown enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 24. Port P9/P10 Registers (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 pullup/pulldown enable	P9REN	06h
Port P9 drive strength	P9DS	08h
Port P9 selection	P9SEL	0Ah
Port P10 input	P10IN	01h
Port P10 output	P10OUT	03h
Port P10 direction	P10DIR	05h
Port P10 pullup/pulldown enable	P10REN	07h
Port P10 drive strength	P10DS	09h
Port P10 selection	P10SEL	0Bh

Table 25. Port P11 Registers (Base Address: 02A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P11 input	P11IN	00h
Port P11 output	P11OUT	02h
Port P11 direction	P11DIR	04h
Port P11 pullup/pulldown enable	P11REN	06h
Port P11 drive strength	P11DS	08h
Port P11 selection	P11SEL	0Ah

Table 26. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 27. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 28. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 29. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 30. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 31. 32-bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 32. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 33. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 34. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 35. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 36. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 37. USCI_A2 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA2CTL1	00h
USCI control 0	UCA2CTL0	01h
USCI baud rate 0	UCA2BR0	06h
USCI baud rate 1	UCA2BR1	07h
USCI modulation control	UCA2MCTL	08h
USCI status	UCA2STAT	0Ah
USCI receive buffer	UCA2RXBUF	0Ch
USCI transmit buffer	UCA2TXBUF	0Eh
USCI LIN control	UCA2ABCTL	10h
USCI IrDA transmit control	UCA2IRTCTL	12h
USCI IrDA receive control	UCA2IRRCTL	13h
USCI interrupt enable	UCA2IE	1Ch
USCI interrupt flags	UCA2IFG	1Dh
USCI interrupt vector word	UCA2IV	1Eh

Table 38. USCI_B2 Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB2CTL1	00h
USCI synchronous control 0	UCB2CTL0	01h
USCI synchronous bit rate 0	UCB2BR0	06h
USCI synchronous bit rate 1	UCB2BR1	07h
USCI synchronous status	UCB2STAT	0Ah
USCI synchronous receive buffer	UCB2RXBUF	0Ch
USCI synchronous transmit buffer	UCB2TXBUF	0Eh
USCI I2C own address	UCB2I2COA	10h
USCI I2C slave address	UCB2I2CSA	12h
USCI interrupt enable	UCB2IE	1Ch
USCI interrupt flags	UCB2IFG	1Dh
USCI interrupt vector word	UCB2IV	1Eh

Table 39. USCI_A3 Registers (Base Address: 0680h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA3CTL1	00h
USCI control 0	UCA3CTL0	01h
USCI baud rate 0	UCA3BR0	06h
USCI baud rate 1	UCA3BR1	07h
USCI modulation control	UCA3MCTL	08h
USCI status	UCA3STAT	0Ah
USCI receive buffer	UCA3RXBUF	0Ch
USCI transmit buffer	UCA3TXBUF	0Eh
USCI LIN control	UCA3ABCTL	10h
USCI IrDA transmit control	UCA3IRTCTL	12h
USCI IrDA receive control	UCA3IRRCTL	13h
USCI interrupt enable	UCA3IE	1Ch
USCI interrupt flags	UCA3IFG	1Dh
USCI interrupt vector word	UCA3IV	1Eh

Table 40. USCI_B3 Registers (Base Address: 06A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB3CTL1	00h
USCI synchronous control 0	UCB3CTL0	01h
USCI synchronous bit rate 0	UCB3BR0	06h
USCI synchronous bit rate 1	UCB3BR1	07h
USCI synchronous status	UCB3STAT	0Ah
USCI synchronous receive buffer	UCB3RXBUF	0Ch
USCI synchronous transmit buffer	UCB3TXBUF	0Eh
USCI I2C own address	UCB3I2COA	10h
USCI I2C slave address	UCB3I2CSA	12h
USCI interrupt enable	UCB3IE	1Ch
USCI interrupt flags	UCB3IFG	1Dh
USCI interrupt vector word	UCB3IV	1Eh

Table 41. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Voltage V_{CC} applied at supply pins DVCC/AVCC to supply pins DVSS/AVSS	–0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE)(2)	–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range(3), T_{stg}	–55°C to 105°C
Maximum junction temperature, T_J	95°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

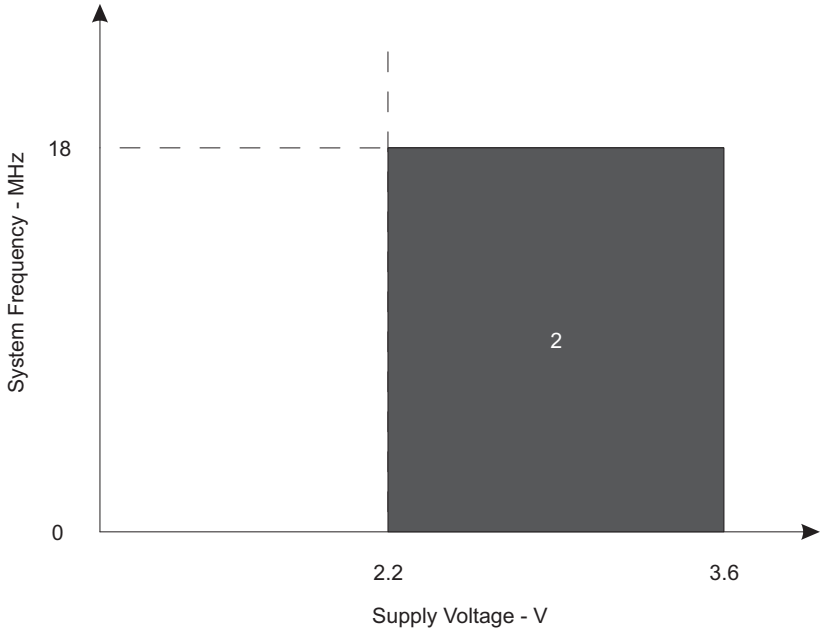
Thermal Packaging Characteristics

				VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air	Low-K board (JESD51-3)	QFP (PZ)	50.1	°C/W
			QFP (PN)	57.9	
		High-K board (JESD51-7)	QFP (PZ)	40.8	
			QFP (PN)	37.9	
θ_{JC}	Junction-to-case thermal resistance		QFP (PZ)	8.9	°C/W
			QFP (PN)	10.3	

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (V_{CC} = $DV_{CC1/2/3/4}$ = AV_{CC})(1)		2.2		3.6	V
V_{SS}	Supply voltage (V_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS}= AV_{SS})			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
CVCORE	Recommended capacitor at VCORE			470		nF
CDVCC/ CVCORE	Capacitor ratio of DV_{CC} to V_{CORE}		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(2) (3) (see Figure 1)	PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		18.0	MHz

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Frequency vs Supply Voltage

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	Execution Memory	V_{CC}	PMMCOREVx	Frequency ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)								UNIT
				1 MHz		4 MHz		8 MHz		16 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ Flash}$	Flash	3.0 V	2	0.37	0.45	1.27	1.47	2.50	2.84	5.00	5.56	mA
$I_{AM,\ RAM}$	RAM	3.0 V	2	0.20	0.29	0.60	0.72	1.12	1.27	2.20	2.60	mA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing worst case JMP $.
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	-40 °C		25 °C		55 °C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3) (4)	3.0 V	2	86	98	86	98	86	98	86	98	µA
I_{LPM2}	Low-power mode 2(5) (4)	3.0 V	2	8.0	15.6	8.0	15.6	8.0	15.6	8.0	15.6	µA
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6) (4)	3.0 V	2	2.3		2.6	3.37	4.5		7.9	15.6	µA
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7) (4)	3.0 V	2	1.39		1.80	2.30	2.95		6.9	14.6	µA
I_{LPM4}	Low-power mode 4(8) (4)	3.0 V	2	1.26		1.69	2.2	3.6		6.8	14.5	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz
(4) Current for brownout included. High and low side supervisor and monitors disabled (SVS_H, SVM_H, SVS_L, SVM_L). RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
(7) Current for watchdog timer and RTC clocked by ACLK included. For this condition, the VLO must be selected as the source for ACLK, MCLK, and SMCLK otherwise additional current will be drawn due to the REFO oscillator. ACLK = MCLK = SMCLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{VLO}$ = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

Schmitt-Trigger Inputs – General Purpose I/O(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Inputs – Ports P1 and P2(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing(2)	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag	2.2 V/3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1) (2)	1.8 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA (1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA (2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA (1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA (2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA (1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA (1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA (2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA (2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA (3)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA (2)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA (3)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA (2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA (3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA (2)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (3)		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Output Frequency – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.6/SMCLK (1) (2)	V_{CC} = 3 V PMMCOREVx = 2		25	MHz
f_{Port_CLK}	Clock output frequency	P1.0/TA0CLK/ACLK P1.6/SMCLK P2.0/TA1CLK/MCLK C_L = 20 pF (2)	V_{CC} = 3 V PMMCOREVx = 2		25	MHz

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

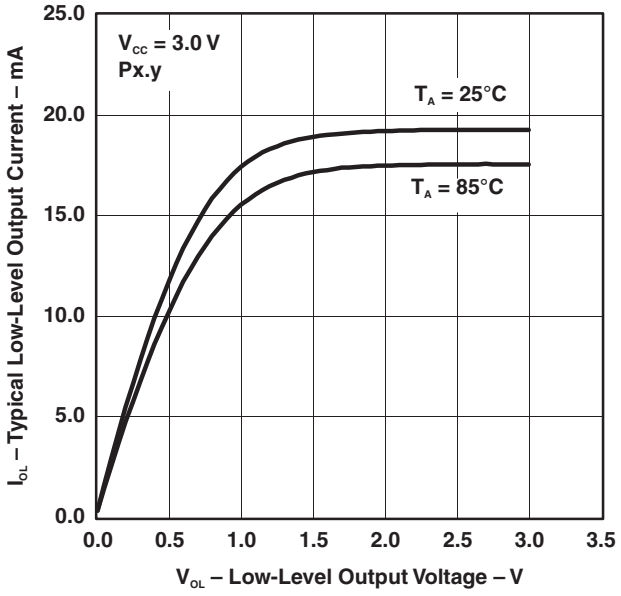


Figure 2.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

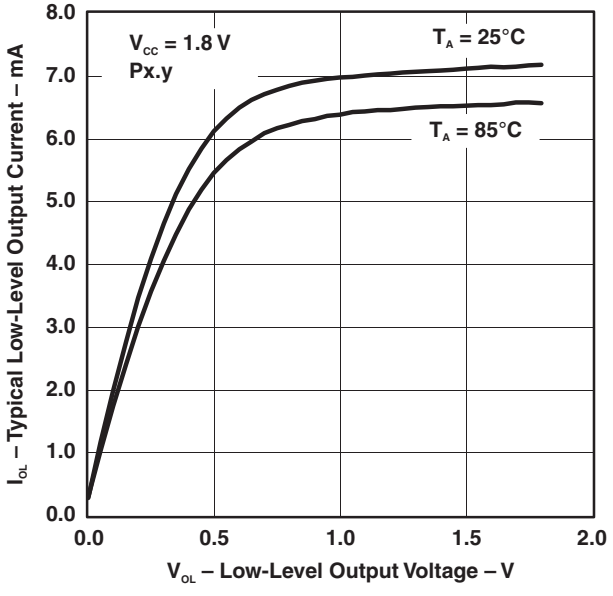


Figure 3.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

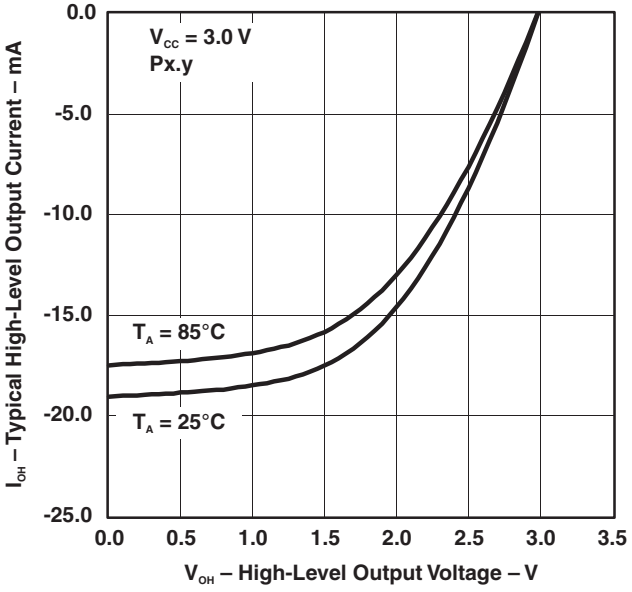


Figure 4.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

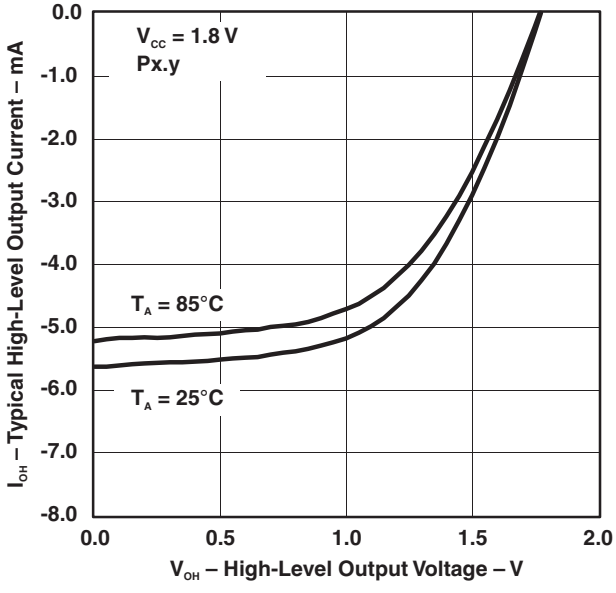


Figure 5.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

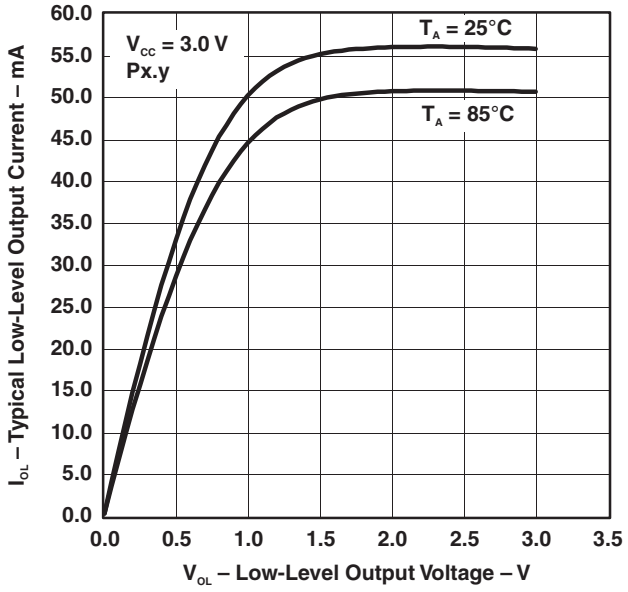


Figure 6.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

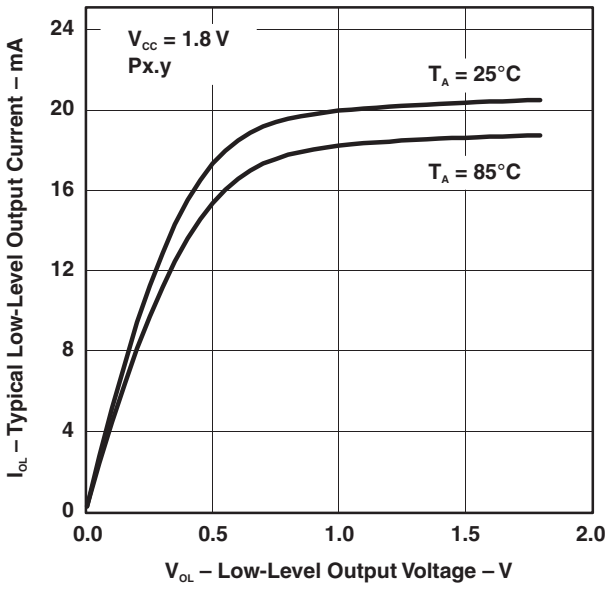


Figure 7.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

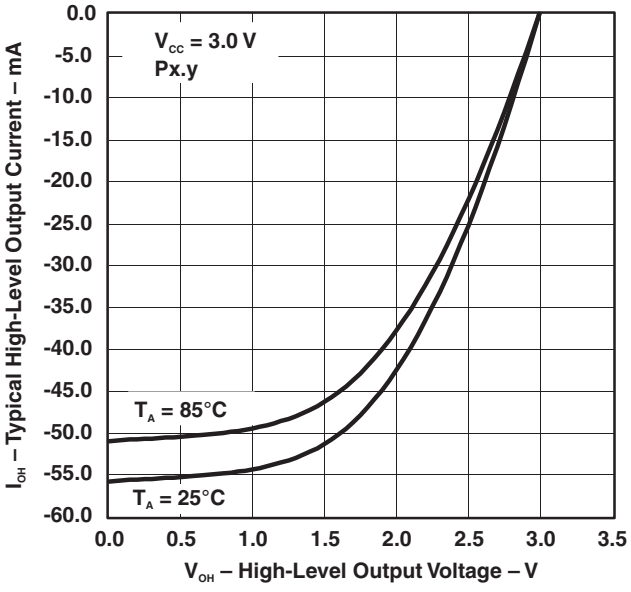


Figure 8.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

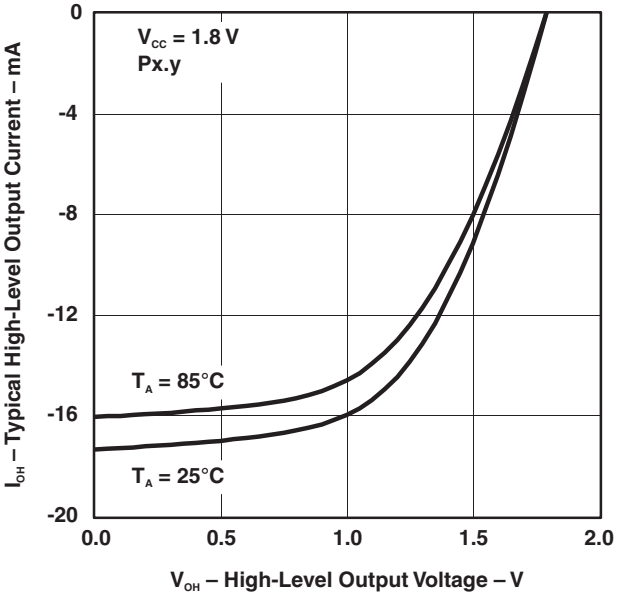


Figure 9.

Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2) (3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
Duty cycle	LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0(8)		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  (a) Keep the trace between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  (a) For XT1DRIVEx = 0, $C_{L,ef\,f} \le 6$ pF.
  (b) For XT1DRIVEx = 1, 6 pF $\le C_{L,ef\,f} \le 9$ pF.
  (c) For XT1DRIVEx = 2, 6 pF $\le C_{L,ef\,f} \le 10$ pF.
  (d) For XT1DRIVEx = 3, $C_{L,ef\,f} \ge 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Crystal Oscillator, XT1, High-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.HF}$	XT1 oscillator crystal current HF mode	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C	3.0 V		200		µA
		f_{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			450		
$f_{XT1,HF0}$	XT1 oscillator crystal frequency, HF mode 0	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0[2]		4		8	MHz
$f_{XT1,HF1}$	XT1 oscillator crystal frequency, HF mode 1	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1[2]		8		16	MHz
$f_{XT1,HF2}$	XT1 oscillator crystal frequency, HF mode 2	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2[2]		16		24	MHz
$f_{XT1,HF3}$	XT1 oscillator crystal frequency, HF mode 3	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3[2]		24		32	MHz
$f_{XT1,HF,SW}$	XT1 oscillator logic-level square-wave input frequency, HF mode, bypass mode	XTS = 1, XT1BYPASS = 1[3] [2]		1.5		32	MHz
OA_{HF}	Oscillation allowance for HF crystals[4]	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,HF}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,HF}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, $f_{XT1,HF}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, $f_{XT1,HF}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time, HF mode	f_{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
(a) Keep the traces between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(3) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

Crystal Oscillator, XT1, High-Frequency Mode[1] (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{L,eff}$	Integrated effective load capacitance, HF mode[5] [6]	XTS = 1			1		pF
Duty cycle	HF mode	XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 20 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency, HF mode[7]	XTS = 1[8]		30		300	kHz

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3.0 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0[3]		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0[3]		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0[3]		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0[3]		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1[4] [3]		1.5		32	MHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
(a) Keep the traces between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

Crystal Oscillator, XT2 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time	f_{OSC} = 6 MHz XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
Duty cycle		Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
		T_A = 25°C	3 V			±1.5	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
Duty cycle		Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
Duty cycle		Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz,		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

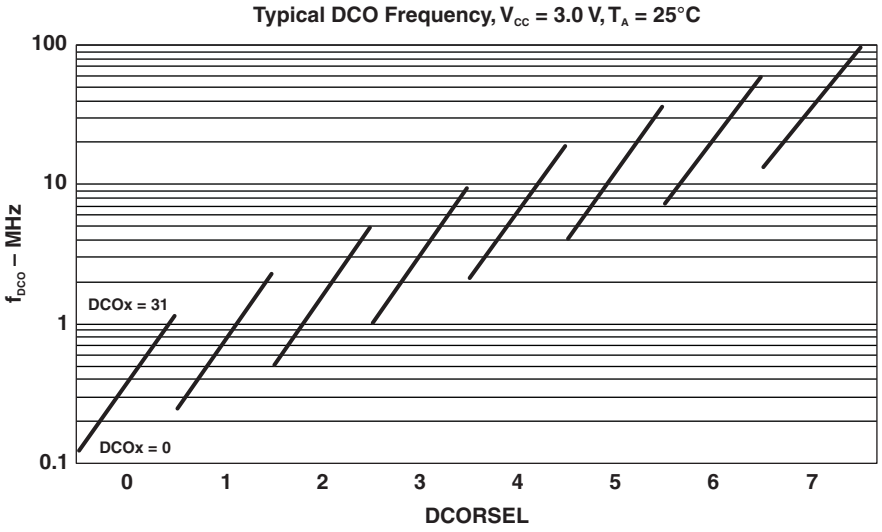


Figure 10. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}\_BOR\_IT-)$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s			1.55	V
$V(DV_{CC}\_BOR\_IT+)$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.80	1.30	1.65	V
$V(DV_{CC}\_BOR\_hys)$	BOR_H hysteresis		100		250	mV
$V(V_{CORE}\_BOR\_IT-)$	BOR_L on voltage, V_{CORE} falling level	DV_{CC} = 1.8 V to 3.6 V	0.69		0.83	V
$V(V_{CORE}\_BOR\_IT+)$	BOR_L off voltage, V_{CORE} rising level	DV_{CC} = 1.8 V to 3.6 V	0.83		1.05	V
$V(V_{CORE}\_BOR\_hys)$	BOR_L hysteresis		70		200	mV
t_{RESET}	Pulse length required at $\overline{RST}$/NMI pin to accept a reset		2			µs

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA	1.60	1.81	1.89	V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA	1.68	1.89	1.98	V
PSRR(DC,AM)	Power-supply rejection ratio, active mode	DV_{CC} = 2.2 V/3.6 V, I(V_{CORE}) = 0 mA, PMMCOREV = 2		60		dB
		DV_{CC} = 2.2 V/3.6 V, I(V_{CORE}) = 21 mA, PMMCOREV = 2		60		
PSRR(DC,LPM)	Power-supply rejection ratio, low-current mode	DV_{CC} = 2.2 V/3.6 V, I(V_{CORE}) = 0 mA, PMMCOREV = 2		50		dB
		DV_{CC} = 2.4 V/3.6 V, I(V_{CORE}) = 30 µA, PMMCOREV = 2		50		

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		2.0		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level	SVSHE = 1, SVSHRVL = 0	1.59	1.64	1.69	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.84	1.91	
		SVSHE = 1, SVSHRVL = 2	1.98	2.04	2.11	
		SVSHE = 1, SVSHRVL = 3	2.10	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.81	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.26	2.33	
		SVSHE = 1, SVSMHRRL = 4		2.40		
		SVSHE = 1, SVSMHRRL = 5		2.70		
		SVSHE = 1, SVSMHRRL = 6		3.00		
		SVSHE = 1, SVSMHRRL = 7		3.00		
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on/off delay time	SVSHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		2.0		µA
$V_{(SVMH)}$	SVM_H on/off voltage level	SVMHE = 1, SVSMHRRL = 0	1.65	1.74	1.86	V
		SVMHE = 1, SVSMHRRL = 1	1.85	1.94	2.02	
		SVMHE = 1, SVSMHRRL = 2	2.02	2.14	2.22	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.26	2.35	
		SVMHE = 1, SVSMHRRL = 4		2.40		
		SVMHE = 1, SVSMHRRL = 5		2.70		
		SVMHE = 1, SVSMHRRL = 6		3.00		
		SVMHE = 1, SVSMHRRL = 7		3.00		
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on/off delay time	SVMHE = 0 → 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		100		

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		µA
$V_{(SVSL\_IT-)}$	SVS_L on voltage level	SVSLE = 1, SVSLRVL = 0	1.20	1.27	1.32	V
		SVSLE = 1, SVSLRVL = 1	1.39	1.47	1.52	
		SVSLE = 1, SVSLRVL = 2	1.60	1.67	1.72	
		SVSLE = 1, SVSLRVL = 3	1.70	1.77	1.82	
$V_{(SVSL\_IT+)}$	SVS_L off voltage level	SVSLE = 1, SVSMLRRL = 0	1.29	1.34	1.39	V
		SVSLE = 1, SVSMLRRL = 1	1.49	1.54	1.59	
		SVSLE = 1, SVSMLRRL = 2	1.69	1.74	1.79	
		SVSLE = 1, SVSMLRRL = 3, 4, 5, 6, 7	1.79	1.84	1.89	
$V_{(SVSL\_HYS)}$	SVS_L hysteresis	SVSLE = 1, SVSMLRRL = 0		70		mV
		SVSLE = 1, SVSMLRRL = 1		70		
		SVSLE = 1, SVSMLRRL = 2		70		
		SVSLE = 1, SVSMLRRL = 3		70		
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on/off delay time	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		2.0		µA
$V_{(SVML)}$	SVM_L on/off voltage level	SVMLE = 1, SVSMLRRL = 0	1.28	1.34	1.40	V
		SVMLE = 1, SVSMLRRL = 1	1.49	1.54	1.60	
		SVMLE = 1, SVSMLRRL = 2	1.68	1.74	1.79	
		SVMLE = 1, SVSMLRRL = 3, 4, 5, 6, 7	1.76	1.84	1.90	
		SVMLE = 1, SVSMLOVPE = 1		2.02		
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on/off delay time	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

Wake-up from Low Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = 2 SVSLFP = 1	2.2/3.0 V			5	µs
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode(2)	PMMCOREV = SVSMLRRL = 2 SVSLFP = 0	2.2/3.0 V		150		µs

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. Please refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208).

(2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. Please refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208).

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	1.8 V/ 3.0 V			25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs. Minimum pulse width required for capture.	1.8 V/ 3.0 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ± 10%	1.8 V/ 3.0 V			25	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs. Minimum pulse width required for capture.	1.8 V/ 3.0 V	20			ns

USCI (UART Mode) - recommended operating conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_τ	UART receive deglitch time(1)		2.2 V	50		600	ns
			3 V	50		600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode) - recommended operating conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Note (1), Figure 11 and Figure 12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	65			ns
			3 V	50			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			25	ns
			3 V			20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.2 V				ns
			3 V				

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 11 and Figure 12.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in Figure 11 and Figure 12.

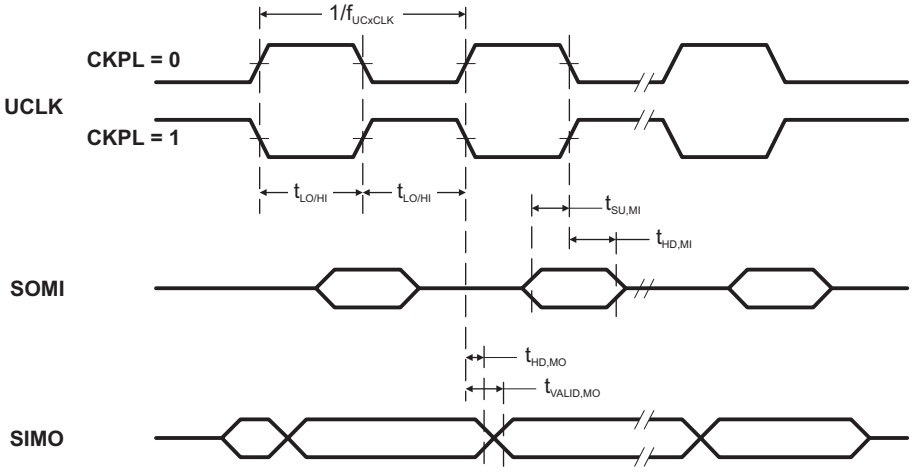


Figure 11. SPI Master Mode, CKPH = 0

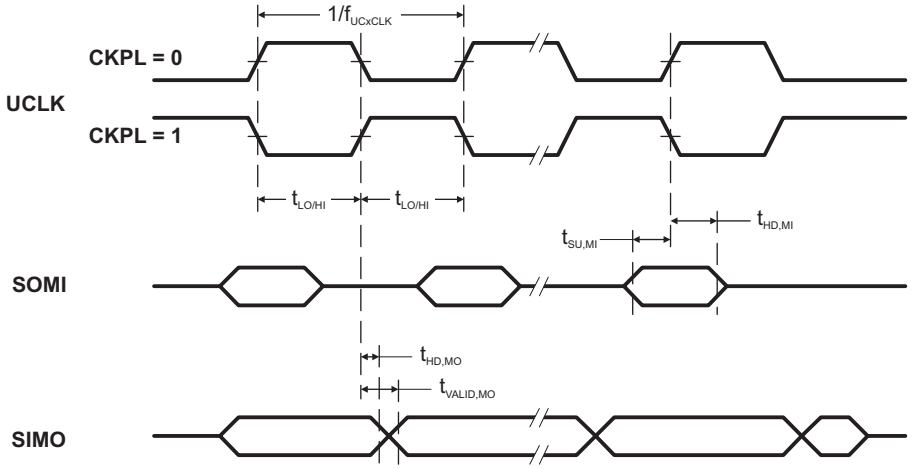


Figure 12. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Note (1), Figure 13 and Figure 14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V/3 V		40		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V/3 V		40		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V/3 V		40		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V			62	ns
			3 V			50	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	2.2 V	0			ns
			3 V	0			

(1) $f_{UCxCLK} = 1/2 \times t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 11 and Figure 12.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 11 and Figure 12.

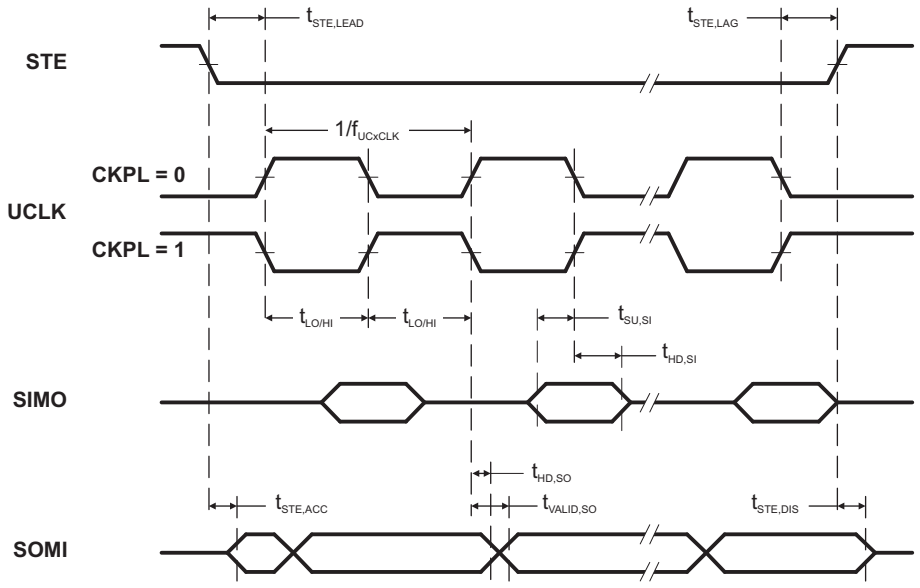


Figure 13. SPI Slave Mode, CKPH = 0

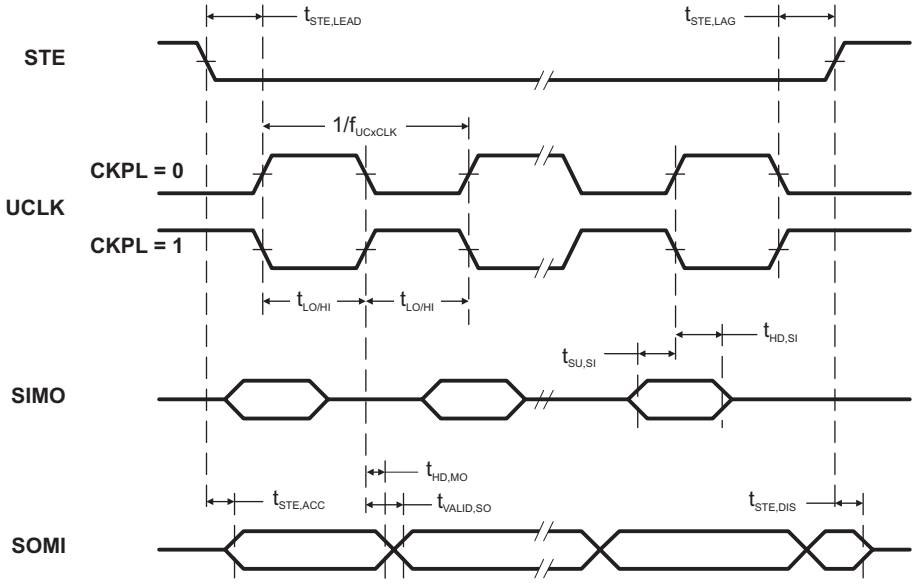


Figure 14. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50		600	ns
			3 V	50		600	

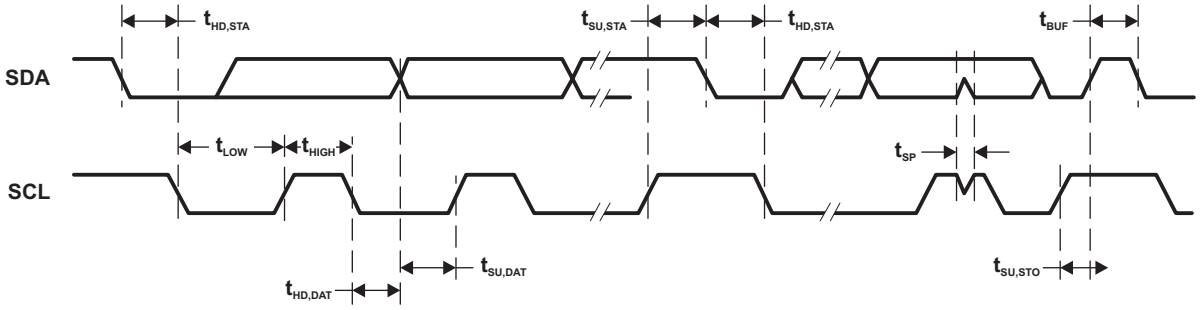


Figure 15. I2C Mode Timing

12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 pins: P6.0 to P6.7, P7.4 to P7.7, P5.0, and P5.1 terminals		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		125	155	µA
			3 V		150	220	
I_{REF+}	Operating supply current into AV_{CC} terminal(4)	ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		150	190	µA
		ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V/3 V		150	180	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON resistance	$0 V \le V_{Ax} \le AV_{CC}$		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See 12-Bit ADC, External Reference and 12-Bit ADC, Built-In Reference.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion. No external load.

12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4		AV_{CC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4		AV_{CC}	V
I_{VeREF+}	Static input current	$0 V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0 V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$C_{VREF+/-}$	Capacitance at $V_{REF+/-}$ terminal			(5)10			µF

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10µF and 100nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx Family User's Guide* (SLAU208).

12-Bit ADC, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+}(max) \le I_{VREF+} \le I_{VREF+}(min)$	3 V	2.35	2.45	2.53	V
		REF2_5V = 0 for 1.5 V, $I_{VREF+}(max) \le I_{VREF+} \le I_{VREF+}(min)$	2.2 V/3 V	1.41	1.47	1.53	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0		2.2			V
		REF2_5V = 1		2.8			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V			–1	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal	I_{VREF+} = +10 µA/–1000 µA, Analog input voltage ~0.75 V, REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = +10 µA/–1000 µA, Analog input voltage ~1.25 V, REF2_5V = 1	3 V			±2	
C_{VREF+}	Capacitance at V_{REF+} terminal	REFON = REFOUT = 1 (1)	2.2 V/3 V	20		100	pF
T_{REF+}	Temperature coefficient of built-in reference (2)	REF2_5V = 0, I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ –1 mA	2.2 V/3 V		30		ppm/°C
		REF2_5V = 1, I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ –1 mA	3 V		30		
t_{SETTLE}	Settling time of reference voltage (3)	V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V, REFOUT = 0, REFON = 0 → 1			20		µs
		V_{REF+} = 2.5 V, V_{AVCC} = 2.8 V, REFOUT = 0, REFON = 0 → 1			20		
		V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V, C_{VREF} = C_{VREF}(max) REFOUT = 1, REFON = 0 → 1			35		
		V_{REF+} = 2.5 V, V_{AVCC} = 2.8 V, C_{VREF} = C_{VREF}(max) REFOUT = 1, REFON = 0 → 1			35		

(1) Two decoupling capacitors, 10µF and 100nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx Family User's Guide* (SLAU208).
(2) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C – (–40°C))
(3) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V/3 V	0.45	4.8	5.4	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator (1)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V/3 V	4.2	4.65	5.0	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12OSC}$ = 4.2 MHz to 5.4 MHz	2.2 V/3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			(2)		
$t_{ADC12ON}$	Turn on settling time of the ADC	See (3)				100	ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (4)	2.2 V/3 V	1000			ns

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(2) 13 × ADC12DIV × $1/f_{ADC12CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4\ V \le (V_{eREF+} - V_{REF-}/V_{eREF-})min \le 1.6\ V$	2.2 V/3 V			±2	LSB
		$1.6\ V < (V_{eREF+} - V_{REF-}/V_{eREF-})min \le V_{AVCC}$				±1.7	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 20 pF	2.2 V/3 V			±1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source R_S < 100 Ω, C_{VREF+} = 20 pF	2.2 V/3 V		±1	±3.5	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 20 pF	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-})min \le (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 20 pF	2.2 V/3 V		±2	±5	LSB

12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (1)	REFON = 0, INCH = 0Ah, ADC12ON = N A, T_A = 25°C	2.2 V		150		µA
			3 V		150		
V_{SENSOR}	See (2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		894		mV
			3 V		894		
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.66		mV/°C
			3 V		3.66		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2.2 V		1.1		V
			3 V		1.5		
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V/3 V	1000			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1) or (ADC12ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

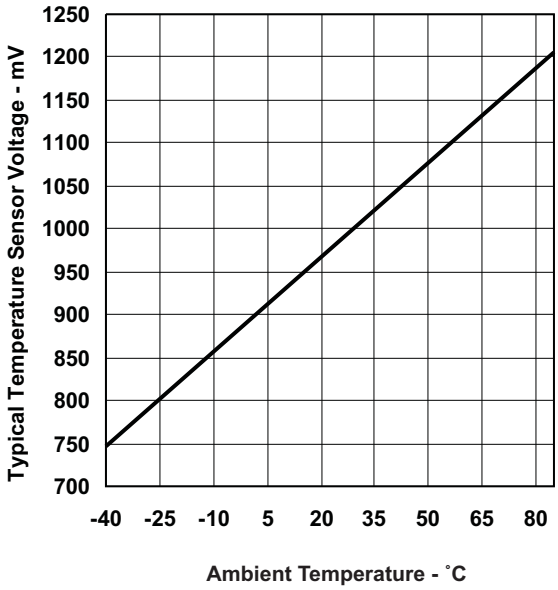


Figure 16. Typical Temperature Sensor Voltage

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DV_{CC} during program			3	5	mA
I_{ERASE}	Average supply current from DV_{CC} during erase				2	mA
I_{MERASE}, I_{BANK}	Average supply current from DV_{CC} during mass erase or bank erase				2	mA
t_{CPT}	Cumulative program time	See (1)			16	ms
	Program/erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
t_{Word}	Word or byte program time	See (2)	64		85	µs
$t_{Block, 0}$	Block program time for first byte or word	See (2)	49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word	See (2)	37		49	µs
$t_{Block, N}$	Block program time for last byte or word	See (2)	55		73	µs
t_{Erase}	Erase time for segment, mass erase, and bank erase when available.	See (2)	23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V/3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length	2.2 V/3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V/3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency - 4-wire JTAG (2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V/3 V	45	60	80	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

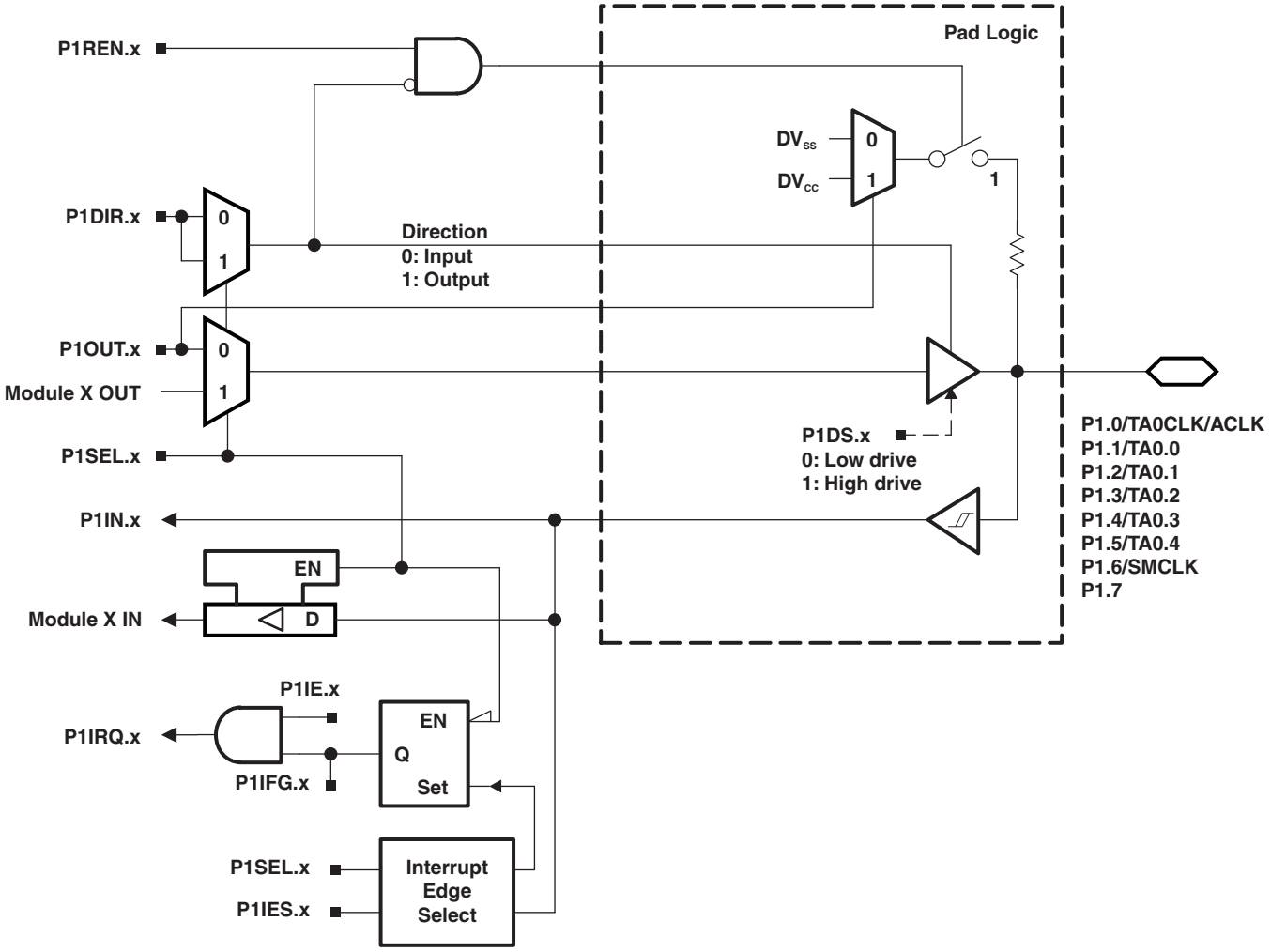


Table 42. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0.TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/SMCLK	6	P1.6 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.7	7	P1.7 (I/O)	I: 0; O: 1	0

Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

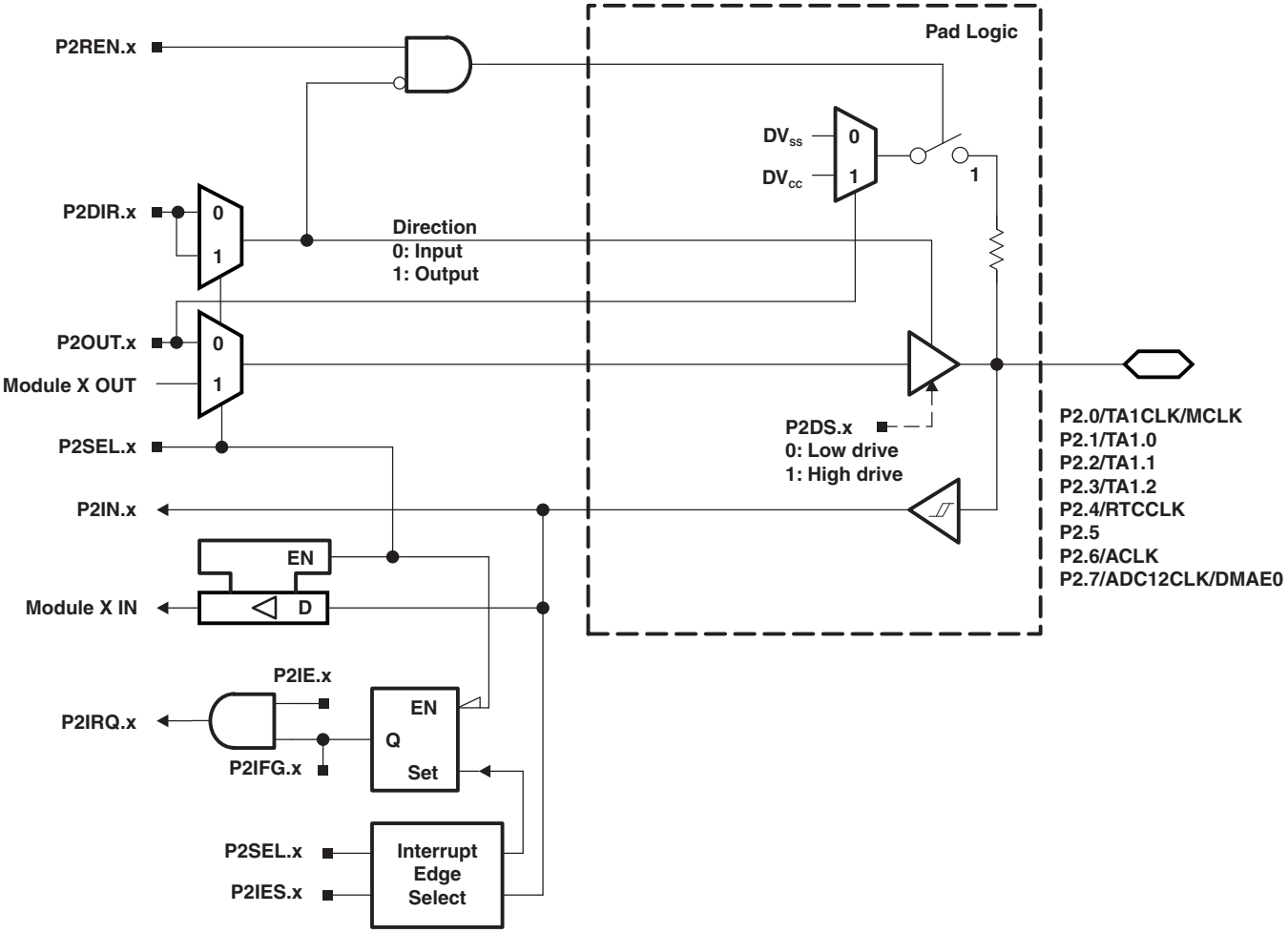


Table 43. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA1CLK/MCLK	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		MCLK	1	1
P2.1/TA1.0	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1
P2.2/TA1.1	2	P2.2 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.3/TA1.2	3	P2.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.4/RTCCLK	4	P2.4 (I/O)	I: 0; O: 1	0
		RTCCLK	1	1
P2.5	5	P2.5 (I/O	I: 0; O: 1	0
P2.6/ACLK	6	P2.6 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		ADC12CLK	1	1

Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

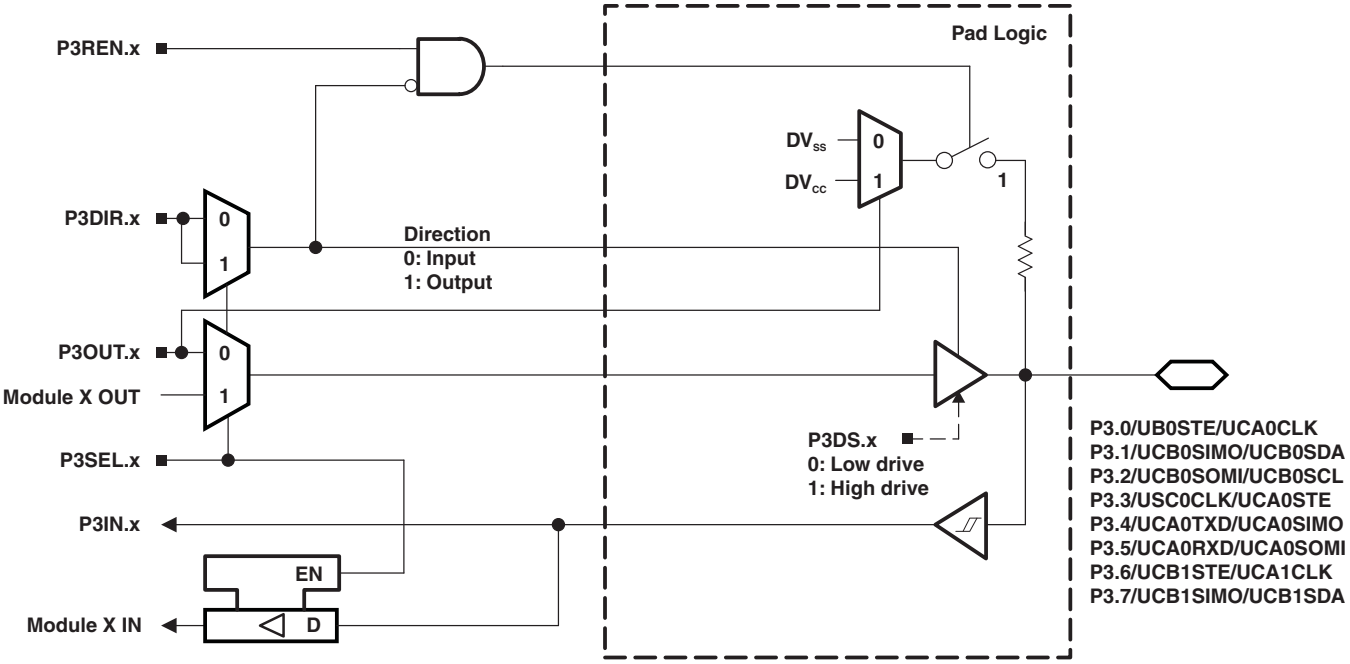


Table 44. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK (2) (3)	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (2) (4)	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (2) (4)	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE (2)	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (2)	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (2)	X	1
P3.6/UCB1STE/UCA1CLK	6	P3.6 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK (2) (5)	X	1
P3.7/UCB1SIMO/UCB1SDA	7	P3.7 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA (2) (4)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output, USCI A1/B1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

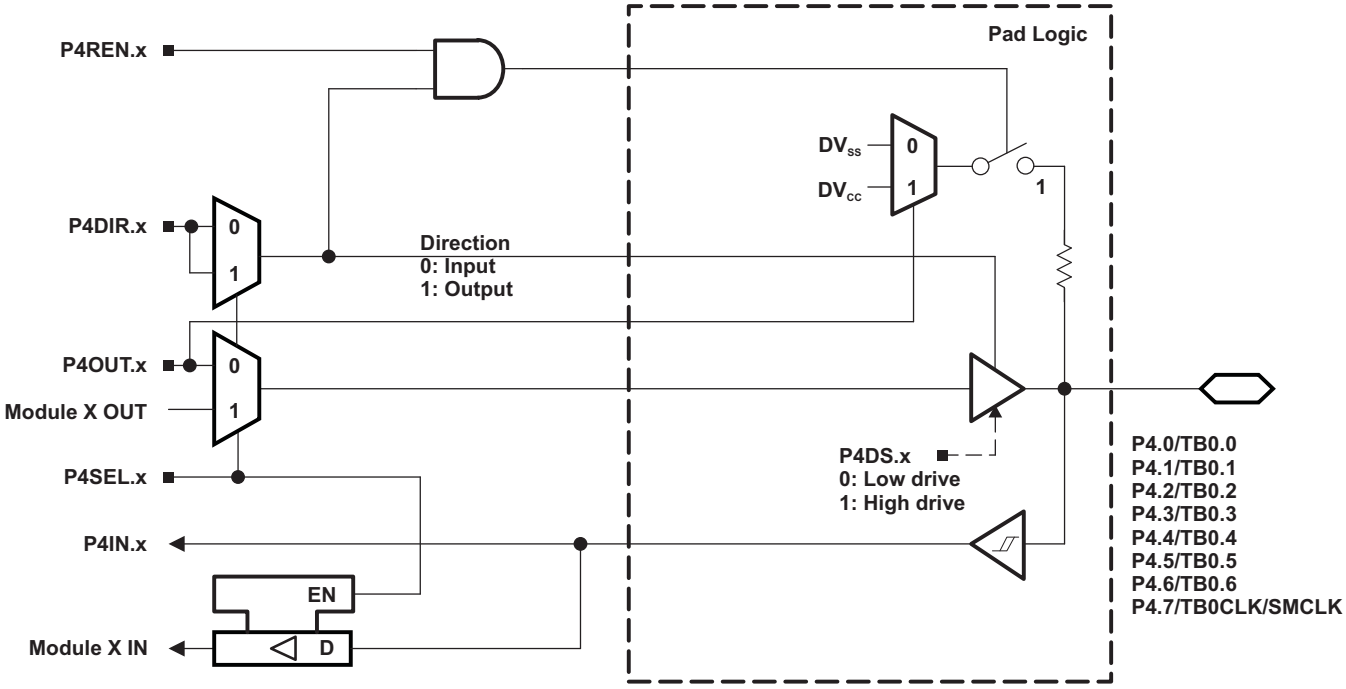


Table 45. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0.0	0	4.0 (I/O)	I: 0; O: 1	0
		TB0.CCI0A and TB0.CCI0B	0	1
		TB0.0 (1)	1	1
P4.1/TB0.1	1	4.1 (I/O)	I: 0; O: 1	0
		TB0.CCI1A and TB0.CCI1B	0	1
		TB0.1 (1)	1	1
P4.2/TB0.2	2	4.2 (I/O)	I: 0; O: 1	0
		TB0.CCI2A and TB0.CCI2B	0	1
		TB0.2 (1)	1	1
P4.3/TB0.3	3	4.3 (I/O)	I: 0; O: 1	0
		TB0.CCI3A and TB0.CCI3B	0	1
		TB0.3 (1)	1	1
P4.4/TB0.5	4	4.4 (I/O)	I: 0; O: 1	0
		TB0.CCI4A and TB0.CCI4B	0	1
		TB0.4 (1)	1	1
P4.5/TB0.5	5	4.5 (I/O)	I: 0; O: 1	0
		TB0.CCI5A and TB0.CCI5B	0	1
		TB0.5 (1)	1	1
P4.6/TB0.6	6	4.6 (I/O)	I: 0; O: 1	0
		TB0.CCI6A and TB0.CCI6B	0	1
		TB0.6 (1)	1	1
P4.7/TB0CLK/SMCLK	7	4.7 (I/O)	I: 0; O: 1	0
		TB0CLK	0	1
		SMCLK	1	1

(1) Setting TBOUTH causes all Timer_B configured outputs to be set to high impedance.

Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

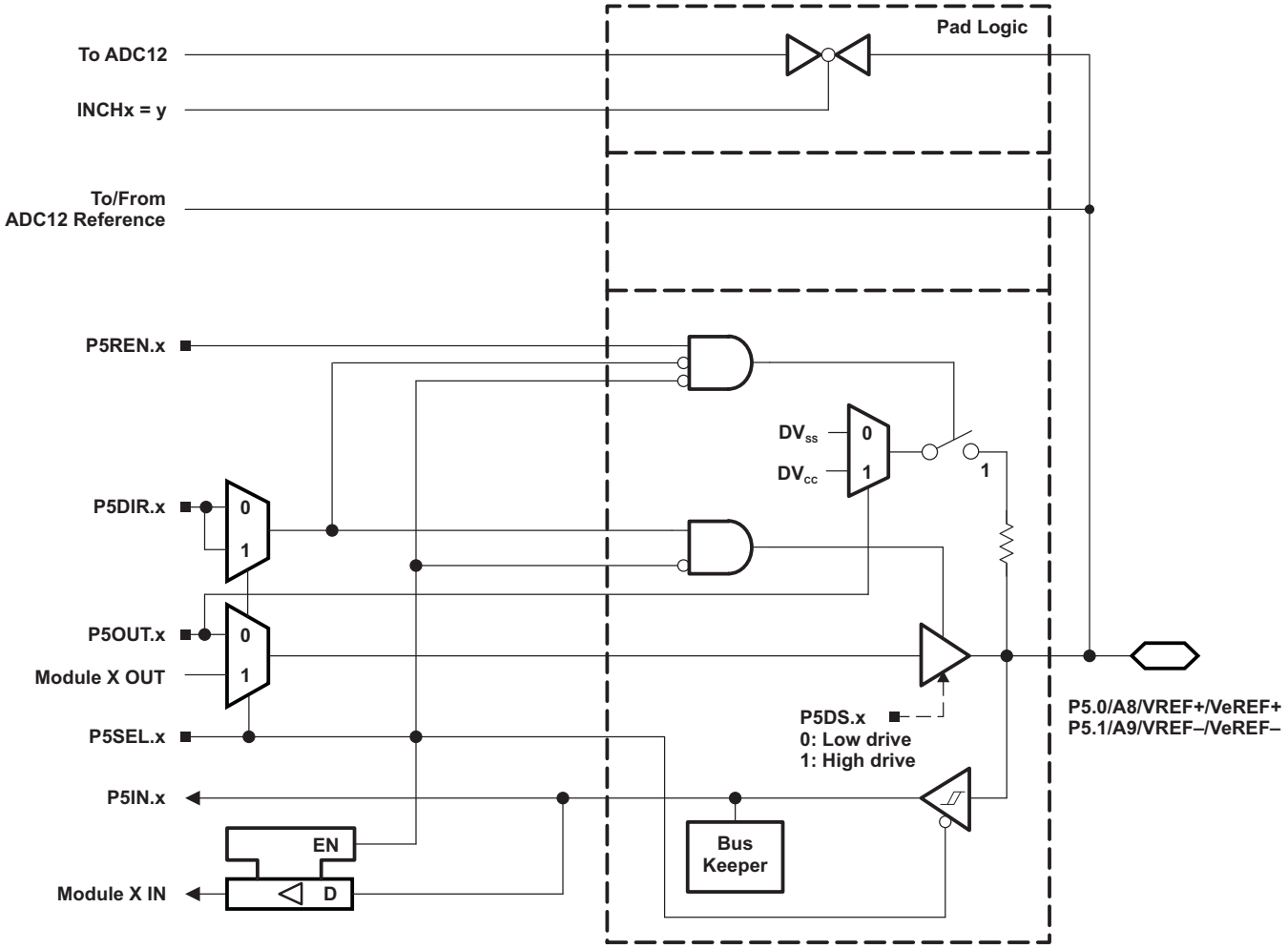
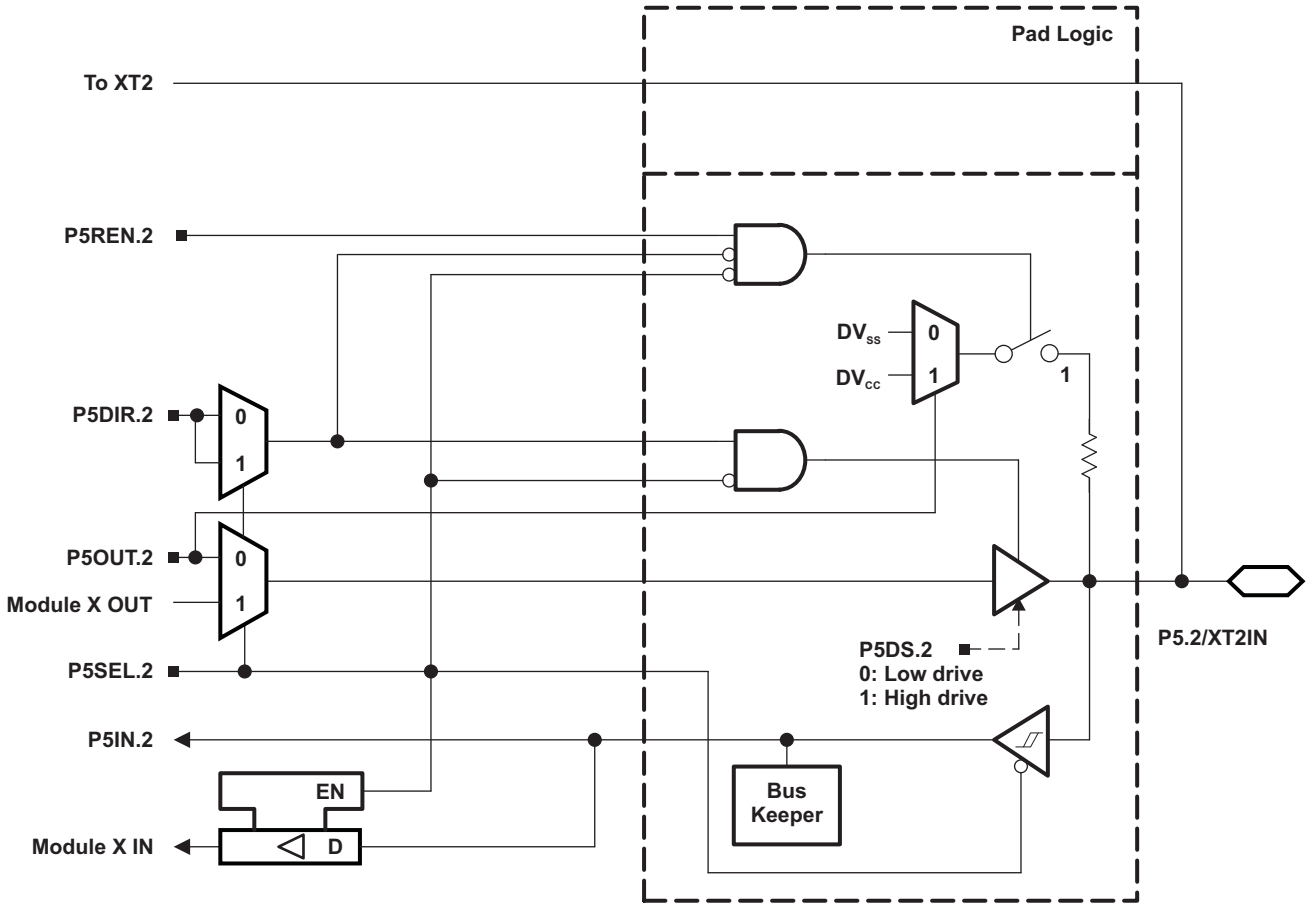


Table 46. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/A8/VREF+/VeREF+	0	P5.0 (I/O)(2)	I: 0; O: 1	0	X
		VeREF+(3)	X	1	0
		VREF+(4)	X	1	1
		A8(5)	X	1	0
P5.1/A9/VREF–/VeREF–	1	P5.1 (I/O)(2)	I: 0; O: 1	0	X
		VeREF–(6)	X	1	0
		VREF–(7)	X	1	1
		A9(8)	X	1	0

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A.
(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin.
(5) When not using an external reference applied to VeREF+ or not outputting the internal reference to VREF+, A8 may be used as an external ADC channel. Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(6) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A.
(7) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF– reference is available at the pin.
(8) When not using an external reference applied to VeREF+ or not outputting the internal reference to VREF+, A8 may be used as an external ADC channel. Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P5, P5.2, Input/Output With Schmitt Trigger



Port P5, P5.3, Input/Output With Schmitt Trigger

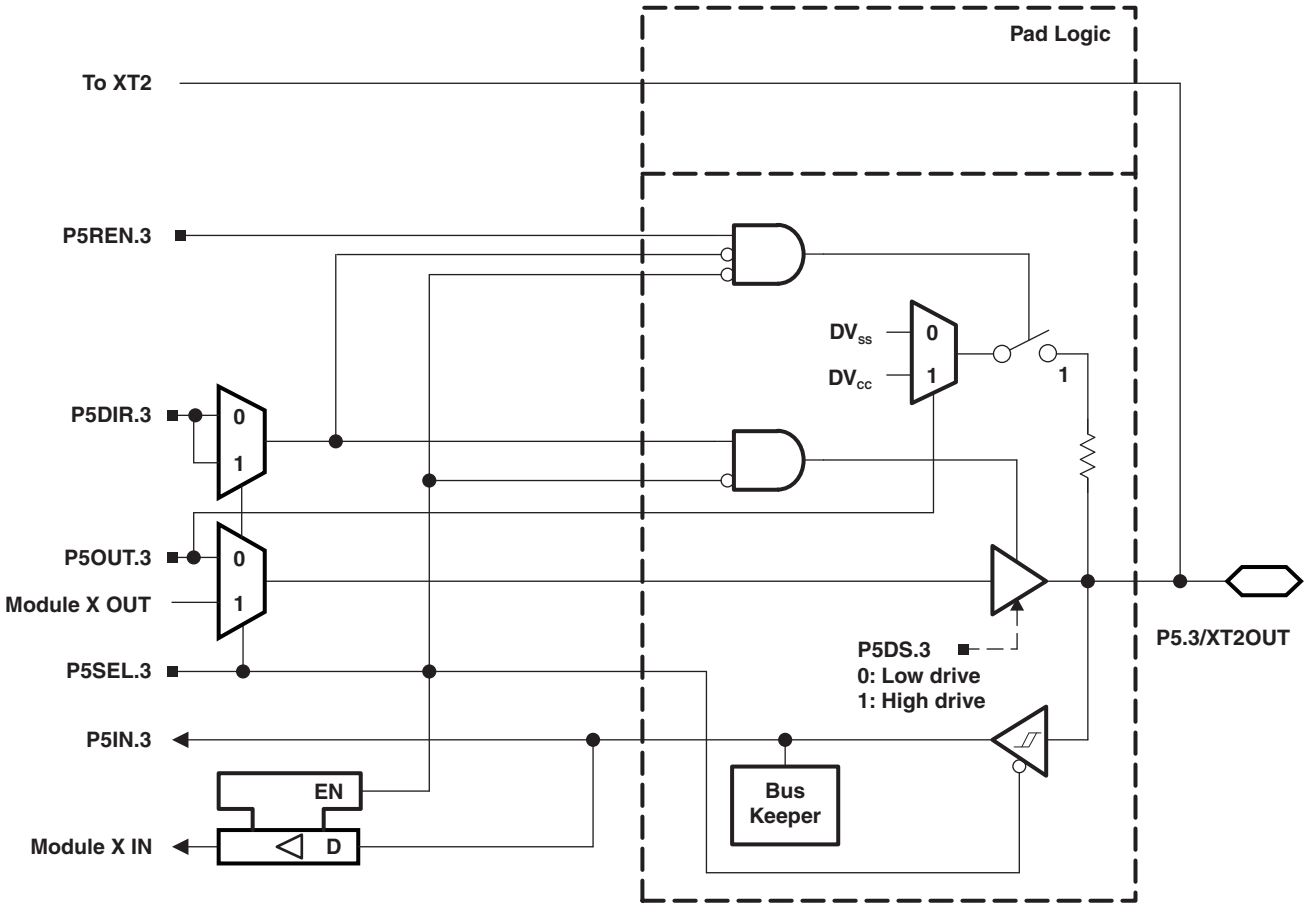


Table 47. Port P5 (P5.2) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode(3)	X	1	X	0
		P5.3 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

Port P5, P5.4 to P5.7, Input/Output With Schmitt Trigger

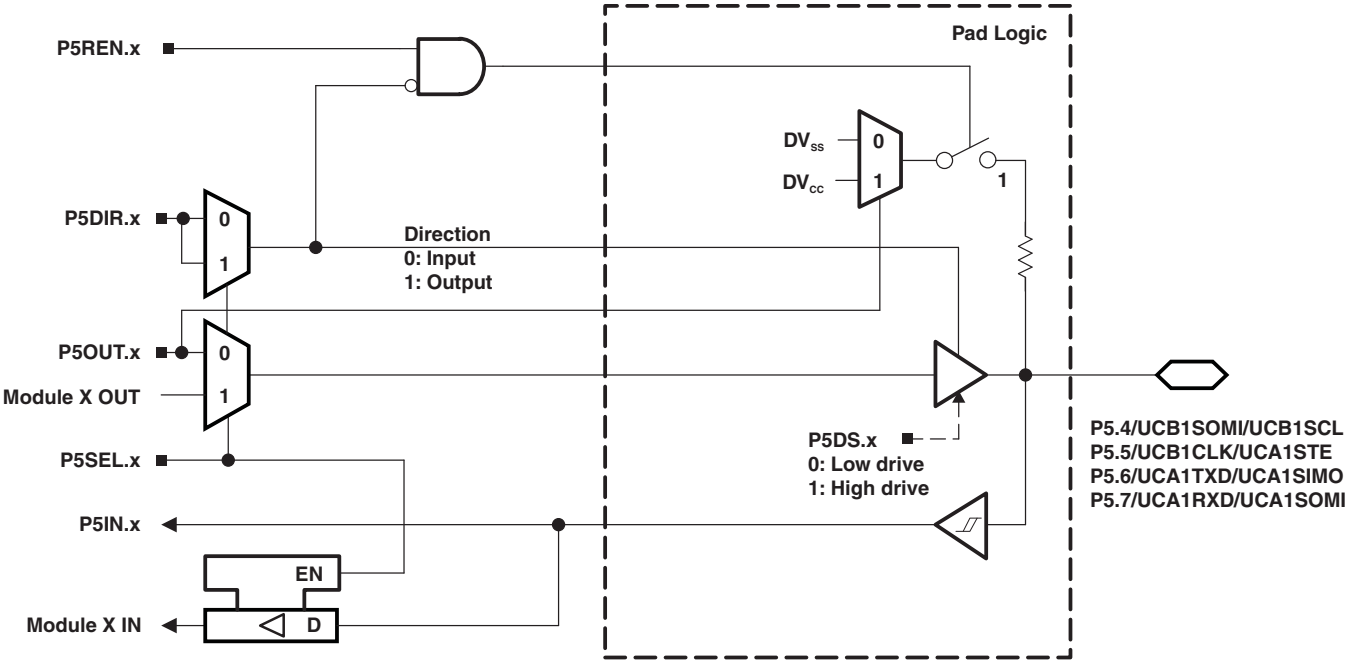


Table 48. Port P5 (P5.4 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P5DIR.x	P5SEL.x
P5.4/UCB1SOMI/UCB1SCL	4	P5.4 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL (2) (3)	X	1
P5.5/UCB1CLK/UCA1STE	5	P5.5 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE (2)	X	1
P5.6/UCA1TXD/UCA1SIMO	6	P5.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO (2)	X	1
P5.7/UCA1RXD/UCA1SOMI	7	P5.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI (2)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

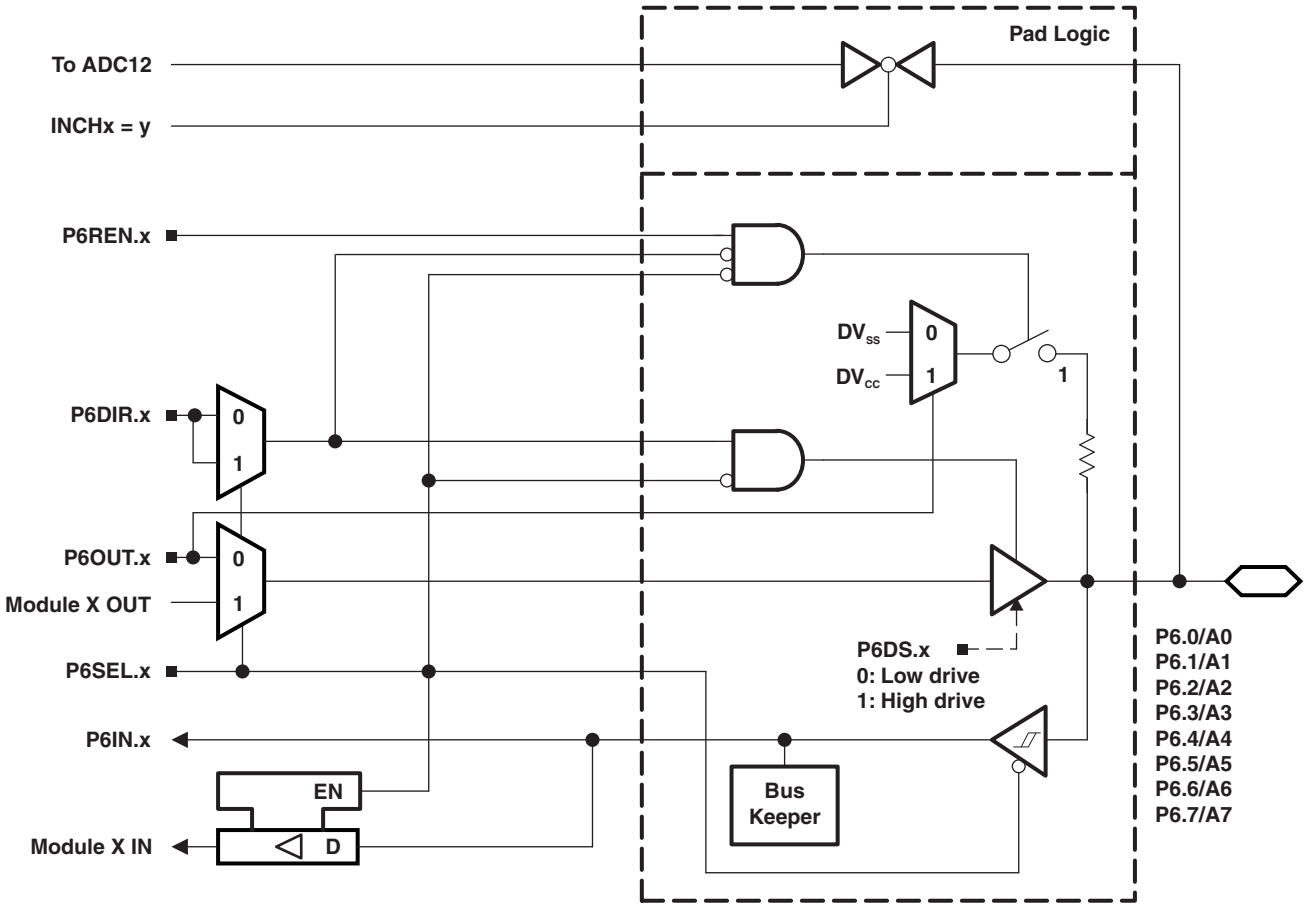
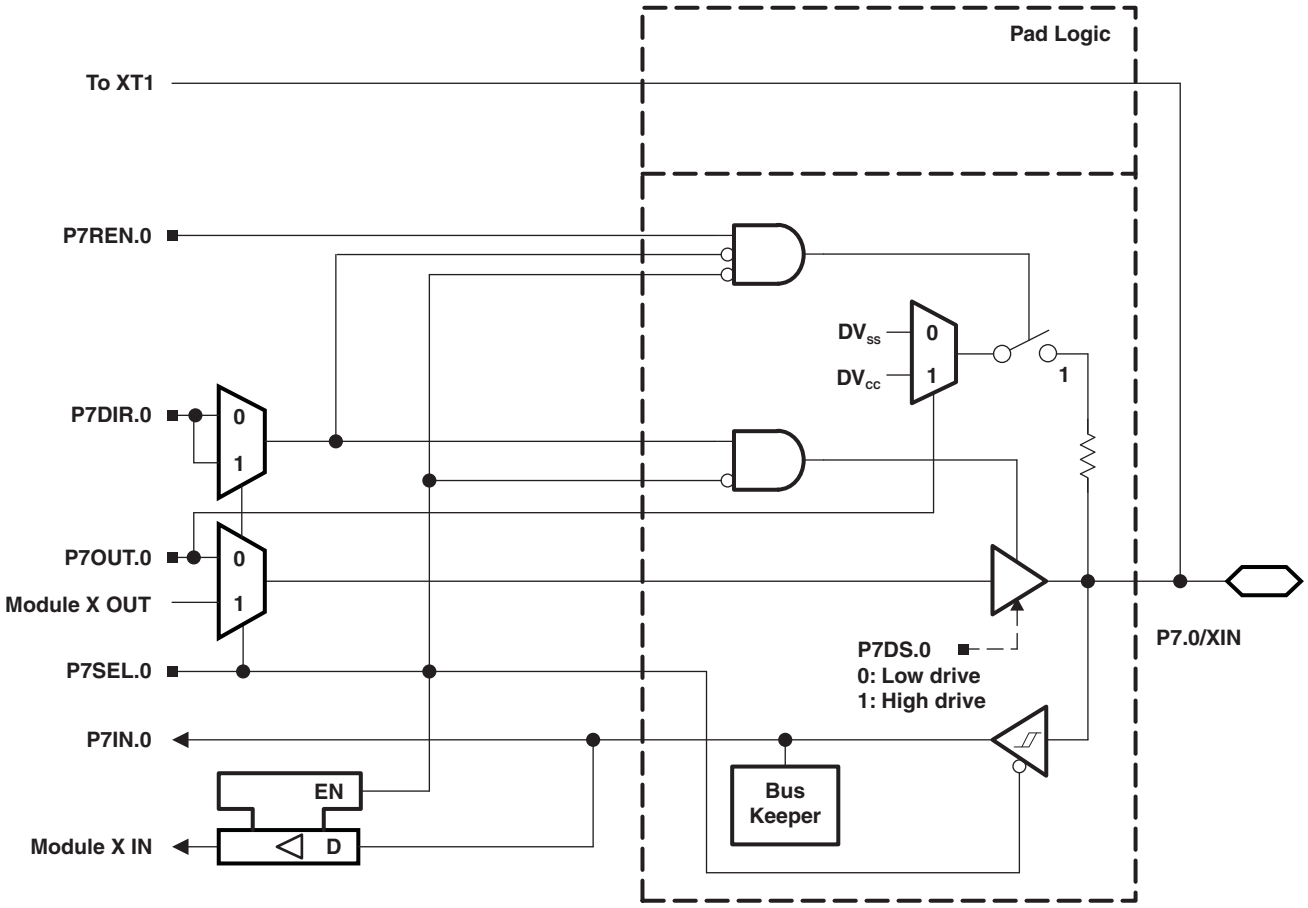


Table 49. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P6DIR.x	P6SEL.x	INCHx
P6.0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	X
		A0(2) (3)	X	X	0
P6.1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	X
		A1(2) (3)	X	X	1
P6.2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	X
		A2(2) (3)	X	X	2
P6.3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	X
		A3(2) (3)	X	X	3
P6.4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	X
		A4(2) (3)	X	X	4
P6.5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	X
		A5(1) (2) (3)	X	X	5
P6.6/A6	6	P6.6 (I/O)	I: 0; O: 1	0	X
		A6(2) (3)	X	X	6
P6.7/A7	7	P6.7 (I/O)	I: 0; O: 1	0	X
		A7(2) (3)	X	X	7

(1) X = Don't care
(2) Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

Port P7, P7.0, Input/Output With Schmitt Trigger



Port P7, P7.1, Input/Output With Schmitt Trigger

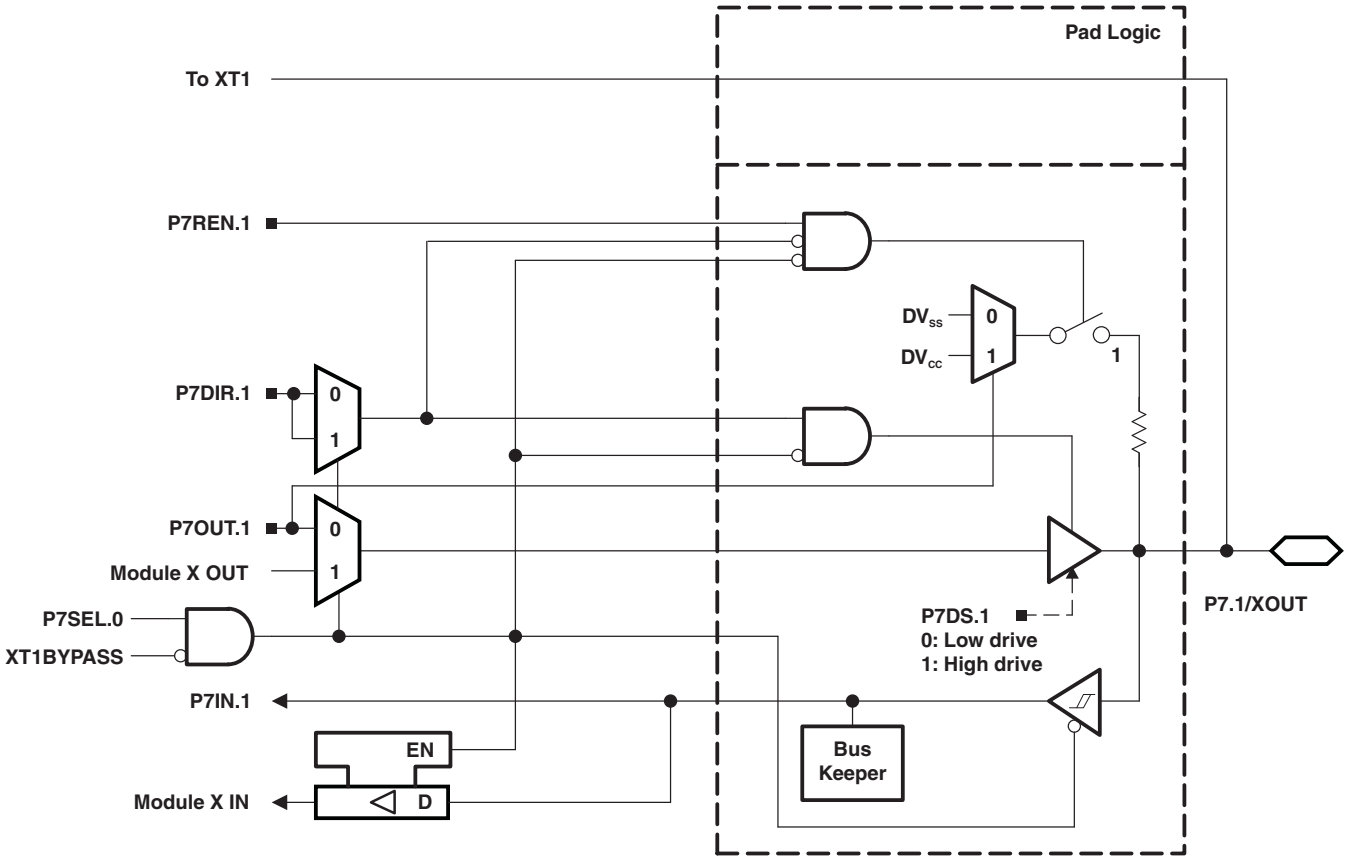


Table 50. Port P7 (P7.0 and P7.1) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P7DIR.x	P7SEL.0	P7SEL.1	XT1BYPASS
P7.0/XIN	0	P7.0 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode(2)	X	1	X	0
		XIN bypass mode(2)	X	1	X	1
P7.1/XOUT	1	P7.1 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode(3)	X	1	X	0
		P7.1 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P7SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P7.0 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.1 can be used as general-purpose I/O.

Port P7, P7.2 and P7.3, Input/Output With Schmitt Trigger

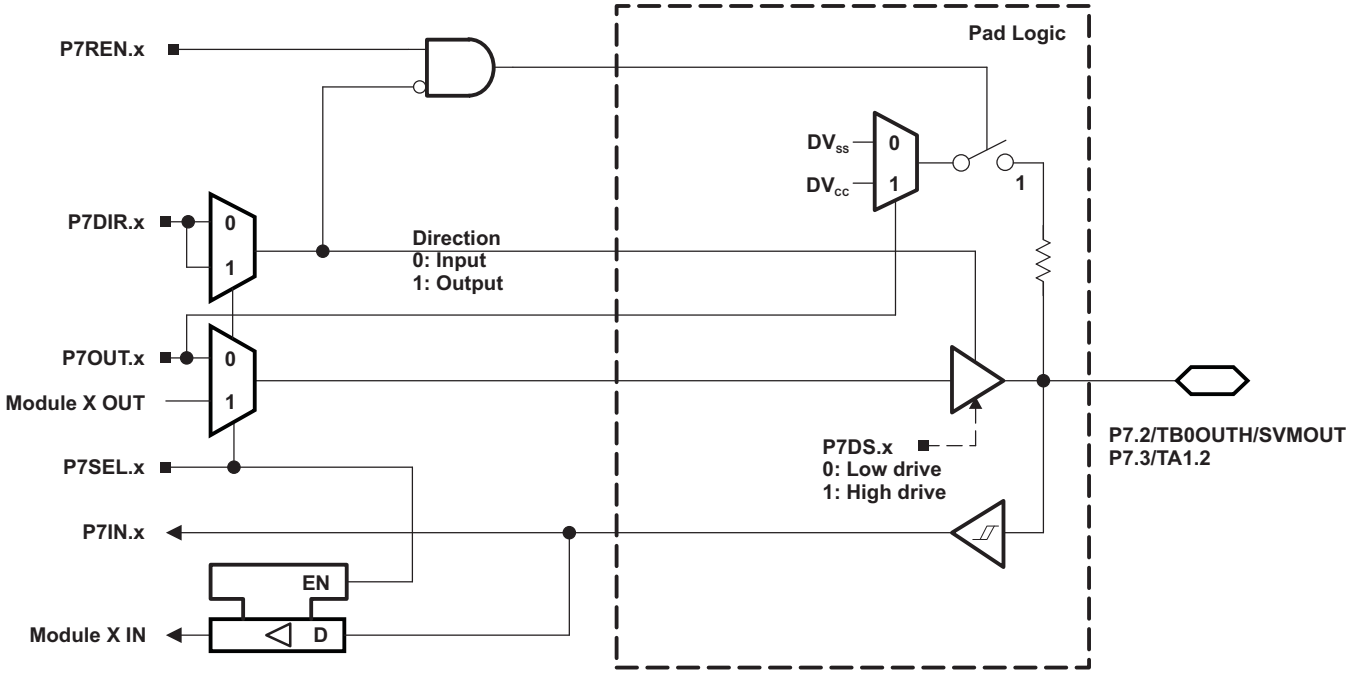


Table 51. Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P7DIR.x	P7SEL.x
P7.2/TB0OUTH/SVMOUT	2	P7.2 (I/O)	I: 0; O: 1	0
		TB0OUTH	0	1
		SVMOUT	1	1
P7.3/TA1.2	3	P7.3 (I/O)	I: 0; O: 1	0
		TA1.CCI2B	0	1
		TA1.2	1	1

Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger

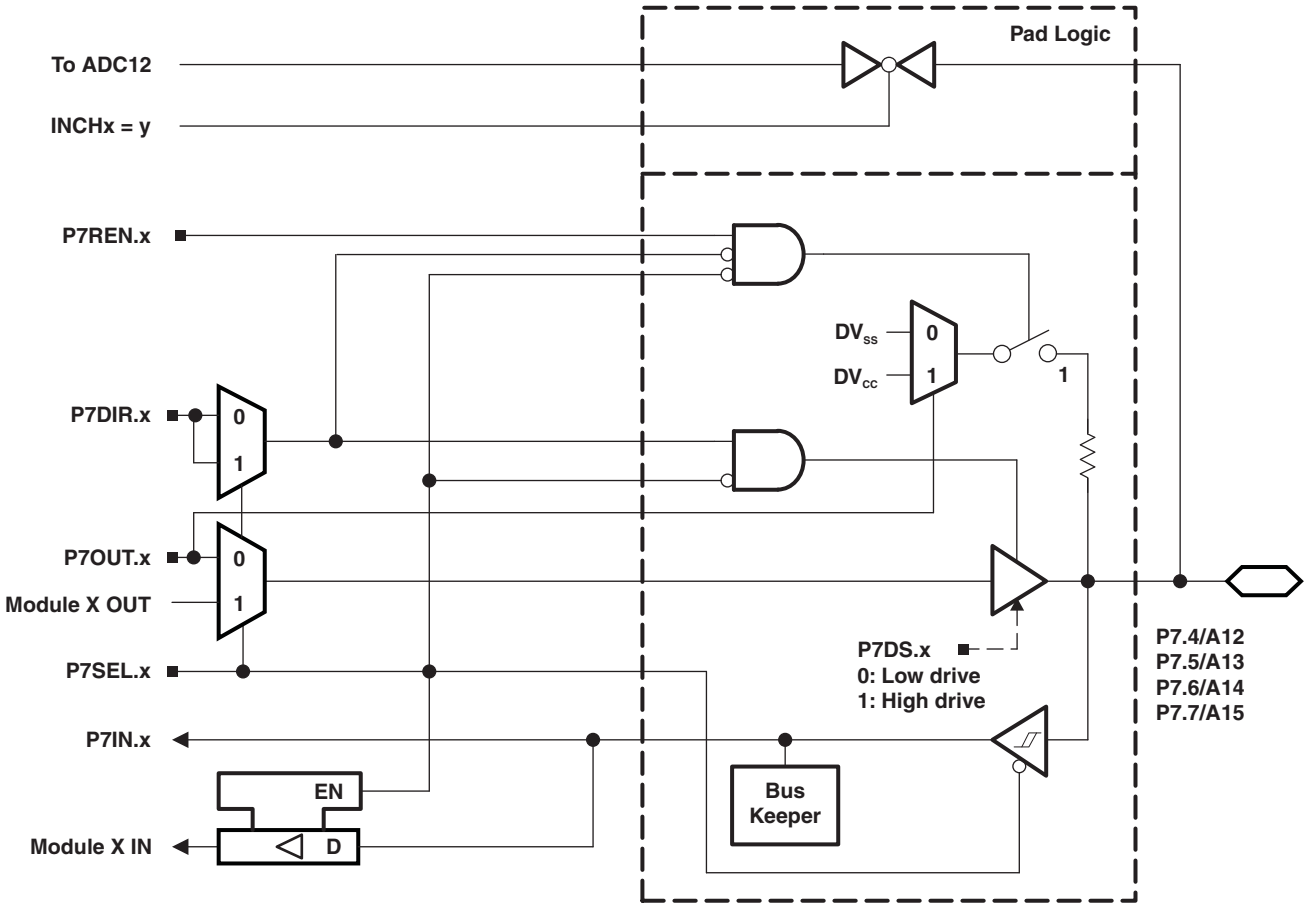


Table 52. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P7DIR.x	P7SEL.x	INCHx
P7.4/A12	4	P7.4 (I/O)	I: 0; O: 1	0	X
		A12 (2) (3)	X	X	12
P7.5/A13	5	P7.5 (I/O)	I: 0; O: 1	0	X
		A13 (4) (5)	X	X	13
P7.6/A14	6	P7.6 (I/O)	I: 0; O: 1	0	X
		A14 (4) (5)	X	X	14
P7.7/A15	7	P7.7 (I/O)	I: 0; O: 1	0	X
		A15 (4) (5)	X	X	15

(1) X = Don't care
(2) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.
(4) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

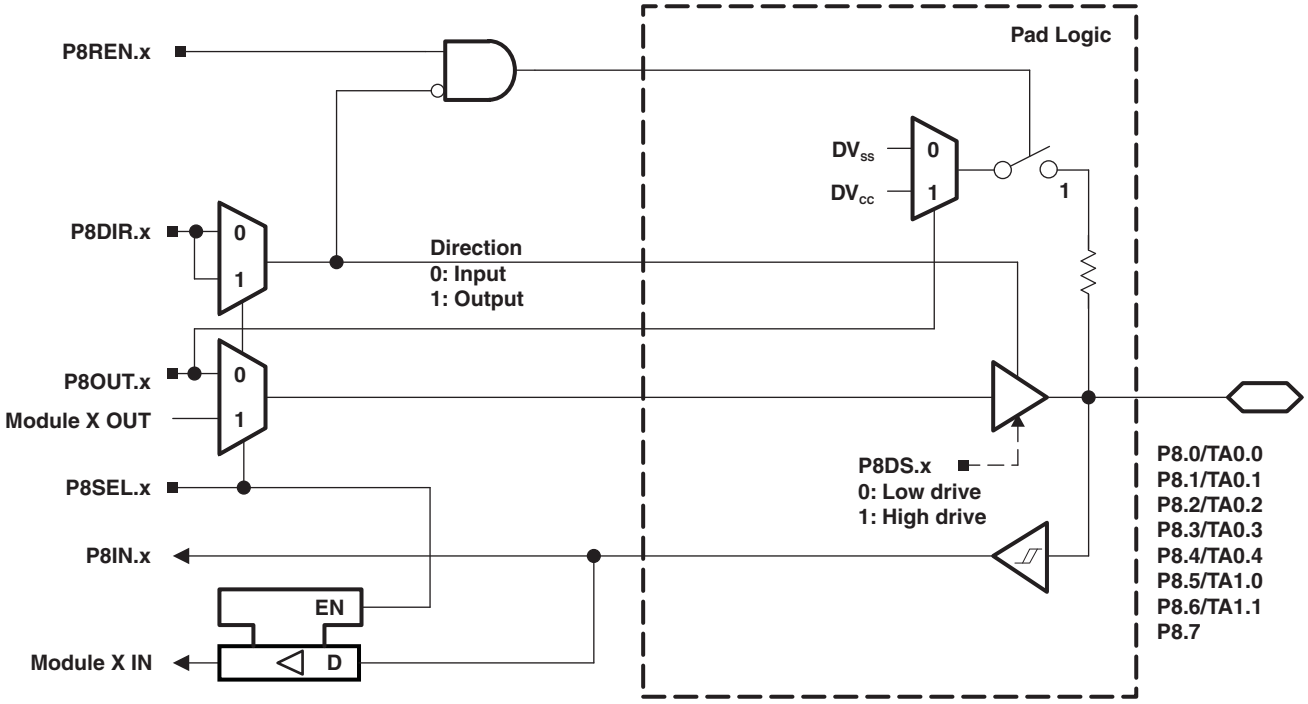


Table 53. Port P8 (P8.0 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.0/TA0.0	0	P8.0 (I/O)	I: 0; O: 1	0
		TA0.CCI0B	0	1
		TA0.0	1	1
P8.1/TA0.1	1	P8.1 (I/O)	I: 0; O: 1	0
		TA0.CCI1B	0	1
		TA0.1	1	1
P8.2/TA0.2	2	P8.2 (I/O)	I: 0; O: 1	0
		TA0.CCI2B	0	1
		TA0.2	1	1
P8.3/TA0.3	3	P8.3 (I/O)	I: 0; O: 1	0
		TA0.CCI3B	0	1
		TA0.3	1	1
P8.4/TA0.4	4	P8.4 (I/O)	I: 0; O: 1	0
		TA0.CCI4B	0	1
		TA0.4	1	1
P8.5/TA1.0	5	P8.5 (I/O)	I: 0; O: 1	0
		TA1.CCI0B	0	1
		TA1.0	1	1
P8.6/TA1.1	6	P8.6 (I/O)	I: 0; O: 1	0
		TA1.CCI1B	0	1
		TA1.1	1	1
P8.7	7	P8.7 (I/O)	I: 0; O: 1	0

Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger

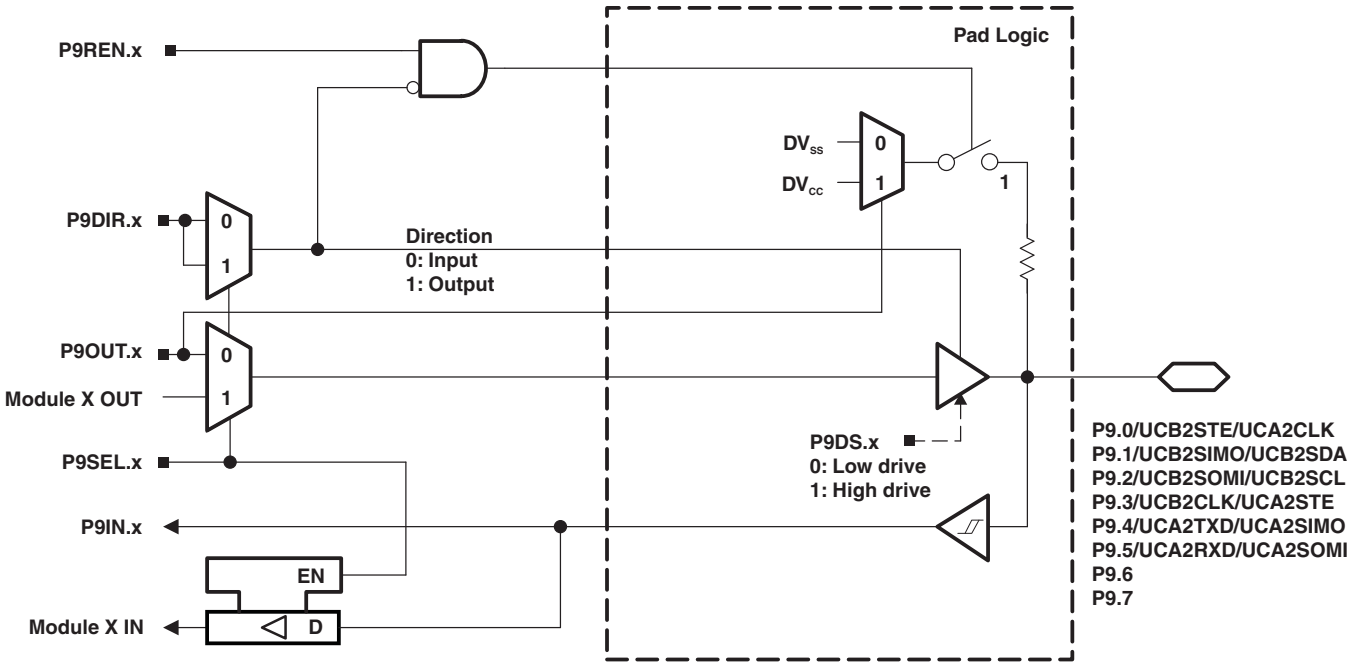


Table 54. Port P9 (P9.0 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P9DIR.x	P9SEL.x
P9.0/UCB2STE/UCA2CLK	0	P9.0 (I/O)	I: 0; O: 1	0
		UCB2STE/UCA2CLK (2) (3)	X	1
P9.1/UCB2SIMO/UCB2SDA	1	P9.1 (I/O)	I: 0; O: 1	0
		UCB2SIMO/UCB2SDA (2) (4)	X	1
P9.2/UCB2SOMI/UCB2SCL	2	P9.2 (I/O)	I: 0; O: 1	0
		UCB2SOMI/UCB2SCL (2) (4)	X	1
P9.3/UCB2CLK/UCA2STE	3	P9.3 (I/O)	I: 0; O: 1	0
		UCB2CLK/UCA2STE (2)	X	1
P9.4/UCA2TXD/UCA2SIMO	4	P9.4 (I/O)	I: 0; O: 1	0
		UCA2TXD/UCA2SIMO (2)	X	1
P9.5/UCA2RXD/UCA2SOMI	5	P9.5 (I/O)	I: 0; O: 1	0
		UCA2RXD/UCA2SOMI (2)	X	1
P9.6	6	P9.6 (I/O)	I: 0; O: 1	0
P9.7	7	P9.7 (I/O)	I: 0; O: 1	0

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA2CLK function takes precedence over UCB2STE function. If the pin is required as UCA2CLK input or output, USCI A2/B2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P10, P10.0 to P10.7, Input/Output With Schmitt Trigger

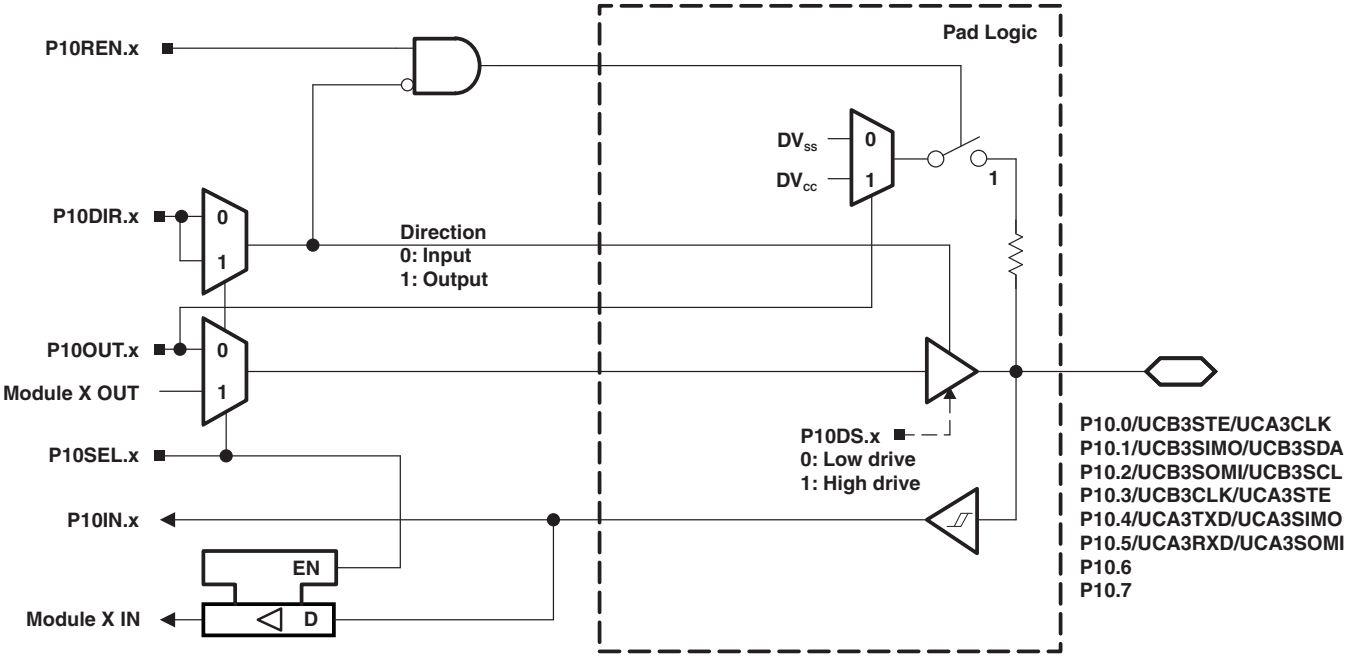


Table 55. Port P10 (P10.0 to P10.7) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P10DIR.x	P10SEL.x
P10.0/UCB3STE/UCA3CLK	0	P10.0 (I/O)	I: 0; O: 1	0
		UCB3STE/UCA3CLK (2) (3)	X	1
P10.1/UCB3SIMO/UCB3SDA	1	P10.1 (I/O)	I: 0; O: 1	0
		UCB3SIMO/UCB3SDA (2) (4)	X	1
P10.2/UCB3SOMI/UCB3SCL	2	P10.2 (I/O)	I: 0; O: 1	0
		UCB3SOMI/UCB3SCL (2) (4)	X	1
P10.3/UCB3CLK/UCA3STE	3	P10.3 (I/O)	I: 0; O: 1	0
		UCB3CLK/UCA3STE (2)	X	1
P10.4/UCA3TXD/UCA3SIMO	4	P10.4 (I/O)	I: 0; O: 1	0
		UCA3TXD/UCA3SIMO (2)	X	1
P10.5/UCA3RXD/UCA3SOMI	5	P10.5 (I/O)	I: 0; O: 1	0
		UCA3RXD/UCA3SOMI (2)	X	1
P10.6	6	P10.6 (I/O)	I: 0; O: 1	0
		Reserved (5)	X	1
P10.7	7	P10.7 (I/O)	I: 0; O: 1	0
		Reserved (5)	x	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA3CLK function takes precedence over UCB3STE function. If the pin is required as UCA3CLK input or output, USCI A3/B3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) The secondary function on these pins are reserved for factory test purposes. Application should keep the P10SEL.x of these ports cleared to prevent potential conflicts with the application.

Port P11, P11.0 to P11.2, Input/Output With Schmitt Trigger

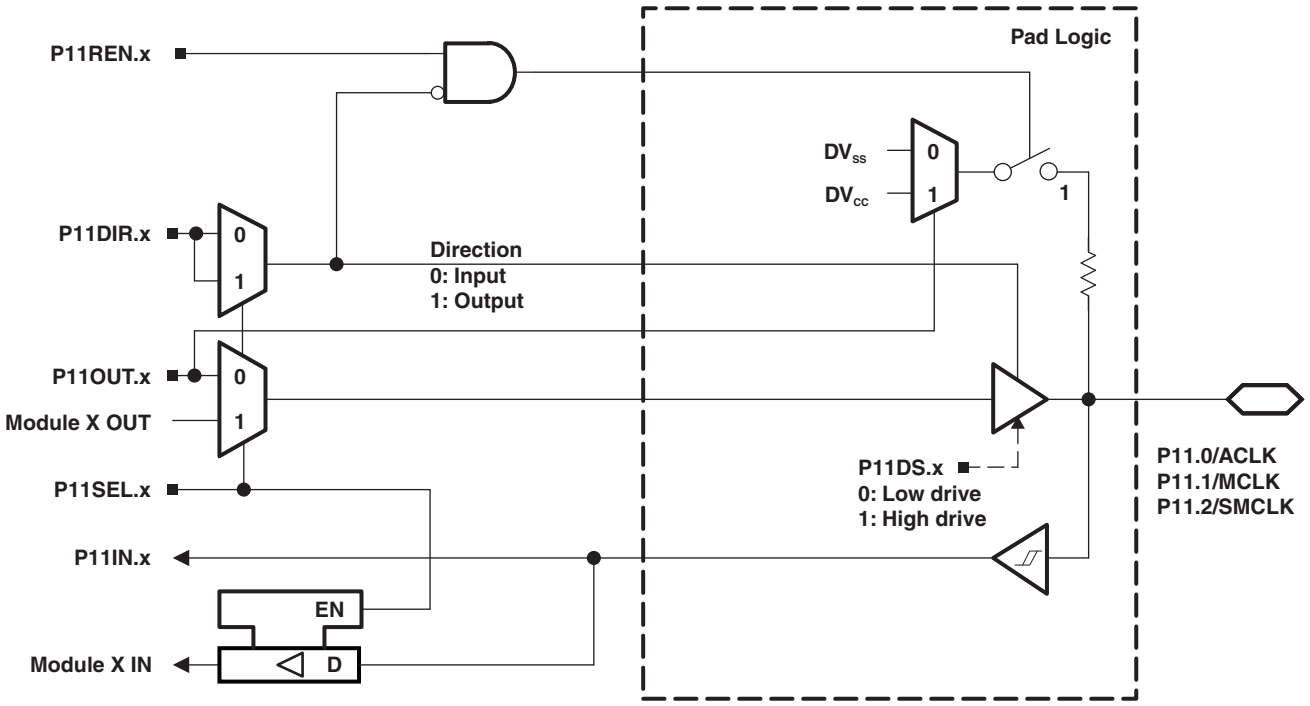
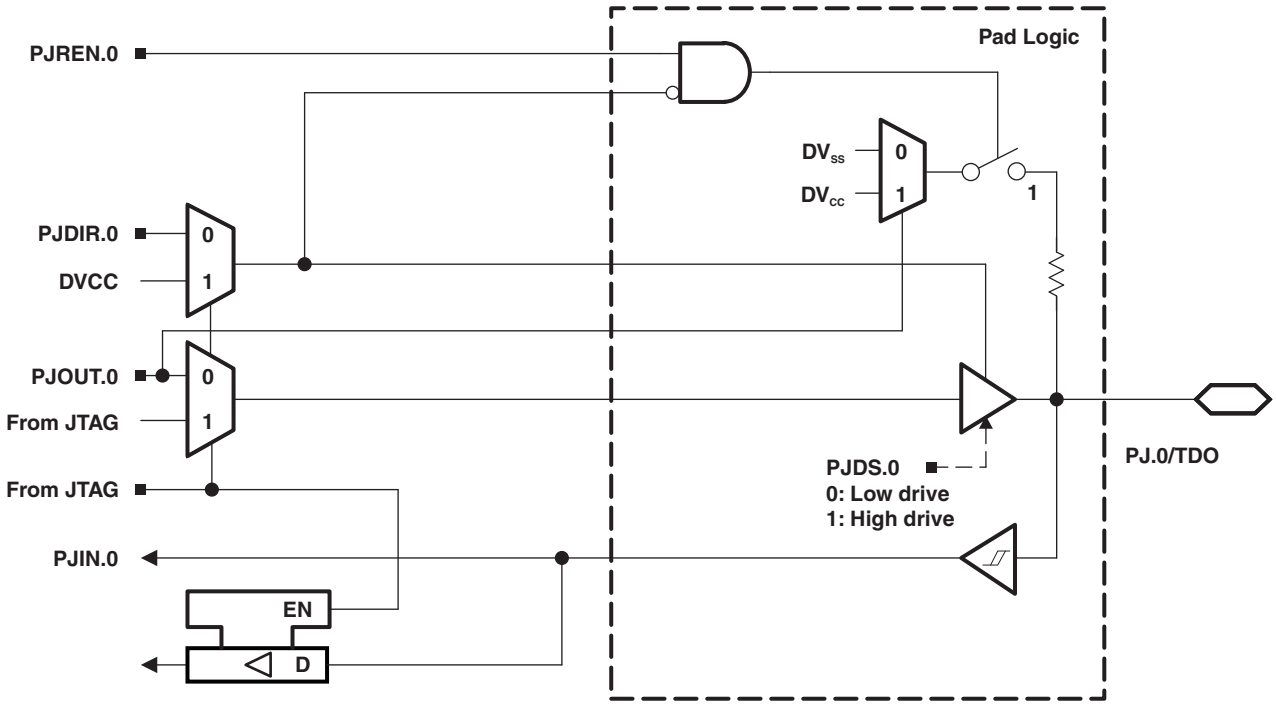


Table 56. Port P11 (P11.0 to P11.2) Pin Functions

PIN NAME (P11.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P11DIR.x	P11SEL.x
P11.0/ACLK	0	P11.0 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P11.1/MCLK	1	P11.1 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P11.2/SMCLK	2	P11.2 (I/O)	I: 0; O: 1	0
		SMCLK	1	1

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

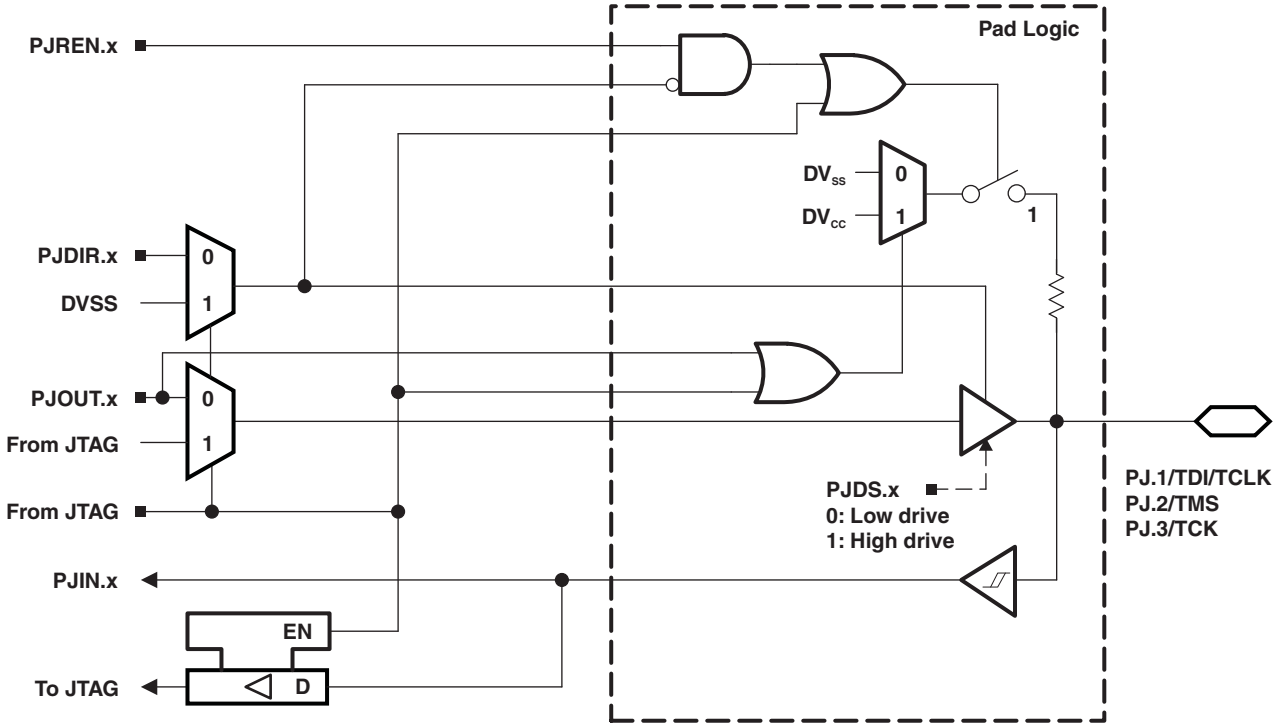


Table 57. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)[2]	I: 0; O: 1
		TDO[3]	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)[2]	I: 0; O: 1
		TDI/TCLK[3] [4]	X
PJ.2/TMS	2	PJ.2 (I/O)[2]	I: 0; O: 1
		TMS[3] [4]	X
PJ.3/TCK	3	PJ.3 (I/O)[2]	I: 0; O: 1
		TCK[3] [4]	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

TLV (Device Descriptor) Structures

Table 58 lists the complete contents of the device descriptor tag-length-value (TLV) structure.

Table 58. Device Descriptor Table(1)

	Description	Address	Size bytes	'F5438	'F5437	'F5436	'F5435	'F5419	'F5418
				Value	Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	54h	54h	54h	54h	54h	54h
	Device ID	01A05h	1	38h	37h	36h	35h	19h	18h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	10h	10h	10h	10h	10h	10h
	ADC12 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Factor	01A1Ah	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Factor	01A20h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit	per unit
Peripheral Descriptor	Peripheral Descriptor Tag	01A26h	1	02h	02h	02h	02h	02h	02h
	Peripheral Descriptor Length	01A27h	1	5Dh	55h	5Eh	56h	5Dh	55h
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 30h	0Eh 30h	0Eh 30h	0Eh 30h	0Eh 30h	0Eh 30h

(1) NA = Not applicable

Table 58. Device Descriptor Table[1] (continued)

	Description	Address	Size bytes	'F5438	'F5437	'F5436	'F5435	'F5419	'F5418
				Value	Value	Value	Value	Value	Value
	Memory 4		2	2Eh 98h	2Eh 98h	2Eh 97h	2Eh 97h	2Eh 96h	2Eh 96h
	Memory 5		0/1	NA	NA	94h	94h	NA	NA
	delimiter		1	00h	00h	00h	00h	00h	00h
	Peripheral count		1	1Fh	1Bh	1Fh	1Fh	1Fh	1Bh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-8		2	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	Package		2	00h 1Fh	00h 1Fh	00h 1Fh	00h 1Fh	00h 1Fh	00h 1Fh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Dh	01h 3Dh	01h 3Dh	01h 3Dh	01h 3Dh	01h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	Port 1/2		2	08h 51h	08h 51h	08h 51h	08h 51h	08h 51h	08h 51h
	Port 3/4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5/6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	Port 7/8		2	02h 54h	02h 54h	02h 54h	02h 54h	02h 54h	02h 54h
	Port 9/10		2	02h 55h	NA	02h 55h	NA	02h 55h	NA
	Port 11/12		2	02h 56h	NA	02h 56h	NA	02h 56h	NA
	JTAG		2	08h 5Fh	0Ch 5F	08h 5Fh	0Ch 5F	08h 5Fh	0Ch 5F
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	RTC		2	0Eh 68h	0Eh 68h	0Eh 68h	0Eh 68h	0Eh 68h	0Eh 68h

Table 58. Device Descriptor Table[1] (continued)

	Description	Address	Size bytes	'F5438	'F5437	'F5436	'F5435	'F5419	'F5418
				Value	Value	Value	Value	Value	Value
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A/B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	USCI_A/B		2	04h 90h	NA	04h 90h	NA	04h 90h	NA
	USCI_A/B		2	04h 90h	NA	04h 90h	NA	04h 90h	NA
	ADC12_A		2	08h D0h	10h D0h	08h D0h	10h D0h	08h D0h	10h D0h
Interrupts	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h	90h
	USCI_B0		1	91h	91h	91h	91h	91h	91h
	ADC12_A		1	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h
	USCI_A2		1	94h	01h	94h	01h	94h	01h
	USCI_B2		1	95h	01h	95h	01h	95h	01h
	DMA		1	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h
	USCI_A3		1	96h	01h	96h	01h	96h	01h
	USCI_B3		1	97h	01h	97h	01h	97h	01h
	P2		1	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h
	delimiter		1	00h	00h	00h	00h	00h	00h

DATA SHEET REVISION HISTORY

REVISION	DESCRIPTION
SLAS612	Initial release
SLAS612A	Removed previews of MSP430F5437IZQW, MSP430F5435IZQW, MSP430F5418IZQW
SLAS612B	All A-suffix devices moved to separate data sheet (SLAS655)
SLAS612C	Corrected base address for USCI_B3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F5418IPN	NRND	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5418	
MSP430F5418IPNR	NRND	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5418	
MSP430F5419IPZ	NRND	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5419	
MSP430F5419IPZR	NRND	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5419	
MSP430F5435IPN	NRND	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5435	
MSP430F5435IPNR	NRND	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5435	
MSP430F5436IPN	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 85		
MSP430F5436IPNR	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 85		
MSP430F5436IPZ	NRND	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5436 REV #	
MSP430F5436IPZR	NRND	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5436 REV #	
MSP430F5436TPN	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 105		
MSP430F5436TPZ	NRND	LQFP	PZ	100		TBD	Call TI	Call TI	-40 to 105		
MSP430F5437IPN	NRND	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5437	
MSP430F5437IPNR	NRND	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5437	
MSP430F5438CY	NRND	DIESALE	Y	0		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438CYS	NRND	WAFERSALE	YS	0		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438IPN	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438IPNR	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438IPZ	NRND	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5438 REV #	
MSP430F5438IPZR	NRND	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5438 REV #	
MSP430F5438IRGC	NRND	VQFN	RGC	64		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F5438IRGZ	NRND	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438IZQW	NRND	BGA MICROSTAR JUNIOR	ZQW	113		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438IZQWR	NRND	BGA MICROSTAR JUNIOR	ZQW	113		TBD	Call TI	Call TI	-40 to 85		
MSP430F5438TPN	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 105		
MSP430F5438TPNR	NRND	LQFP	PN	80		TBD	Call TI	Call TI	-40 to 105		
MSP430F5438TPZ	NRND	LQFP	PZ	100		TBD	Call TI	Call TI	-40 to 105		
MSP430F5438TPZR	NRND	LQFP	PZ	100		TBD	Call TI	Call TI	-40 to 105		
XMS430F5438IPZ	NRND	LQFP	PZ	100		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

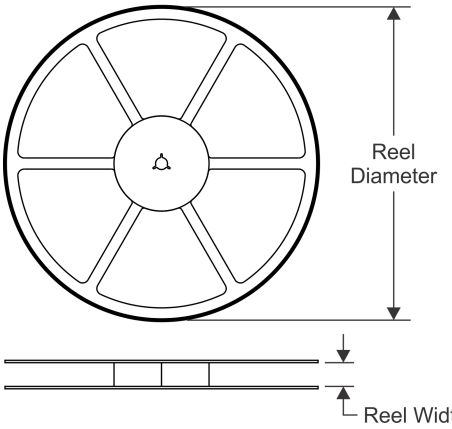
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

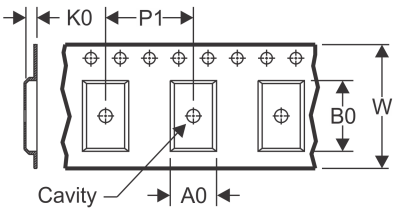
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

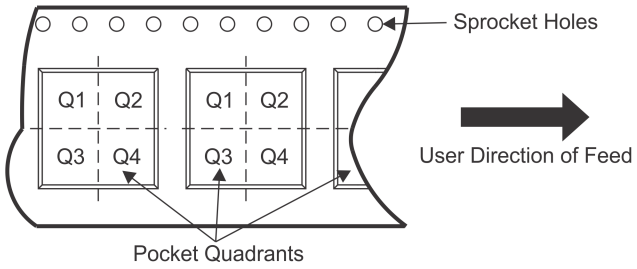


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

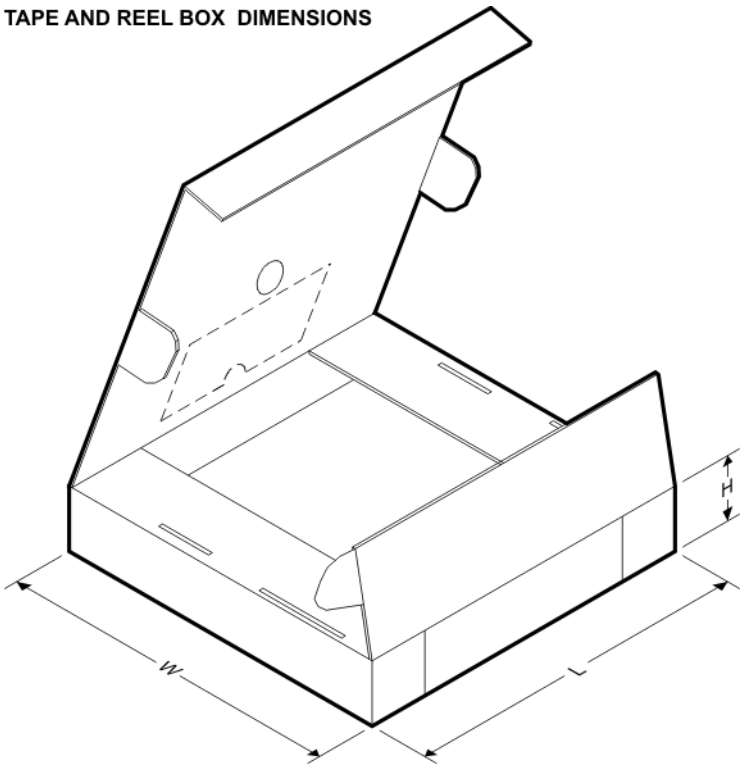
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5418IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5435IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5436IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5437IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5438IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2

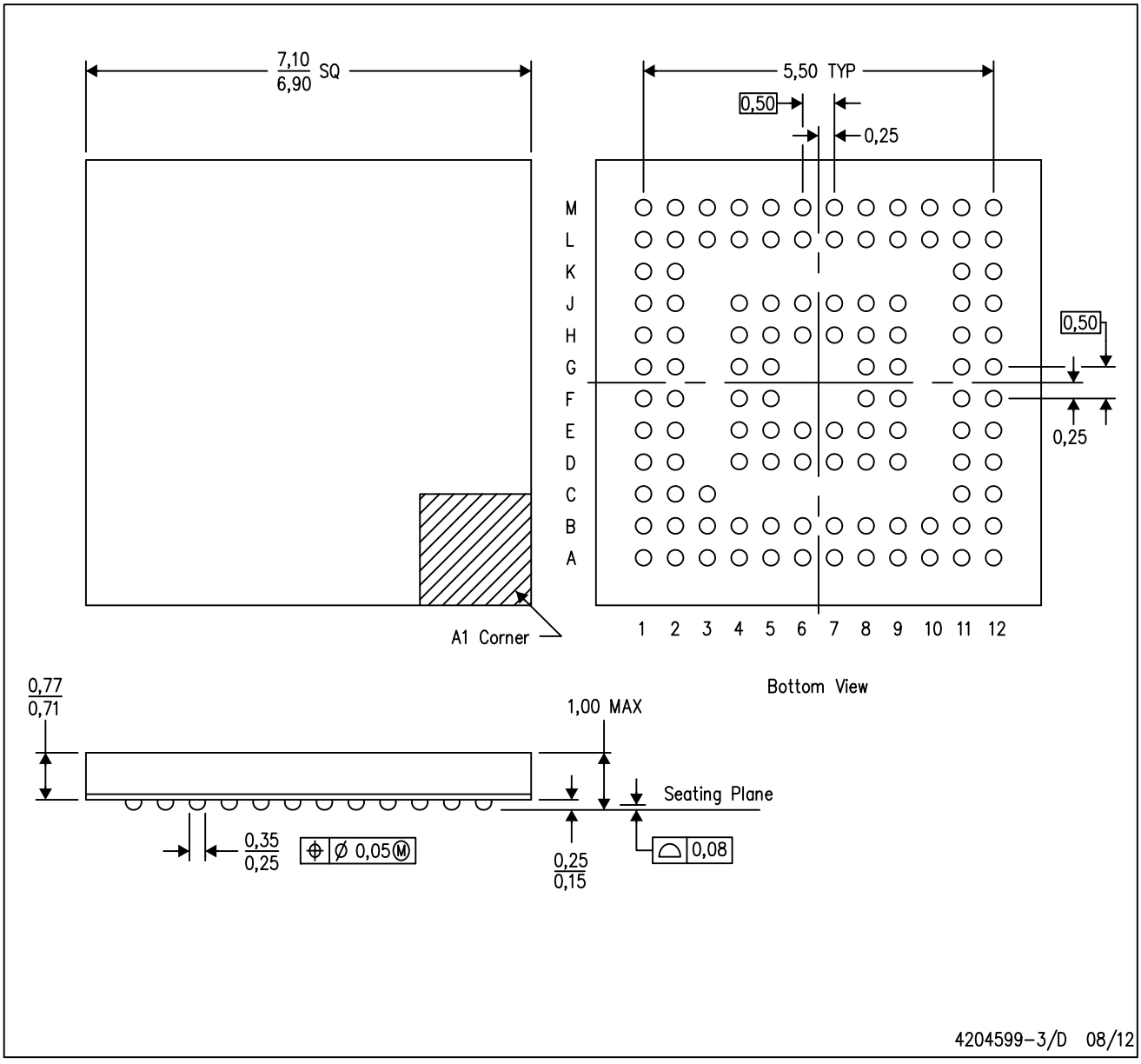
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5418IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F5435IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F5436IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5437IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F5438IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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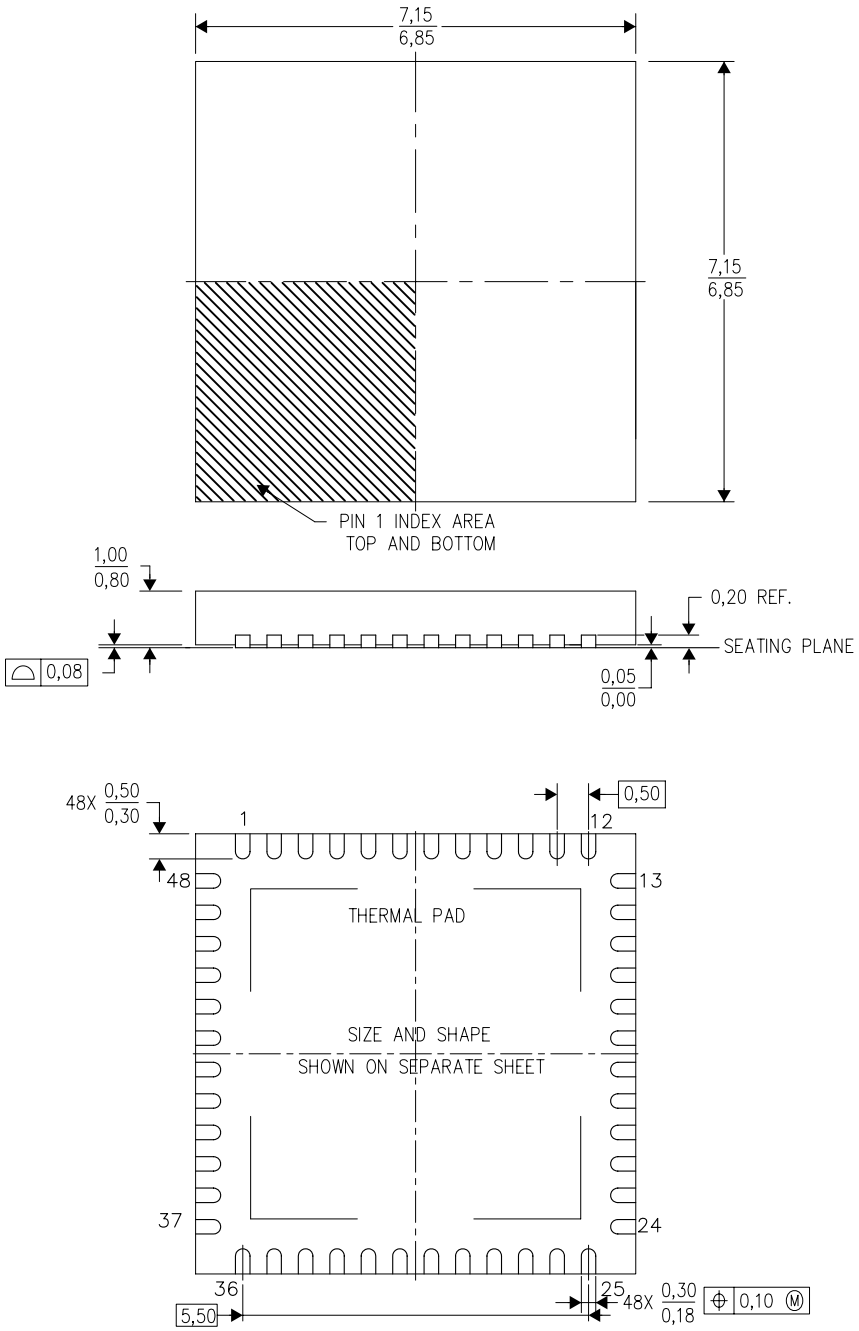
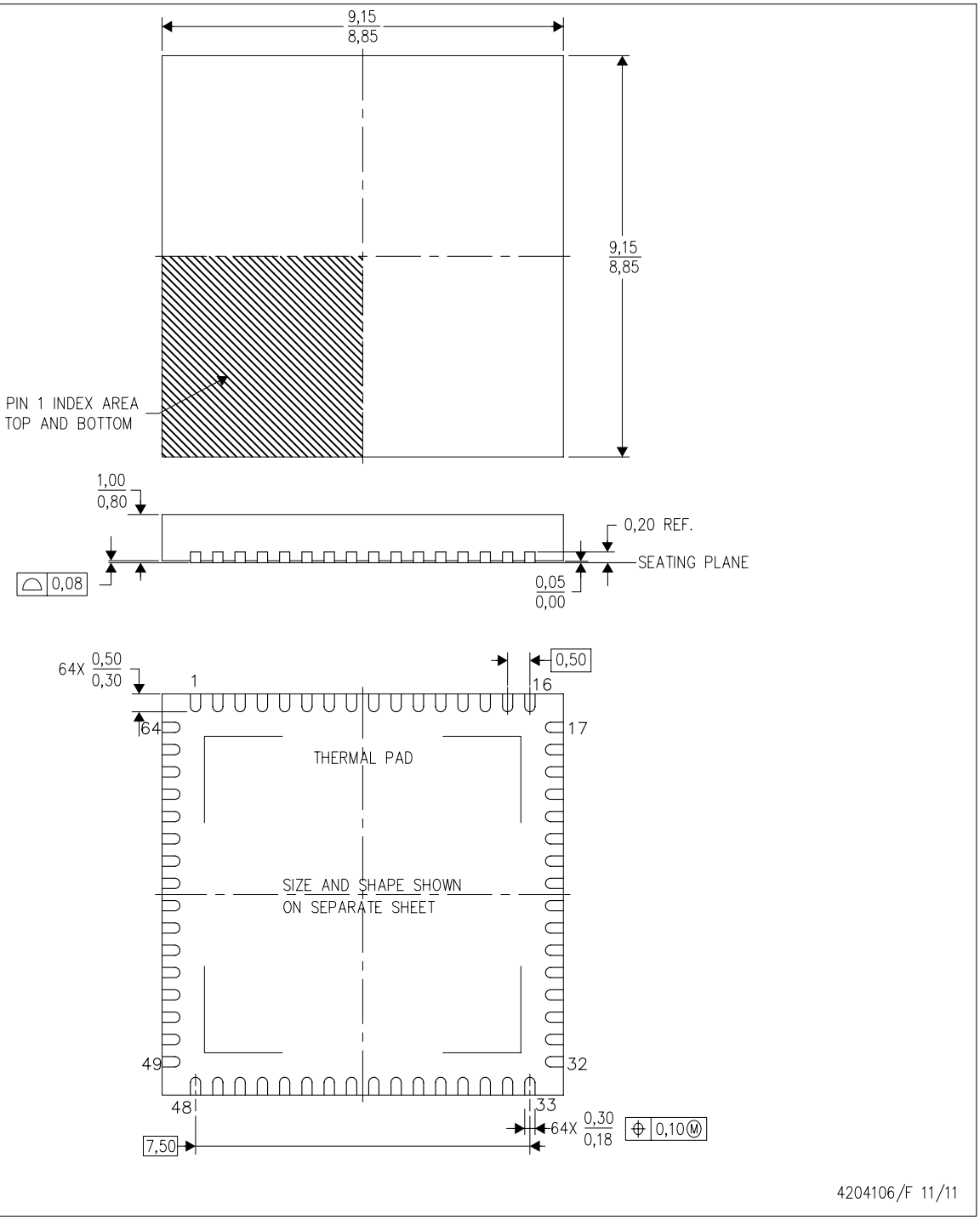
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

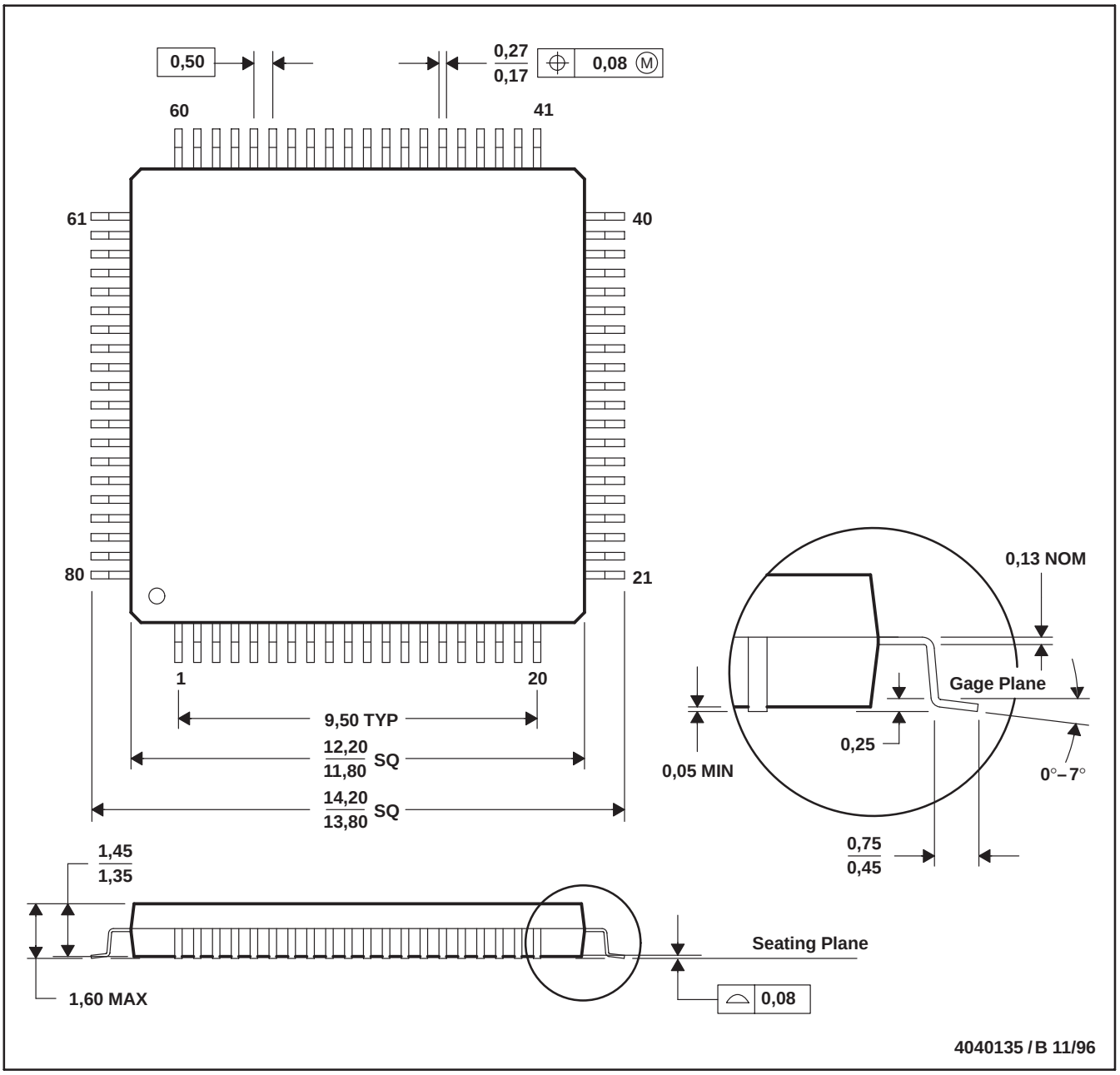
RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

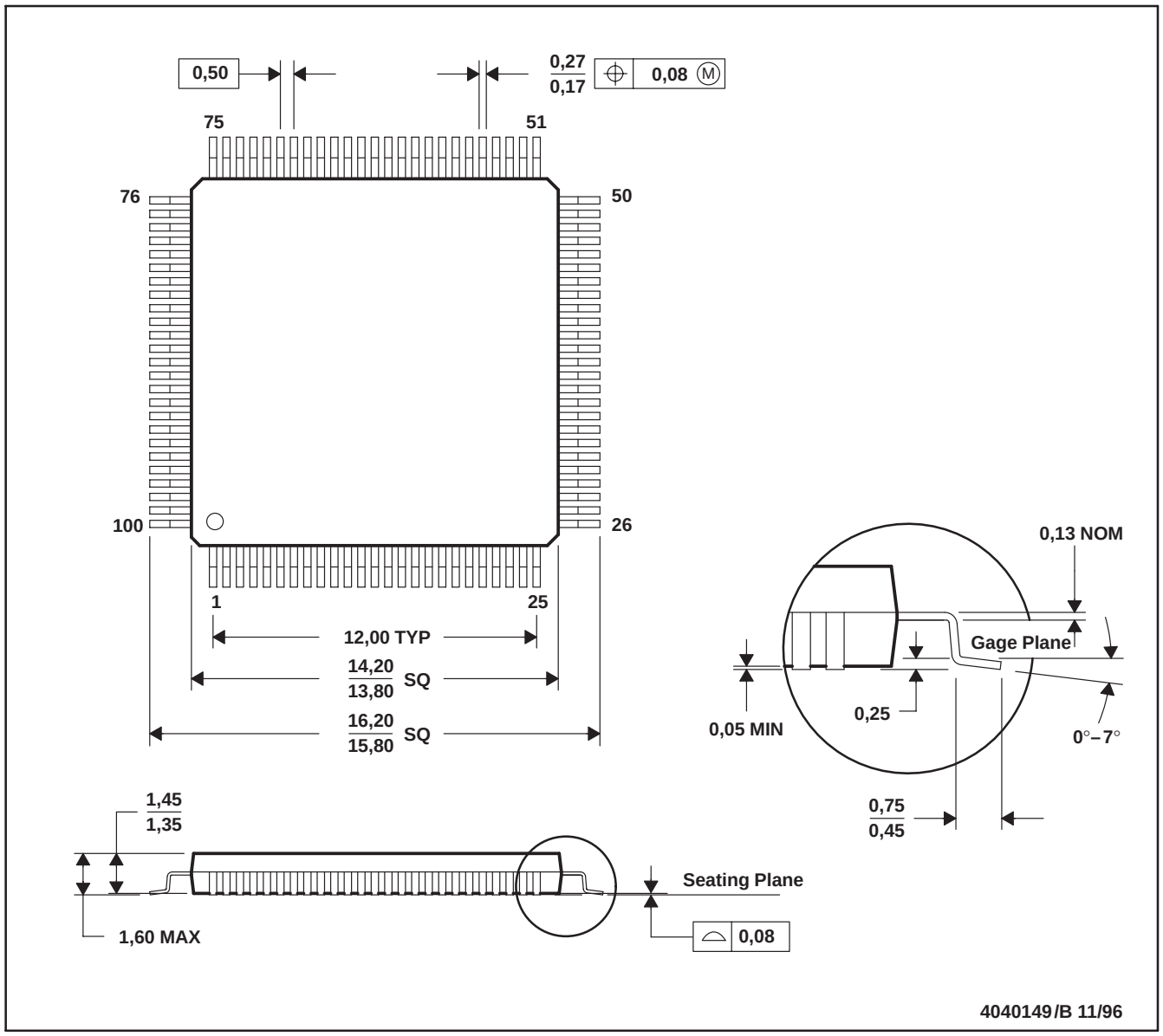
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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